

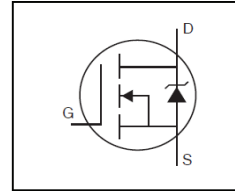
**Features**

- Advanced Process Technology
- Ultra Low On-Resistance
- Logic Level Gate Drive
- 150°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified \*

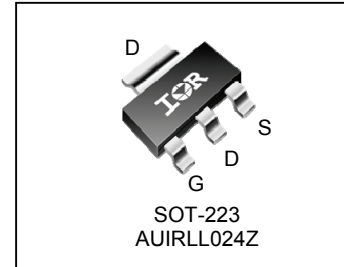
**Description**

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

HEXFET® Power MOSFET



<b>V<sub>DSS</sub></b>	<b>55V</b>
<b>R<sub>DS(on)</sub> typ.</b>	<b>48mΩ</b>
<b>max.</b>	<b>60mΩ</b>
<b>I<sub>D</sub></b>	<b>5.0A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRLL024Z	SOT-223	Tape and Reel	2500	AUIRLL024ZTR

**Absolute Maximum Ratings**

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>A</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V ⑦	5.0	A
I <sub>D</sub> @ T <sub>A</sub> = 70°C	Continuous Drain Current, V <sub>GS</sub> @ 10V ⑦	4.0	
I <sub>DM</sub>	Pulsed Drain Current ①	40	W
P <sub>D</sub> @ T <sub>A</sub> = 25°C	Maximum Power Dissipation (PCB Mount) ⑦	2.8	
P <sub>D</sub> @ T <sub>A</sub> = 25°C	Maximum Power Dissipation (PCB Mount) ⑧	1.0	
	Linear Derating Factor (PCB Mount) ⑦	0.02	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 16	V
E <sub>AS</sub>	Single Pulse Avalanche Energy (Thermally Limited) ②	21	mJ
E <sub>AS (Tested)</sub>	Single Pulse Avalanche Energy (Tested Value) ⑥	38	
I <sub>AR</sub>	Avalanche Current ①	See Fig. 12a, 12b, 15, 16	A
E <sub>AR</sub>	Repetitive Avalanche Energy ⑤		mJ
T <sub>J</sub>	Operating Junction and	-55 to + 150	°C
T <sub>STG</sub>	Storage Temperature Range		

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
R <sub>θJA</sub>	Junction-to-Ambient (PCB Mount, steady state) ⑦	—	45	°C/W
R <sub>θJA</sub>	Junction-to-Ambient (PCB Mount, steady state) ⑧	—	120	

HEXFET® is a registered trademark of Infineon.

\*Qualification standards can be found at [www.infineon.com](http://www.infineon.com)

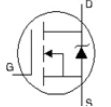
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	55	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.049	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	48	60	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 3.0A ③
		—	—	80		V <sub>GS</sub> = 5.0V, I <sub>D</sub> = 3.0A ③
		—	—	100		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 3.0A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	3.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Trans conductance	7.5	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 3.0A
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 55V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 55V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	200	nA	V <sub>GS</sub> = 16V
	Gate-to-Source Reverse Leakage	—	—	-200		V <sub>GS</sub> = -16V

**Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

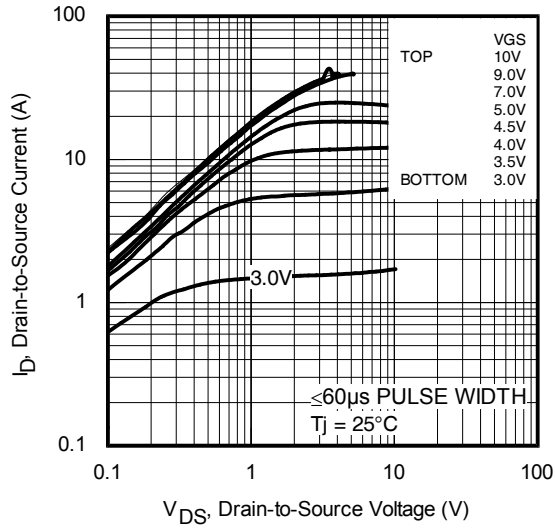
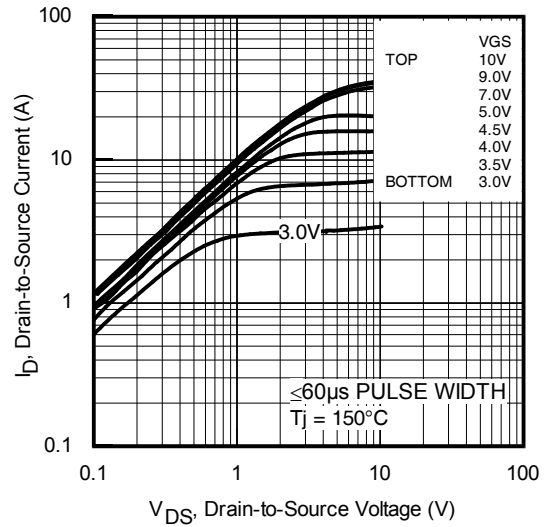
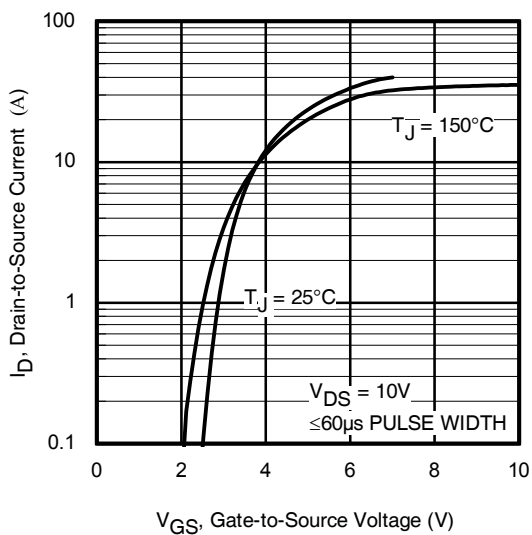
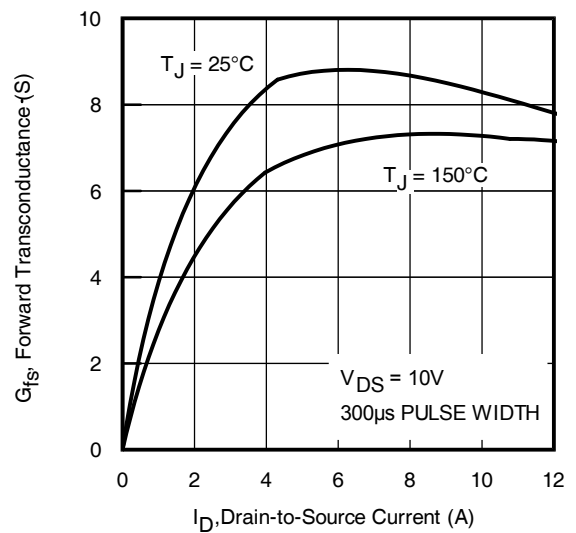
Q <sub>g</sub>	Total Gate Charge	—	7.0	11	nC	I <sub>D</sub> = 3.0A
Q <sub>gs</sub>	Gate-to-Source Charge	—	1.5	—		V <sub>DS</sub> = 44V
Q <sub>gd</sub>	Gate-to-Drain Charge	—	4.0	—		V <sub>GS</sub> = 5.0V ③
t <sub>d(on)</sub>	Turn-On Delay Time	—	8.6	—	ns	V <sub>DD</sub> = 28V
t <sub>r</sub>	Rise Time	—	33	—		I <sub>D</sub> = 3.0A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	20	—		R <sub>G</sub> = 56Ω
t <sub>f</sub>	Fall Time	—	15	—		V <sub>GS</sub> = 5.0V ③
C <sub>iss</sub>	Input Capacitance	—	380	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	66	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	36	—		f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	220	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V, f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	53	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 44V, f = 1.0MHz
C <sub>oss eff.</sub>	Effective Output Capacitance	—	93	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 44V ④

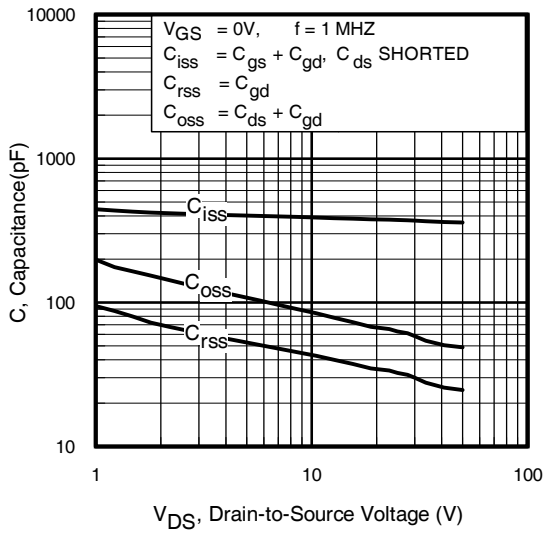
**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	5.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	40		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 3.0A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	15	23	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 3.0A, V <sub>DD</sub> = 28V
Q <sub>rr</sub>	Reverse Recovery Charge	—	9.1	14	nC	di/dt = 100A/μs ③
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

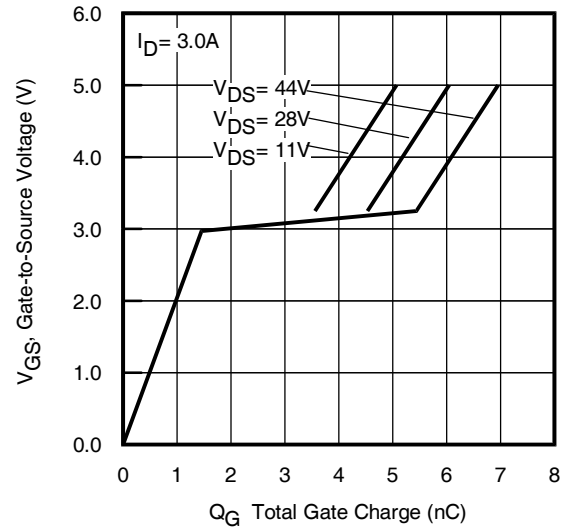
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Limited by T<sub>Jmax</sub>, Starting T<sub>J</sub> = 25°C, L = 4.8mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 3.A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.
- ③ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.
- ④ C<sub>oss eff.</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑤ Limited by T<sub>Jmax</sub>, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population, starting T<sub>J</sub> = 25°C, L = 4.8mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 3.0A, V<sub>GS</sub> = 10V.
- ⑦ When mounted on 1 inch square copper board.
- ⑧ When mounted on FR-4 board using minimum recommended footprint.

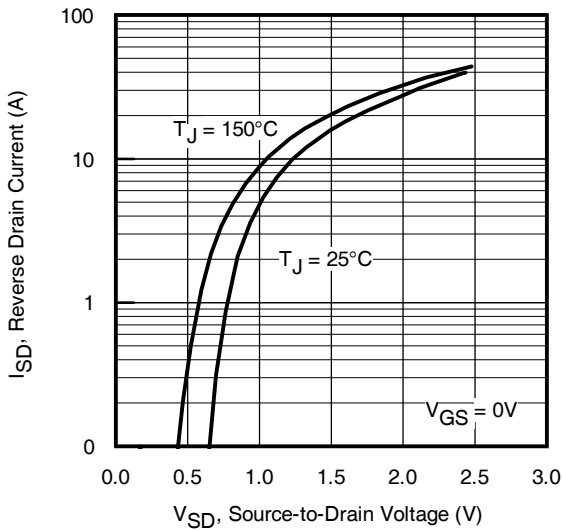

**Fig. 1** Typical Output Characteristics

**Fig. 2** Typical Output Characteristics

**Fig. 3** Typical Transfer Characteristics

**Fig. 4** Typical Forward Trans conductance vs. Drain Current



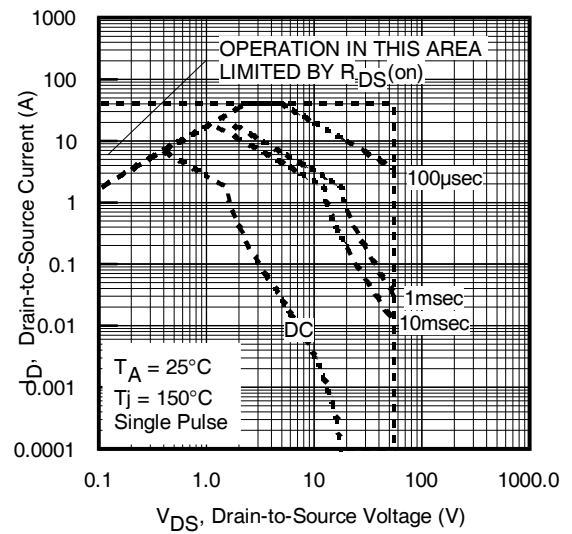
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



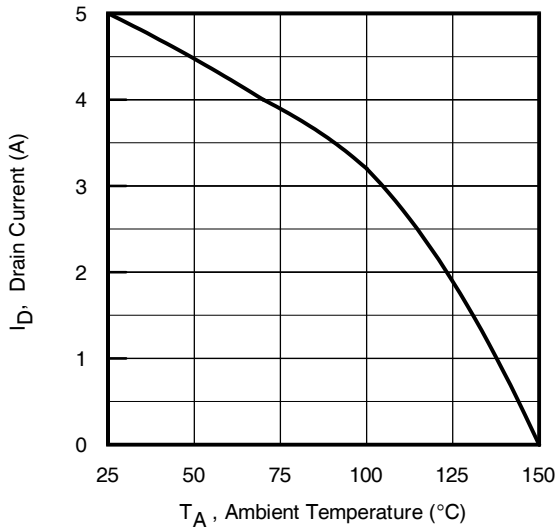
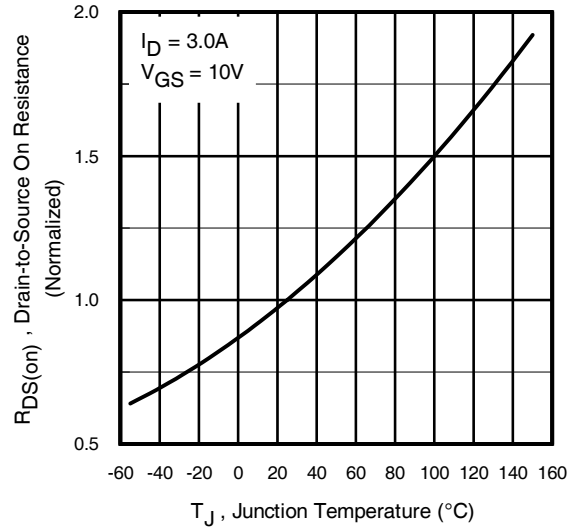
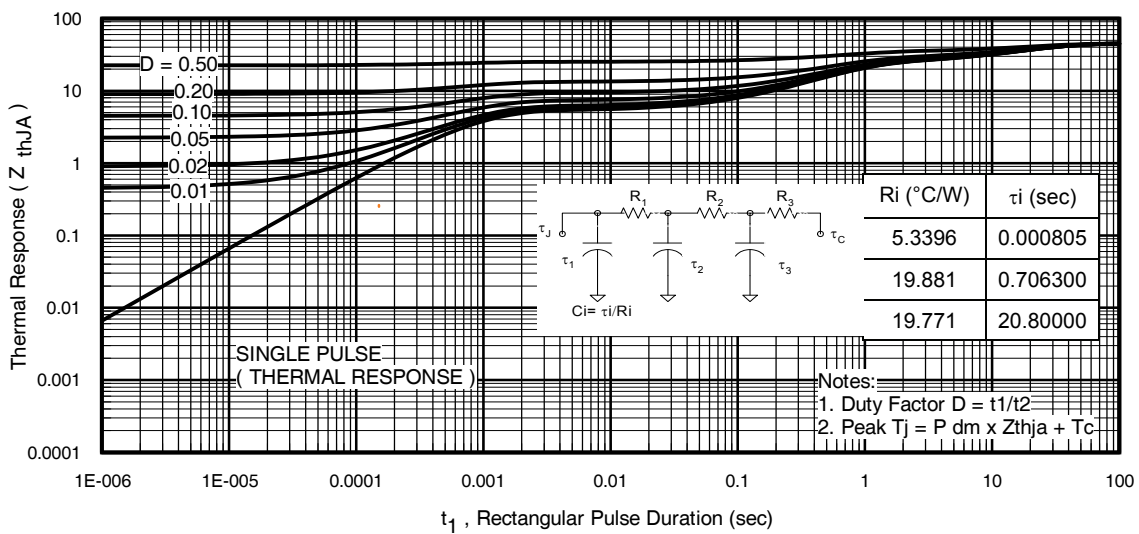
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

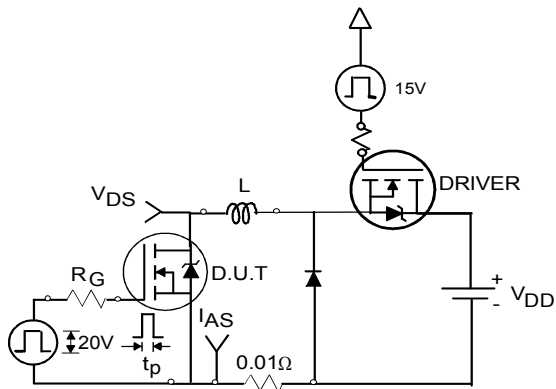
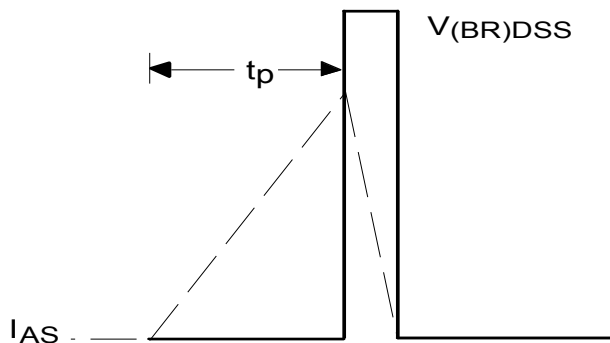
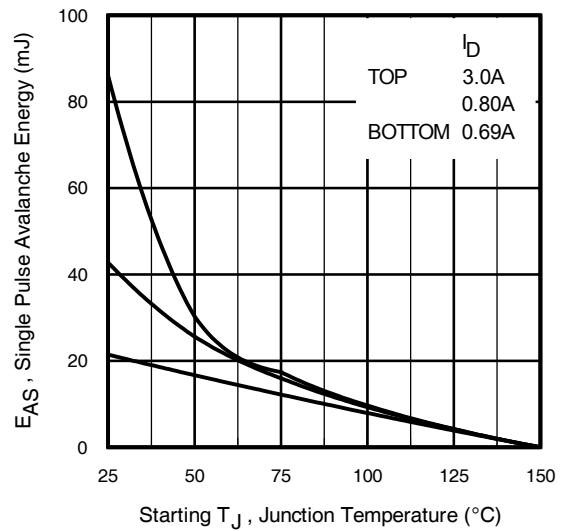
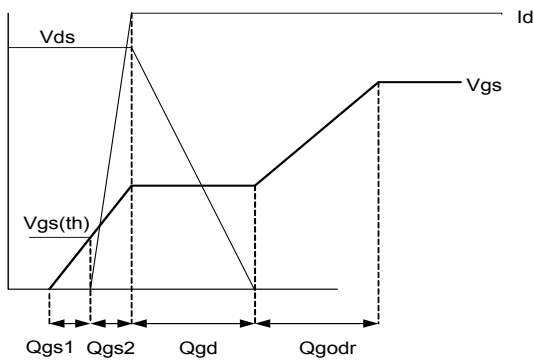
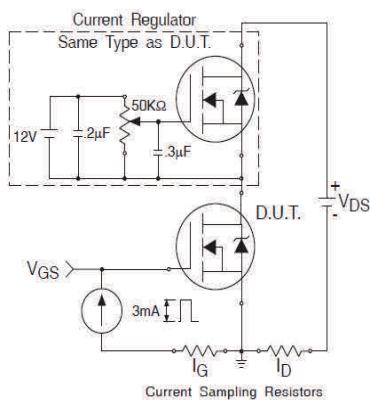
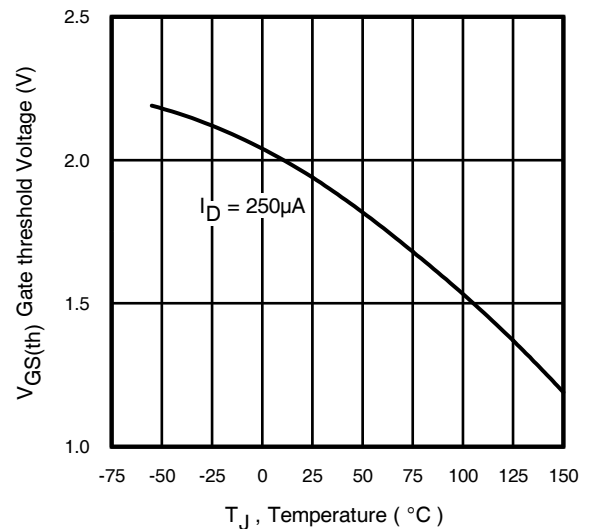


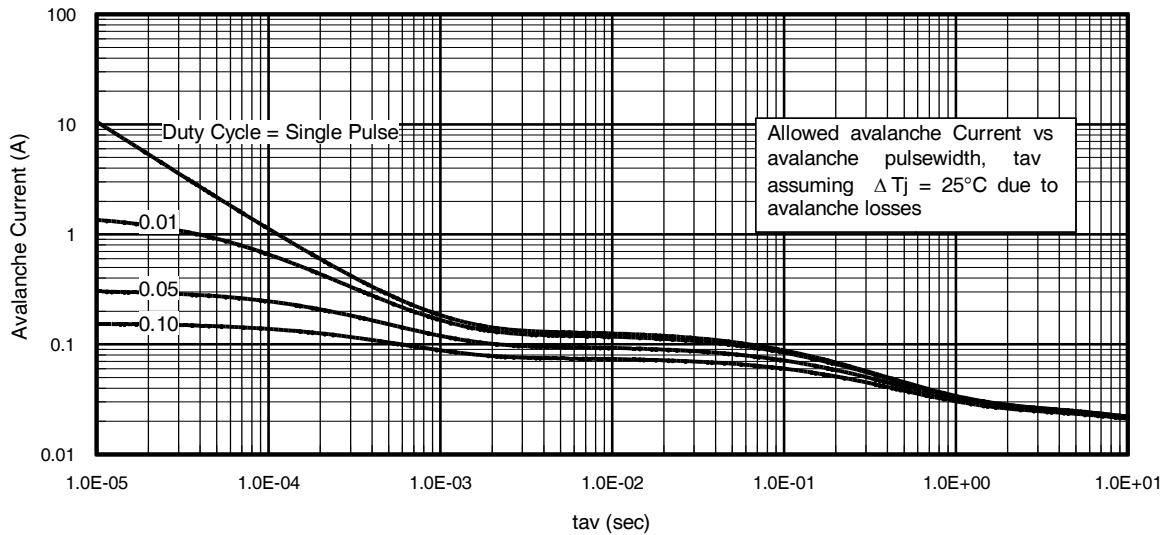
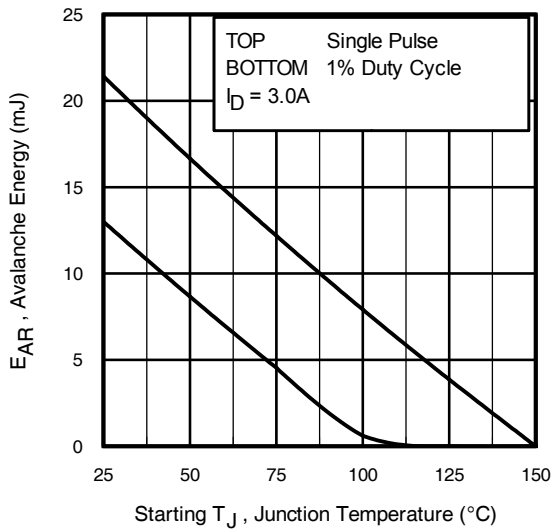
**Fig. 7** Typical Source-to-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area


**Fig 9.** Maximum Drain Current Vs. Ambient Temperature

**Fig 10.** Normalized On-Resistance vs. Temperature

**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient


**Fig 12a. Unclamped Inductive Test Circuit**

**Fig 12b. Unclamped Inductive Waveforms**

**Fig 12c. Maximum Avalanche Energy Vs. Drain Current**

**Fig 13a. Basic Gate Charge Waveform**

**Fig 13b. Gate Charge Test Circuit**

**Fig 14. Threshold Voltage vs. Temperature**


**Fig 15.** Typical Avalanche Current vs. Pulse width

**Fig 16.** Maximum Avalanche Energy vs. Temperature

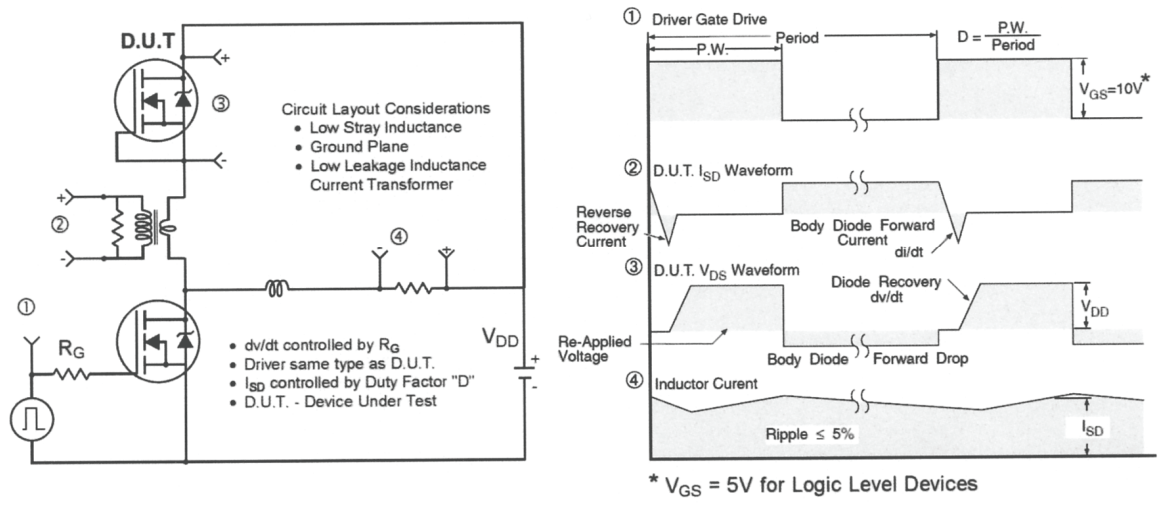
**Notes on Repetitive Avalanche Curves , Figures 15, 16:  
(For further info, see AN-1005 at www.infineon.com)**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

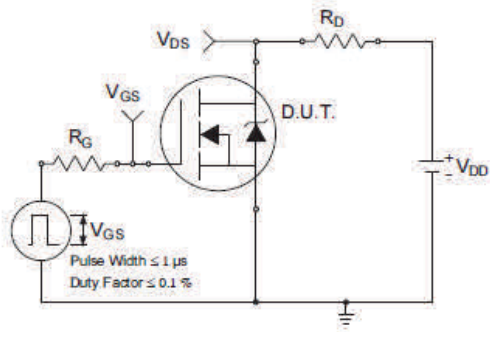
$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [ 1.3 \cdot BV \cdot Z_{th} ]$$

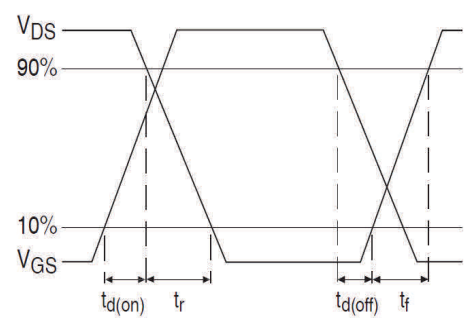
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



**Fig 17.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

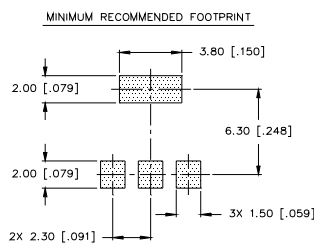
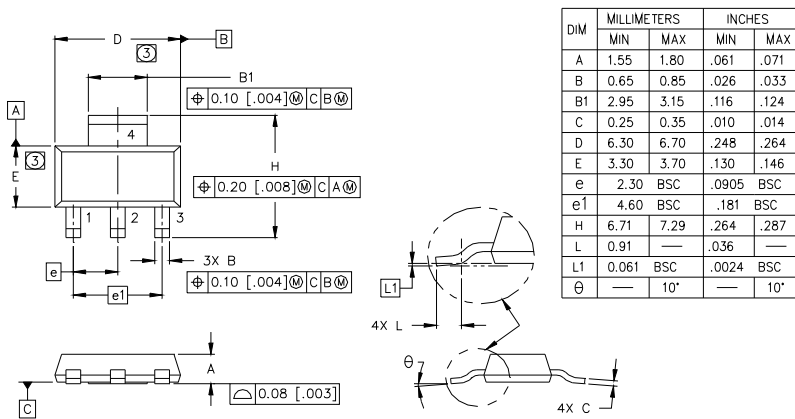


**Fig 18a.** Switching Time Test Circuit



**Fig 18b.** Switching Time Waveforms

## SOT-223 (TO-261AA) Package Outline (Dimensions are shown in millimeters (inches))



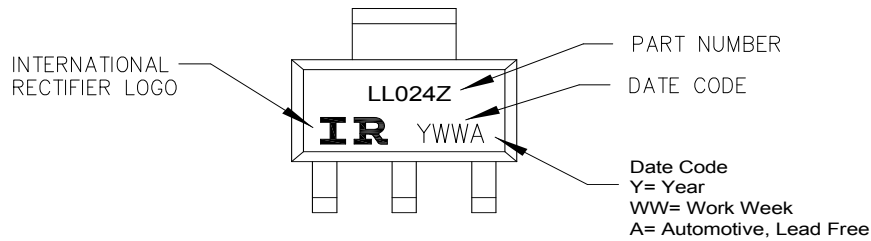
**LEAD ASSIGNMENTS**

- 1 = GATE
- 2 = DRAIN
- 3 = SOURCE
- 4 = DRAIN

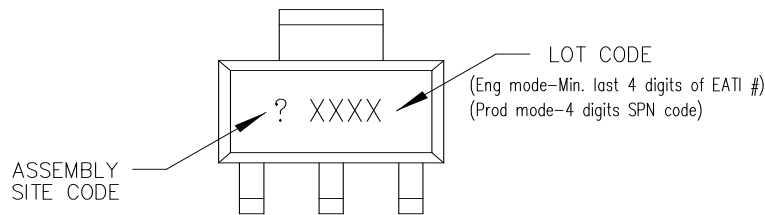
**NOTES:**

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS DO NOT INCLUDE MOLD FLASH.
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-261AA.
5. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

## SOT-223(TO-261AA) Part Marking Information

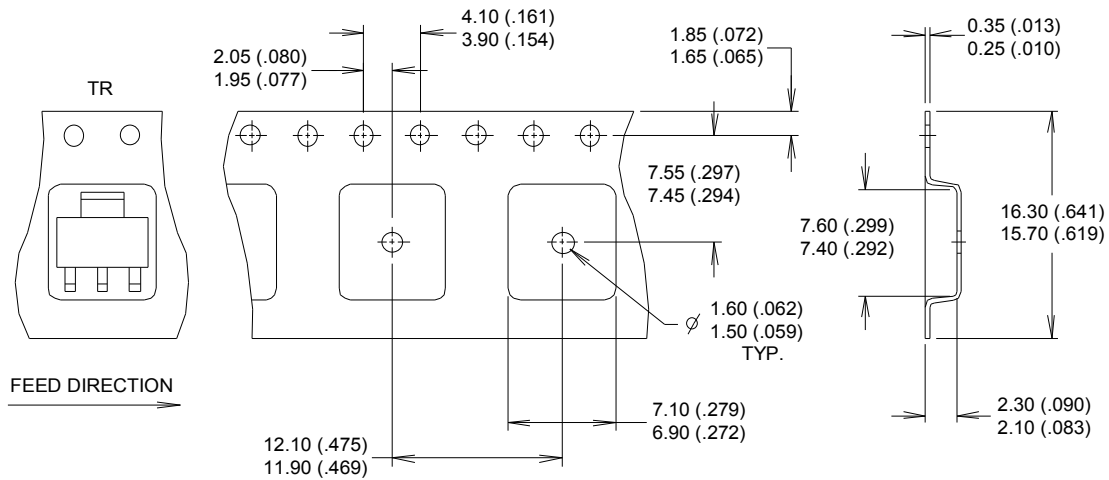


TOP MARKING

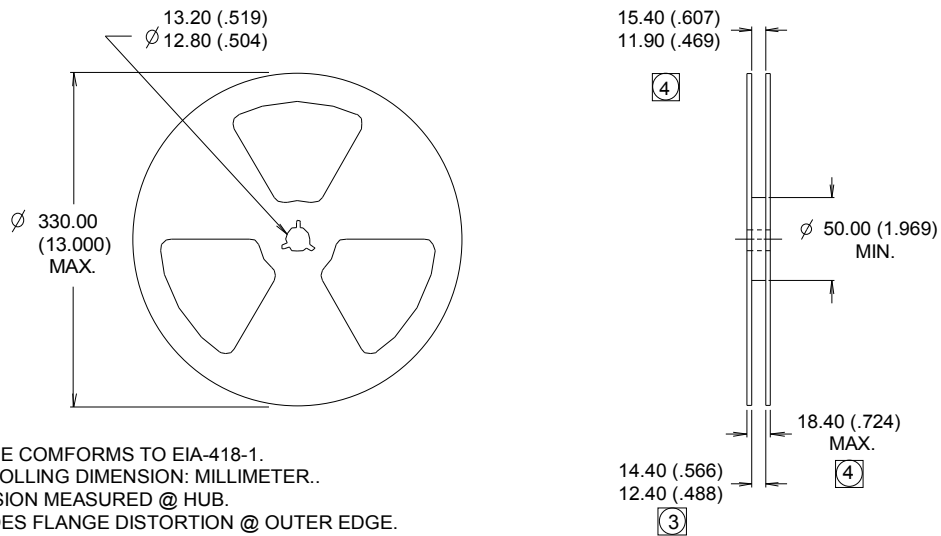


BOTTOM MARKING

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**SOT-223(TO-261AA) Tape and Reel** (Dimensions are shown in millimeters (inches))

**NOTES :**

1. CONTROLLING DIMENSION: MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.
3. EACH  $\varnothing 330.00$  (13.00) REEL CONTAINS 2,500 DEVICES.


**NOTES :**

1. OUTLINE COMFORMS TO EIA-418-1.
2. CONTROLLING DIMENSION: MILLIMETER..
- ③ DIMENSION MEASURED @ HUB.
- ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information**

<b>Qualification Level</b>		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		SOT-223	MSL1
<b>ESD</b>	Machine Model	Class M1B (+/- 100V) <sup>†</sup> AEC-Q101-002	
	Human Body Model	Class H0 (+/- 250V) <sup>†</sup> AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 1125V) <sup>†</sup> AEC-Q101-005	
<b>RoHS Compliant</b>		Yes	

† Highest passing voltage.

**Revision History**

Date	Comments
3/26/2014	<ul style="list-style-type: none"> <li>Added "Logic Level Gate Drive" bullet in the features section on page 1</li> <li>Updated part marking on page 9</li> <li>Updated data sheet with new IR corporate template</li> </ul>
10/29/2015	<ul style="list-style-type: none"> <li>Updated datasheet with corporate template</li> <li>Corrected ordering table on page 1.</li> </ul>

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