

Dual N-channel 60 V, 23 mΩ typ., 33 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 double island package

Datasheet - production data

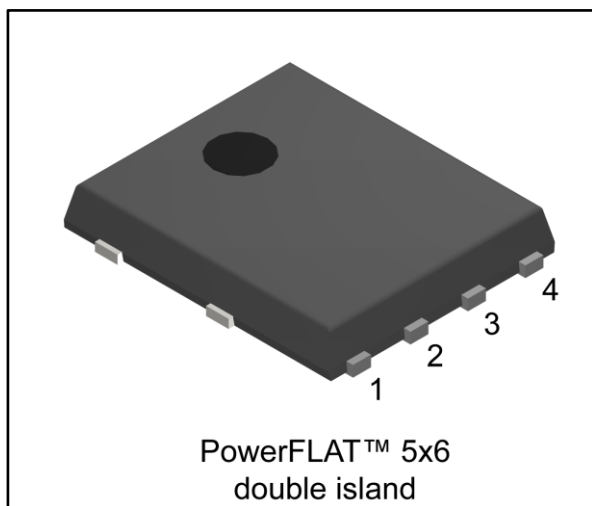
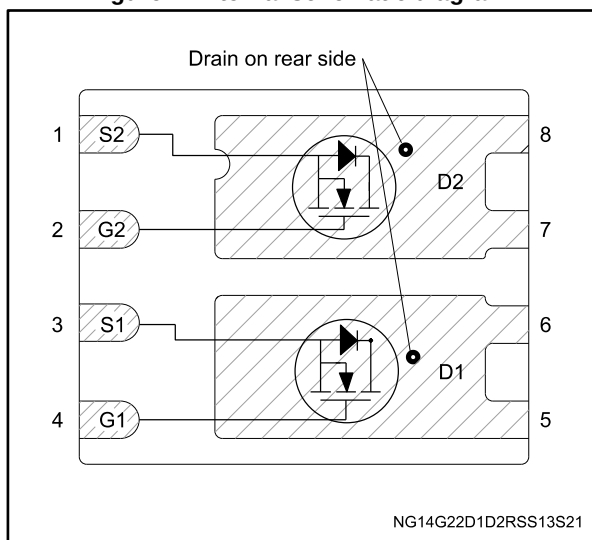


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STL36DN6F7	60 V	27 mΩ	33 A

- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This dual N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STL36DN6F7	36DN6F7	PowerFLAT™ 5x6 double island	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves).....	5
3	Test circuits	7
4	Package information	8
	4.1 PowerFLAT 5x6 double island type C package information.....	9
	4.2 Packing information.....	12
5	Revision history	14

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	33	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	23	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	9	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	6.7	A
$I_{DM}^{(1)(3)}$	Drain current (pulsed)	132	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	36	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	58	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	W
T_J	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature range		

Notes:(1) This value is rated according to R_{thj-c} .(2) The value is rated according to $R_{thj-pcb}$.

(3) Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction- case	2.6	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	$^\circ\text{C/W}$

Notes:(1) When mounted on FR-4 board of 1 inch², 2oz Cu, $t < 10\text{ s}$.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 1 mA	60			V
I _{DSS}	Zero gate voltage drain current	V _{DS} = 60 V, V _{GS} = 0 V			1	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2		4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 4.5 A		23	27	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 30 V, f = 1 MHz, V _{GS} = 0 V	-	420	-	pF
C _{oss}	Output capacitance		-	215	-	pF
C _{rss}	Reverse transfer capacitance		-	16	-	pF
Q _g	Total gate charge	V _{DD} = 30 V, I _D = 9 A V _{GS} = 0 to 10 V (see Figure 14: "Test circuit for gate charge behavior")	-	8	-	nC
Q _{gs}	Gate-source charge		-	2.3	-	nC
Q _{gd}	Gate-drain charge		-	2.1	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 30 V, I _D = 4.5 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	7.85	-	ns
t _r	Rise time		-	3.25	-	ns
t _{d(off)}	Turn-off delay time		-	12.1	-	ns
t _f	Fall time		-	3.95	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{SD} ⁽¹⁾	Forward on voltage	I _{SD} = 9 A, V _{GS} = 0 V	-		1.2	V
t _{rr}	Reverse recovery time	I _D = 9 A, di/dt = 100 A/μs V _{DD} = 48 V (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	17.1		ns
Q _{rr}	Reverse recovery charge		-	6.67		nC
I _{RRM}	Reverse recovery current		-	0.8		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

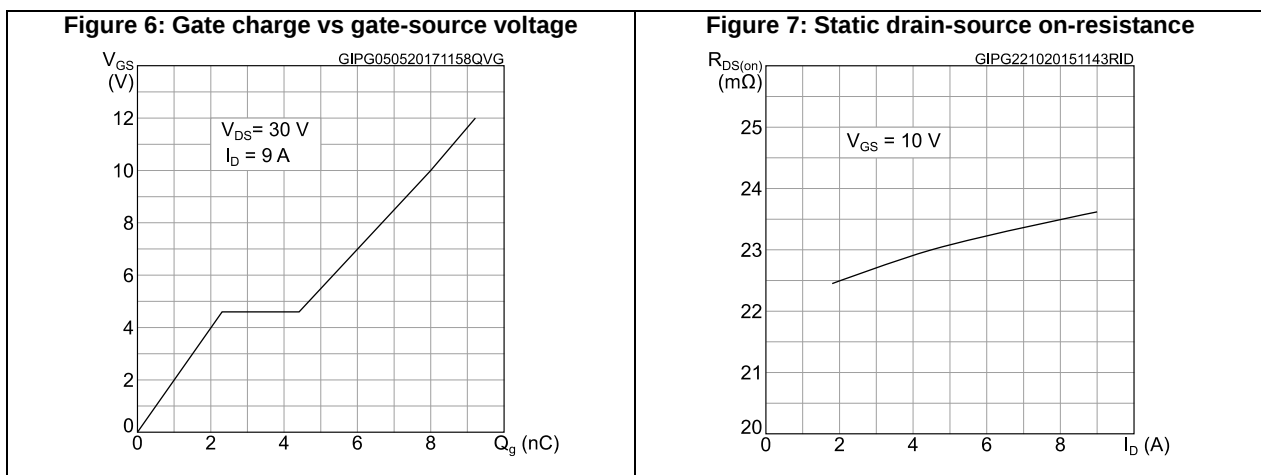
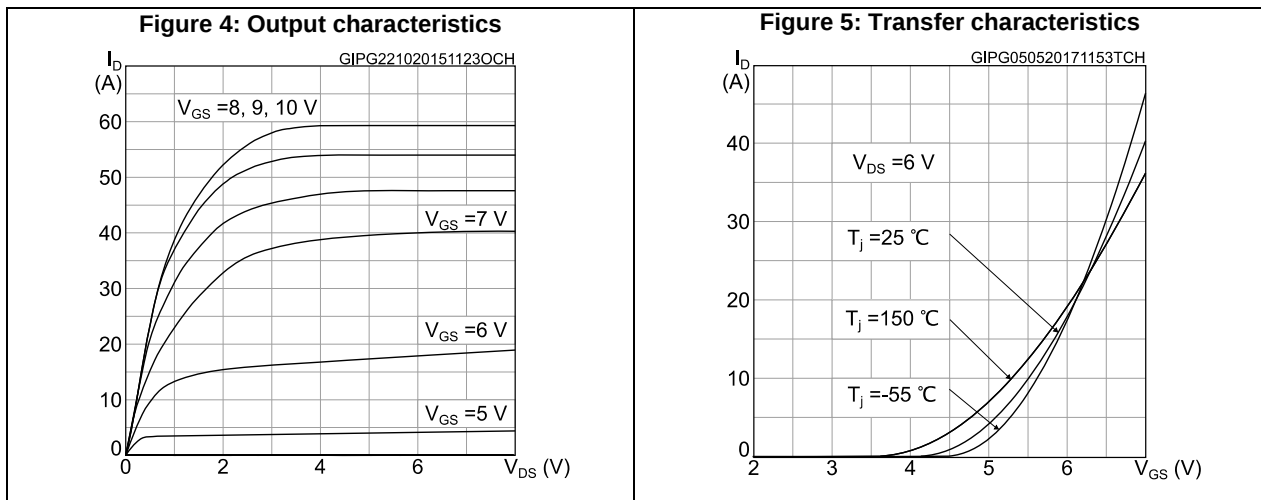
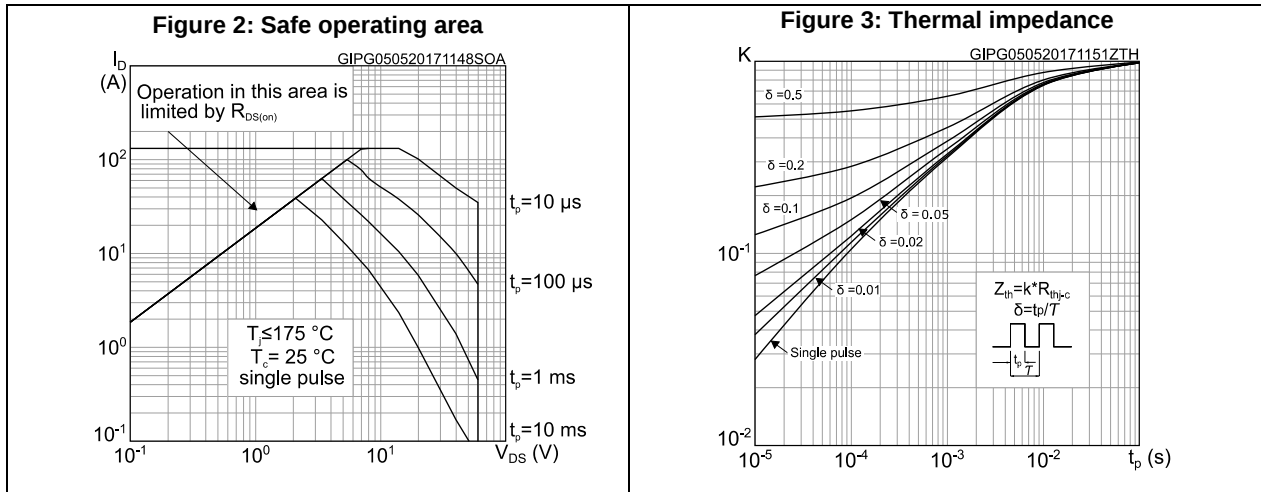


Figure 8: Capacitance variations

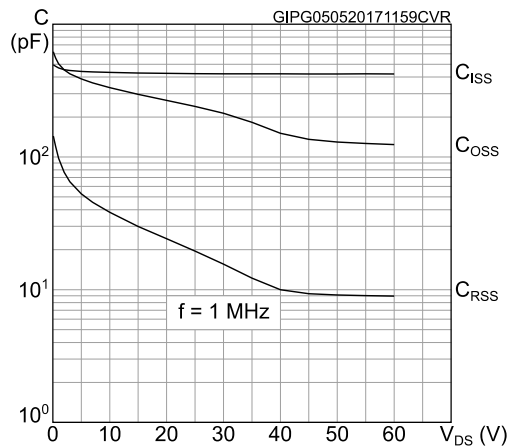


Figure 9: Normalized gate threshold voltage vs temperature

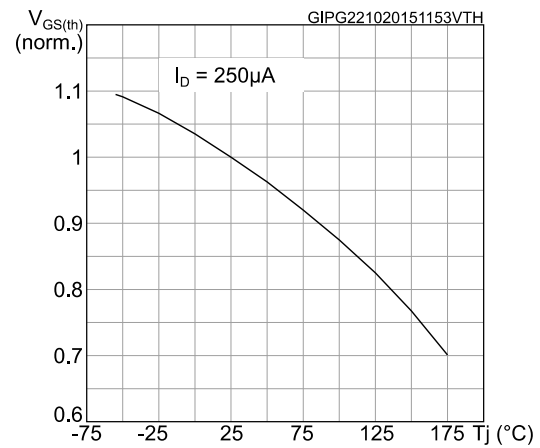


Figure 10: Normalized on-resistance vs temperature

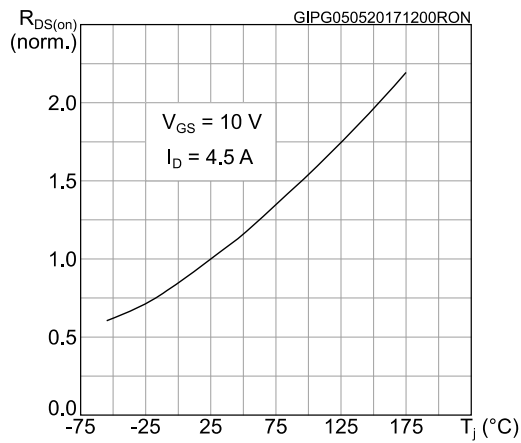
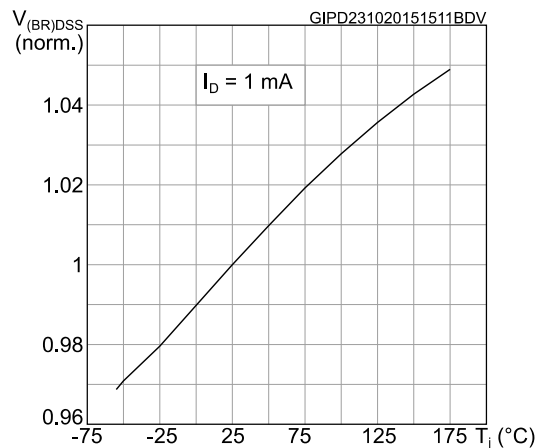
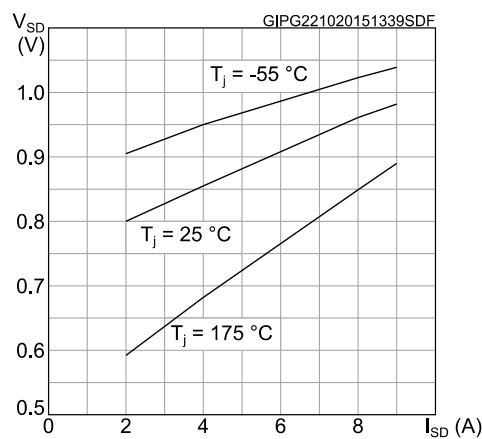
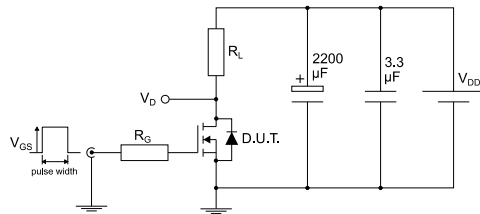
Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

Figure 12: Source-drain diode forward characteristics



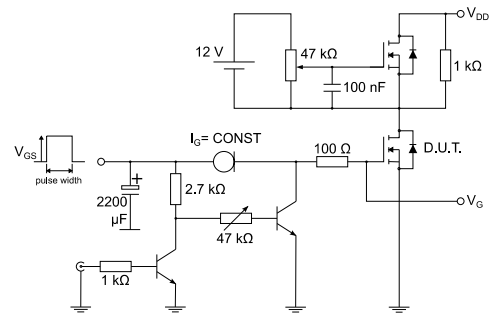
3 Test circuits

Figure 13: Test circuit for resistive load switching times



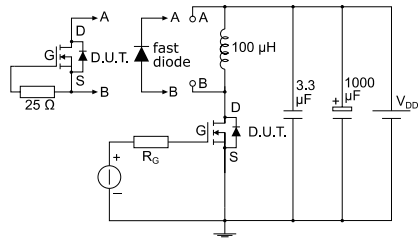
AM01468v1

Figure 14: Test circuit for gate charge behavior



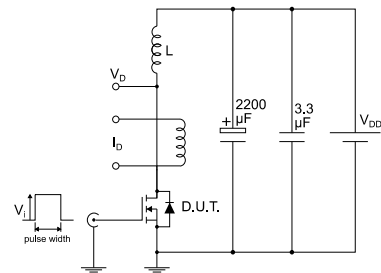
AM01469v1

Figure 15: Test circuit for inductive load switching and diode recovery times



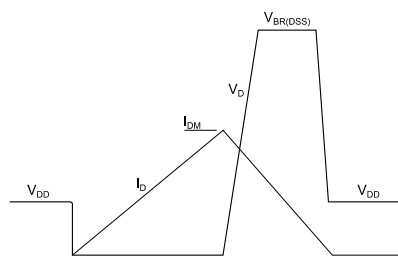
AM01470v1

Figure 16: Unclamped inductive load test circuit



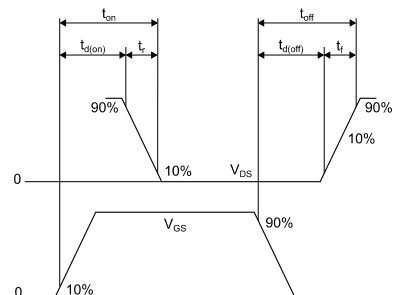
AM01471v1

Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 PowerFLAT 5x6 double island type C package information

Figure 19: PowerFLAT™ 5x6 double island type C package outline

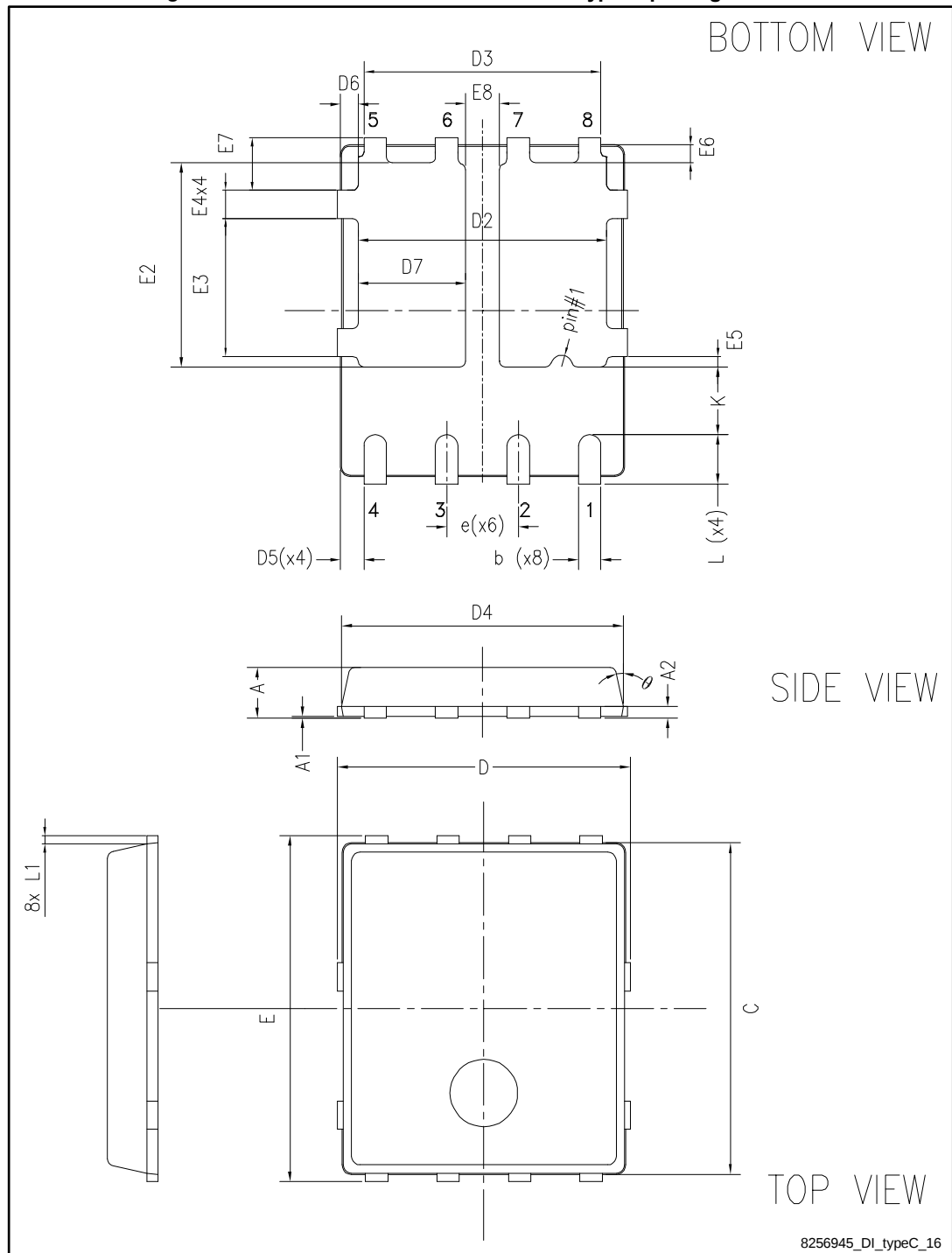
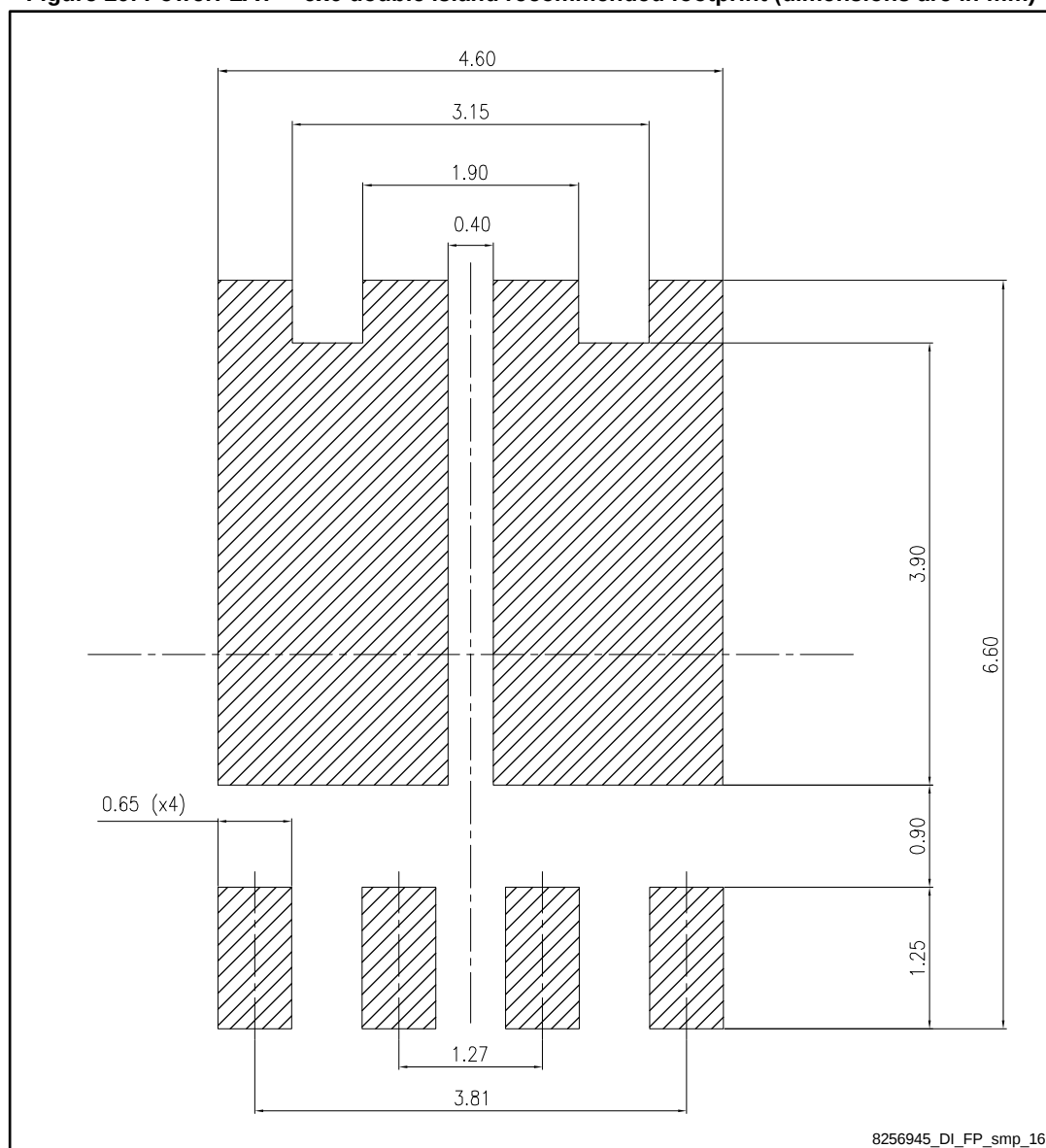


Table 8: PowerFLAT™ 5x6 double island type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
D7	1.68		1.98
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
E8	0.55		0.75
K	1.05		1.35
L	0.725		1.025
L1	0.05	0.15	0.25
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 double island recommended footprint (dimensions are in mm)



4.2 Packing information

Figure 21: PowerFLAT™ 5x6 tape (dimensions are in mm)

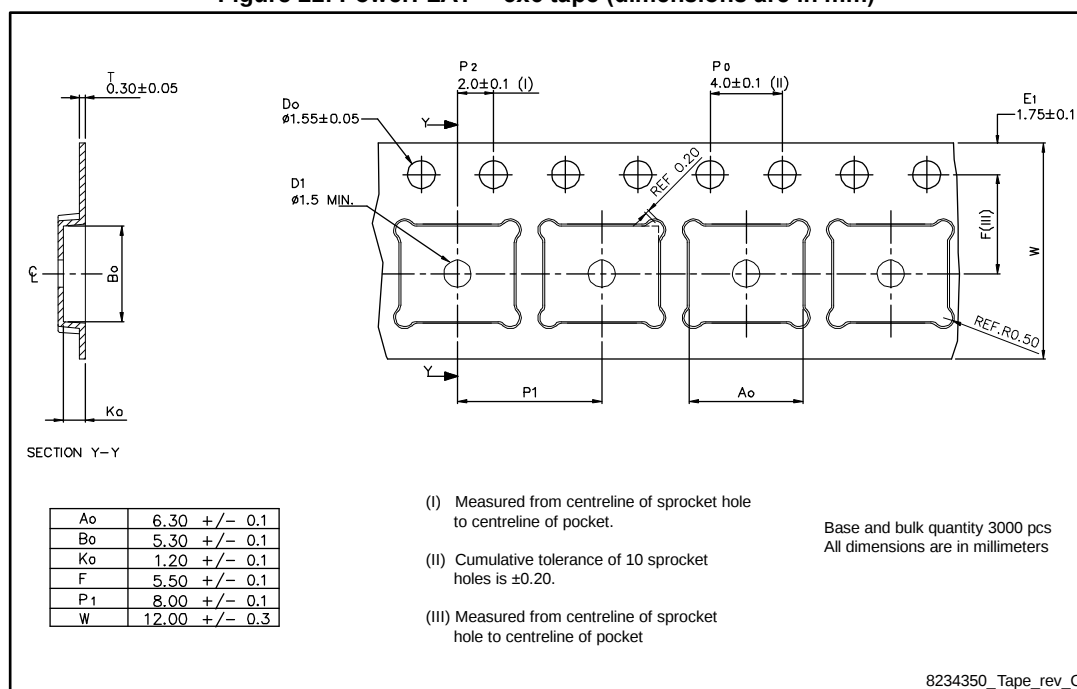


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

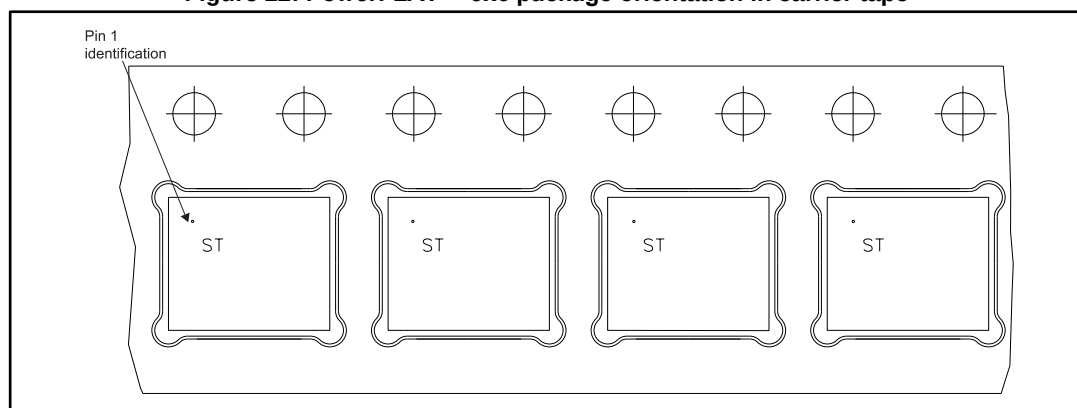
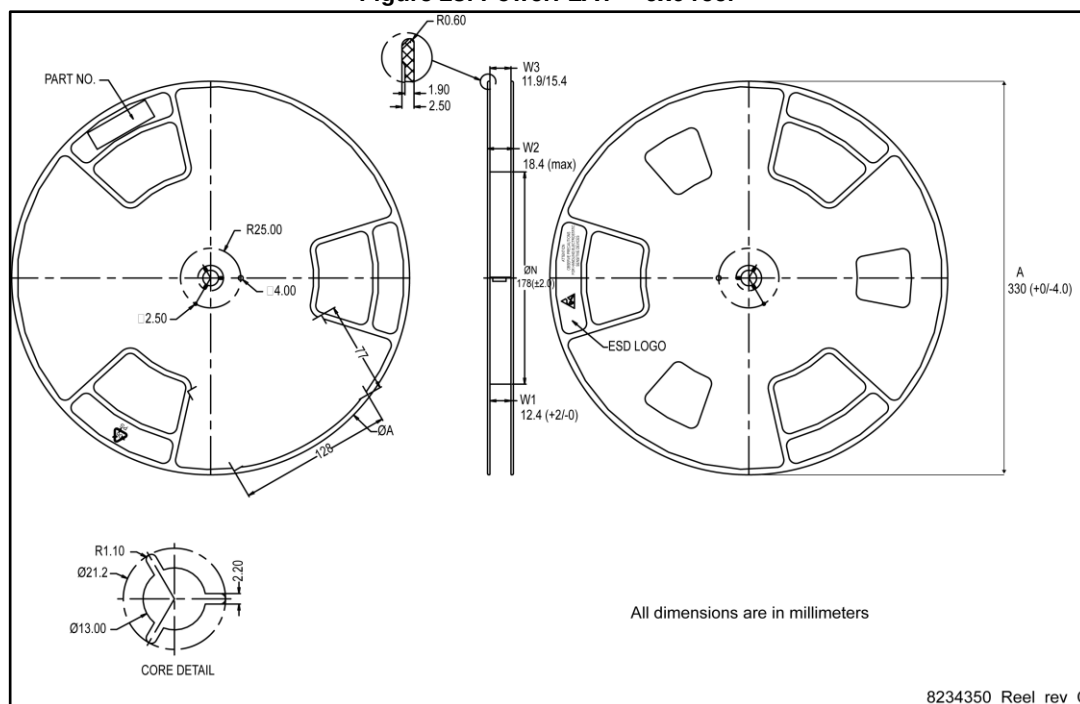


Figure 23: PowerFLAT™ 5x6 reel



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
20-Aug-2015	1	First release.
22-Oct-2015	2	Document status promoted from preliminary to production data. Updated <i>Section 2: "Electrical ratings"</i> and <i>Section 3: "Electrical characteristics"</i> . Added <i>Section 3.1: "Electrical characteristics (curves)"</i> .
10-May-2017	3	Modified title and features table on cover page. Modified <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 3: "Thermal data"</i> , <i>Table 4: "On /off states"</i> Modified <i>Figure 4: "Output characteristics"</i> , <i>Figure 5: "Transfer characteristics"</i> , <i>Figure 7: "Static drain-source on-resistance"</i> and <i>Figure 12: "Source-drain diode forward characteristics"</i> . Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics – All rights reserved