



PSMNR90-40SSH

N-channel 40 V, 0.9 m Ω , 375 Amps continuous, standard level MOSFET in LPAK88 using NextPowerS3 Technology

1 May 2019

Product data sheet

1. General description

375 Amp continuous current, standard level gate drive, N-channel enhancement mode MOSFET in LPAK88 package. NextPowerS3 family using Nexperia's unique "SchottkyPlus" technology delivers high efficiency and low spiking performance usually associated with MOSFETs with an integrated Schottky or Schottky-like diode but without problematic high leakage current. NextPowerS3 is particularly suited to high efficiency applications at high switching frequencies, and also safe and reliable switching at high load-current.

2. Features and benefits

- 375 Amp continuous current capability
- LPAK88 (8 x 8 mm) LPAK-style low-stress exposed lead-frame for ultimate reliability, optimum soldering and easy solder-joint inspection
- Copper-clip and solder die attach for low package inductance and resistance, and high I_D (max) rating
- Ideal replacement for D2PAK and 10 x 12 mm leadless package types
- Qualified to 175 °C
- Meets UL2595 requirements for creepage and clearance
- Avalanche rated, 100 % tested
- Low Q_G , Q_{GD} and Q_{OSS} for high efficiency, especially at higher switching frequencies
- Superfast switching with soft body-diode recovery for low-spiking and ringing, recommended for low EMI designs
- Unique "SchottkyPlus" technology for Schottky-like switching performance and low I_{DSS} leakage
- Narrow $V_{GS(th)}$ rating for easy paralleling and improved current sharing
- Very strong linear-mode / safe operating area characteristics for safe and reliable switching at high-current conditions

3. Applications

- Brushless DC motor control
- Synchronous rectifier in high-power AC-DC applications, e.g. server power supplies
- Battery protection
- eFuse and load switch
- Hotswap / in-rush current management

4. Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|-----------|-------------------------|---|-----|-----|-----|-----|------|
| V_{DS} | drain-source voltage | $25\text{ °C} \leq T_j \leq 175\text{ °C}$ | | - | - | 40 | V |
| I_D | drain current | $V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2 | [1] | - | - | 375 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; Fig. 1 | | - | - | 375 | W |

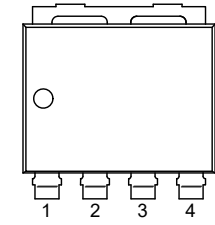
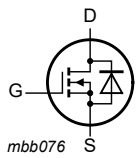
N-channel 40 V, 0.9 mΩ, 375 Amps continuous, standard level MOSFET in LPAK88 using NextPowerS3 Technology

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---|--|------|------|-----|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | - | 0.35 | 0.4 | K/W |
| Static characteristics | | | | | | |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11 | 0.51 | 0.73 | 0.9 | mΩ |
| Dynamic characteristics | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 25\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 13 ; Fig. 14 | - | 118 | 166 | nC |
| Q_{GD} | gate-drain charge | | - | 20 | 40 | nC |
| Source-drain diode | | | | | | |
| Q_r | recovered charge | $I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; [2] ; $V_{DS} = 20\text{ V}$; Fig. 17 | - | 60 | - | nC |

- [1] 375A. Continuous current has been successfully demonstrated during application. Practically, the current will be limited by the PCB, thermal design and operating temperature.
 [2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------------------------|--|--|
| 1 | G | gate |  <p>LPAK88 (SOT1235)</p> |  <p>mbb076</p> |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | S | source | | |
| mb | D | mounting base; connected to drain | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|---------------|---------|--|---------|
| | Name | Description | Version |
| PSMNR90-40SSH | LPAK88 | plastic, single-ended surface-mounted package (LPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body | SOT1235 |

7. Limiting values

Table 4. Limiting values

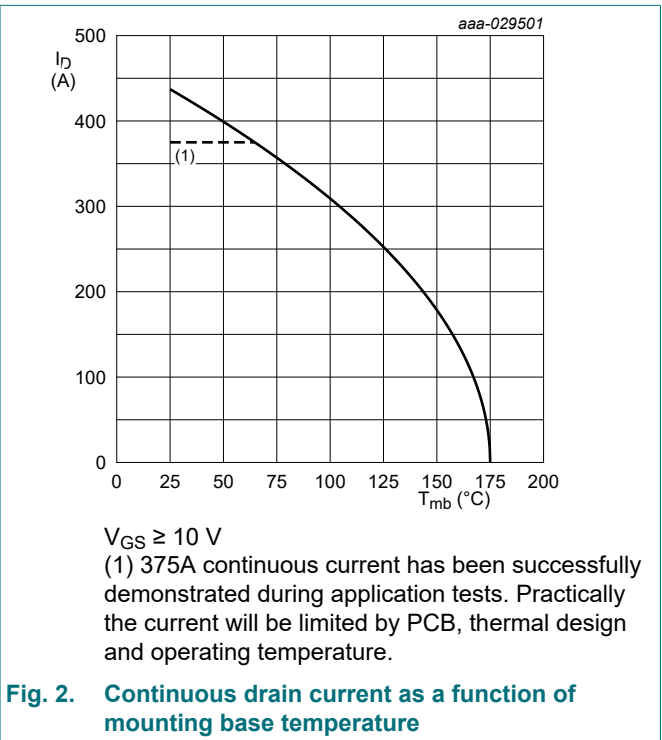
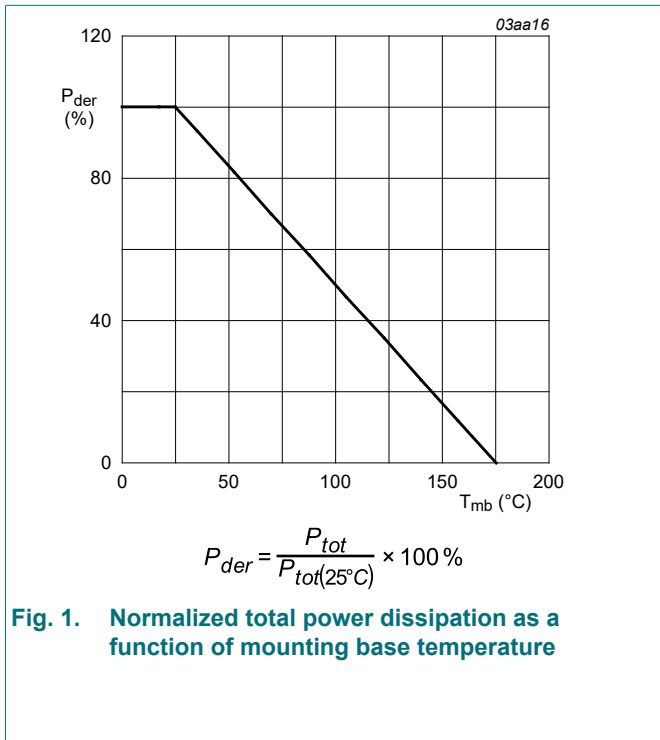
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|---------------------------|--|-----|-----|------|
| V_{DS} | drain-source voltage | $25\text{ °C} \leq T_j \leq 175\text{ °C}$ | - | 40 | V |
| V_{DSM} | peak drain-source voltage | $t_p \leq 20\text{ ns}$; $f \leq 500\text{ kHz}$; $E_{DS(AL)} \leq 200\text{ nJ}$; pulsed | - | 45 | V |
| V_{DGR} | drain-gate voltage | $25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$ | - | 40 | V |
| V_{GS} | gate-source voltage | | -20 | 20 | V |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; Fig. 1 | - | 375 | W |

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| Symbol | Parameter | Conditions | | Min | Max | Unit |
|-----------------------------|--|--|-----|-----|------|------|
| I _D | drain current | V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2 | [1] | - | 375 | A |
| | | V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2 | | - | 309 | A |
| I _{DM} | peak drain current | pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3 | | - | 1749 | A |
| T _{stg} | storage temperature | | | -55 | 175 | °C |
| T _j | junction temperature | | | -55 | 175 | °C |
| T _{slid(M)} | peak soldering temperature | | | - | 260 | °C |
| Source-drain diode | | | | | | |
| I _S | source current | T _{mb} = 25 °C | [2] | - | 500 | A |
| I _{SM} | peak source current | pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C | | - | 1749 | A |
| Avalanche ruggedness | | | | | | |
| E _{DS(AL)S} | non-repetitive drain-source avalanche energy | I _D = 120 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; Fig. 4 | | - | 631 | mJ |
| I _{AS} | non-repetitive avalanche current | V _{sup} = 40 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω | [3] | - | 247 | A |

- [1] 375A. Continuous current has been successfully demonstrated during application. Practically, the current will be limited by the PCB, thermal design and operating temperature.
- [2] 500A. Continuous current has been successfully demonstrated during application. Practically, the current will be limited by the PCB, thermal design and operating temperature.
- [3] Protected by 100% test



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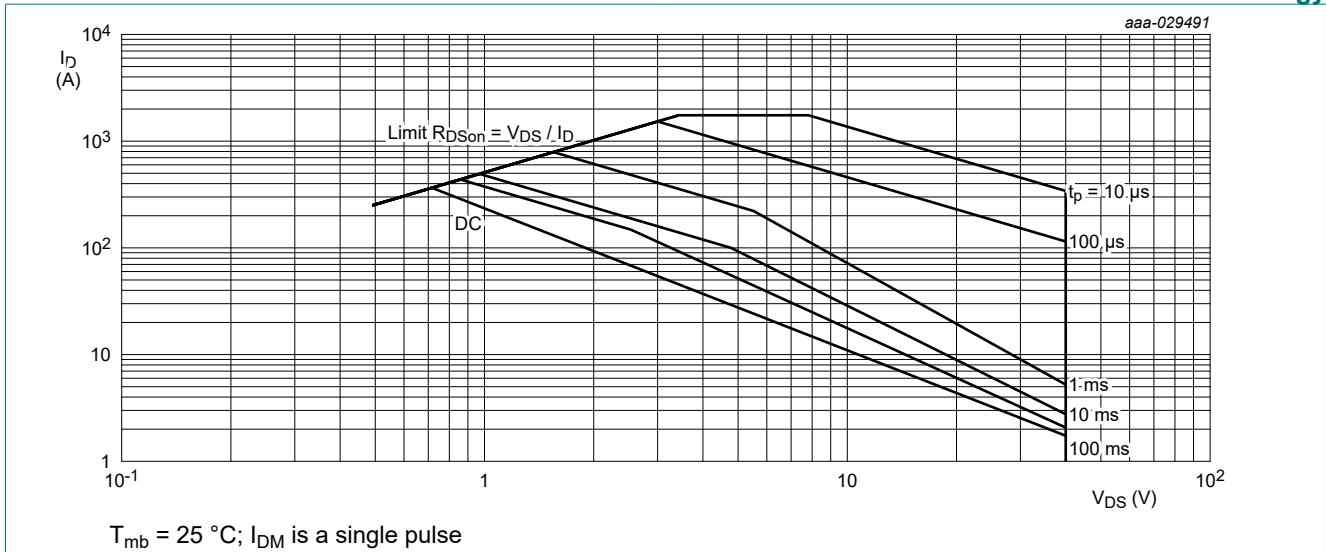


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

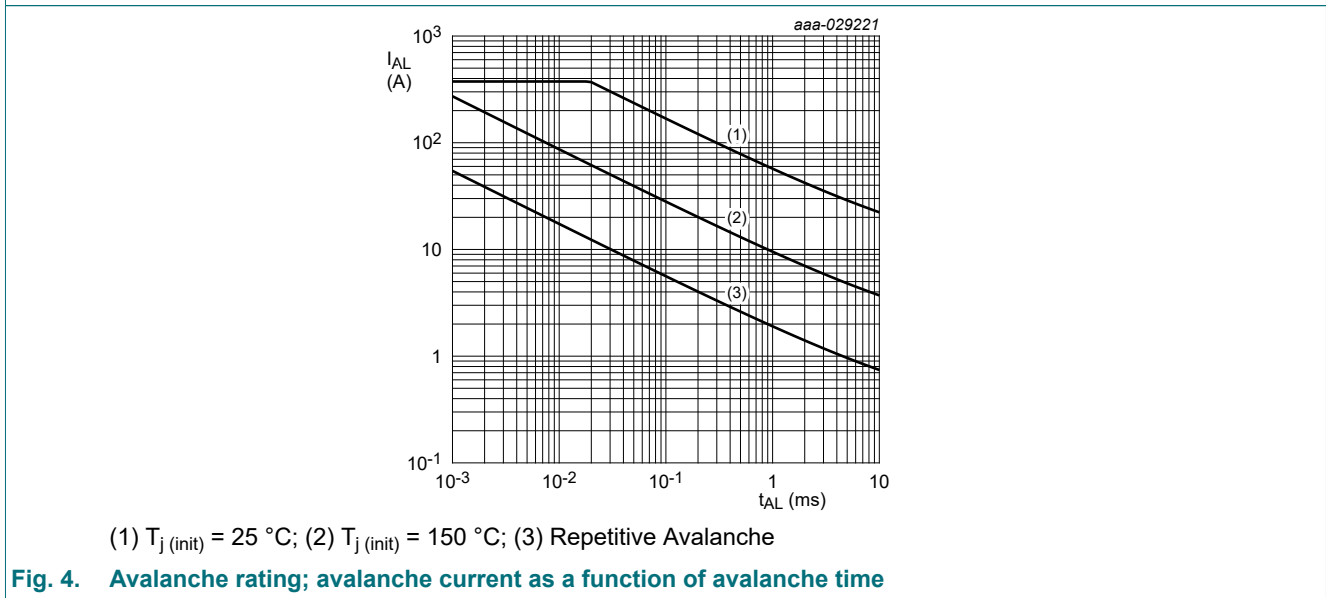


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

8. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|------------------------|-----|------|-----|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | - | 0.35 | 0.4 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Fig. 6 | - | 35 | - | K/W |
| | | Fig. 7 | - | 70 | - | K/W |

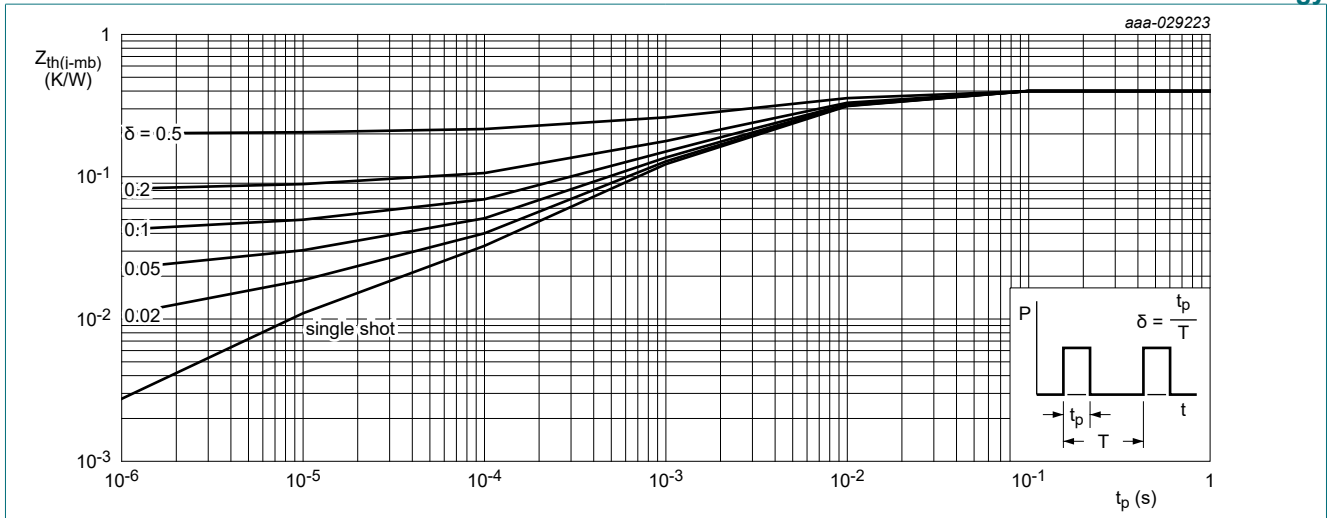


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

aaa-029383

Copper square 25.4 mm x 25.4 mm; 70 μm thick on FR4 board

aaa-029384

70 μm thick copper on FR4 board

Fig. 6. PCB layout for resistance from junction to ambient

Fig. 7. PCB layout with minimum footprint for thermal resistance from junction to ambient

9. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--|--|------|------|-----|---------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | 40 | 43 | - | V |
| | | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$ | 36 | 40 | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ | 2.4 | 3 | 3.6 | V |
| $\Delta V_{GS(th)}/\Delta T$ | gate-source threshold voltage variation with temperature | $25 \text{ }^\circ C \leq T_j \leq 175 \text{ }^\circ C$ | - | -8.1 | - | mV/K |
| I_{DSS} | drain leakage current | $V_{DS} = 32 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | - | 1.2 | μA |
| | | $V_{DS} = 32 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$ | - | 134 | - | μA |
| I_{GSS} | gate leakage current | $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 2 | 100 | nA |
| | | $V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 2 | 100 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 11 | 0.51 | 0.73 | 0.9 | mΩ |

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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|--------------------------------|-----------------------------------|---|-----|------|-------|------|----|
| | | $V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 175\text{ °C}$; Fig. 12 | 1 | 1.5 | 1.96 | mΩ | |
| R_G | gate resistance | $f = 1\text{ MHz}$; $T_j = 25\text{ °C}$ | 0.4 | 1 | 2.5 | Ω | |
| Dynamic characteristics | | | | | | | |
| $Q_{G(\text{tot})}$ | total gate charge | $I_D = 25\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 13 ; Fig. 14 | - | 118 | 166 | nC | |
| | | $I_D = 0\text{ A}$; $V_{DS} = 0\text{ V}$; $V_{GS} = 10\text{ V}$ | - | 58 | - | nC | |
| Q_{GS} | gate-source charge | $I_D = 25\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 13 ; Fig. 14 | - | 34 | 52 | nC | |
| $Q_{GS(\text{th})}$ | pre-threshold gate-source charge | | - | 24 | 35 | nC | |
| $Q_{GS(\text{th-pl})}$ | post-threshold gate-source charge | | - | 11 | 17 | nC | |
| Q_{GD} | gate-drain charge | | - | 20 | 40 | nC | |
| $V_{GS(\text{pl})}$ | gate-source plateau voltage | $I_D = 25\text{ A}$; $V_{DS} = 32\text{ V}$; Fig. 13 ; Fig. 14 | - | 4.3 | - | V | |
| C_{iss} | input capacitance | $V_{DS} = 25\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ °C}$; Fig. 15 | - | 9206 | 12888 | pF | |
| C_{oss} | output capacitance | | - | 1908 | 2671 | pF | |
| C_{rss} | reverse transfer capacitance | | - | 344 | 757 | pF | |
| $t_{d(\text{on})}$ | turn-on delay time | $V_{DS} = 30\text{ V}$; $R_L = 1.2\text{ Ω}$; $V_{GS} = 10\text{ V}$; $R_{G(\text{ext})} = 5\text{ Ω}$ | - | 30 | - | ns | |
| t_r | rise time | | - | 24 | - | ns | |
| $t_{d(\text{off})}$ | turn-off delay time | | - | 72 | - | ns | |
| t_f | fall time | | - | 31 | - | ns | |
| Q_{oss} | output charge | $V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ °C}$ | - | 82 | - | nC | |
| Source-drain diode | | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; Fig. 16 | - | 0.76 | 1 | V | |
| t_{rr} | reverse recovery time | $I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; Fig. 17 | - | 48 | - | ns | |
| Q_r | recovered charge | | [1] | - | 60 | - | nC |
| t_a | reverse recovery rise time | | - | - | 27 | - | ns |
| t_b | reverse recovery fall time | | - | - | 21 | - | ns |

[1] includes capacitive recovery

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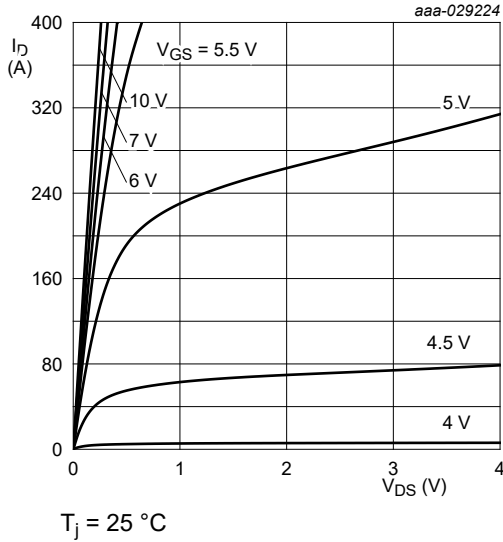


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

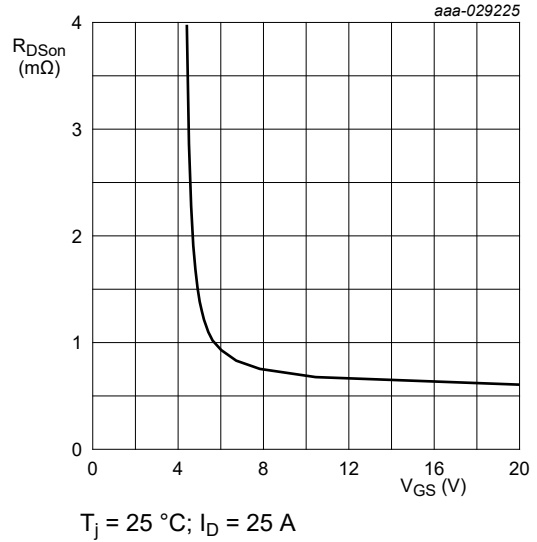


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

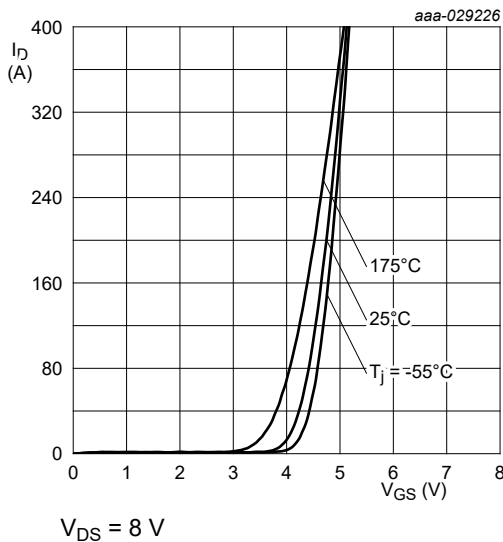


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

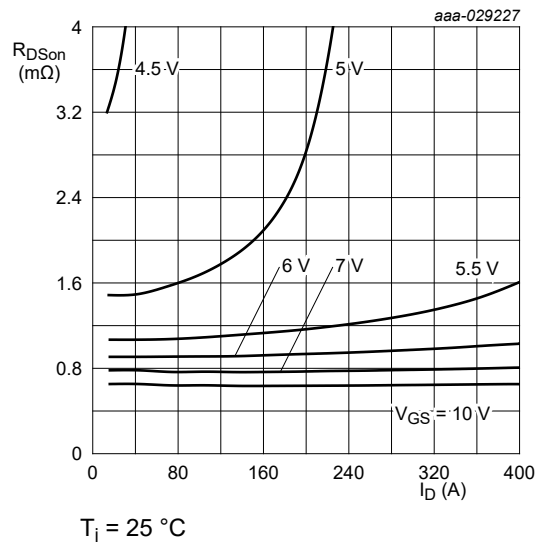
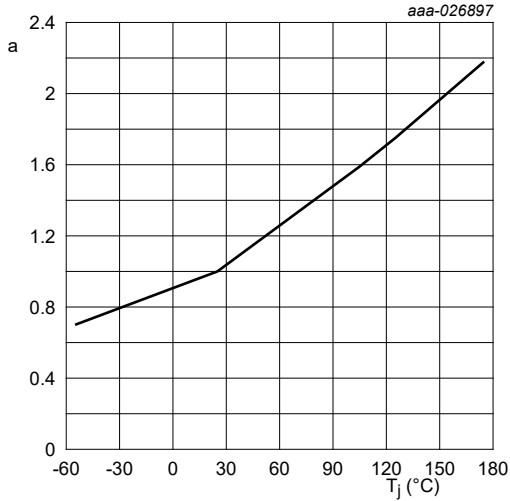


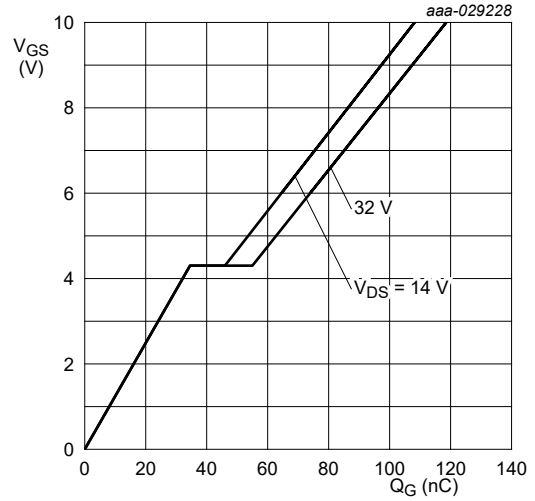
Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

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$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^{\circ}\text{C}; I_D = 25\text{ A}$

Fig. 13. Gate-source voltage as a function of gate charge; typical values

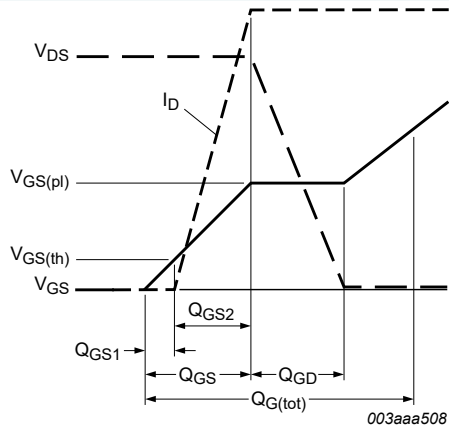
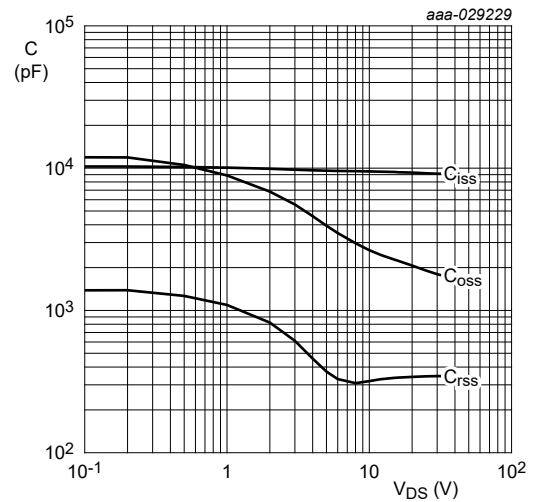


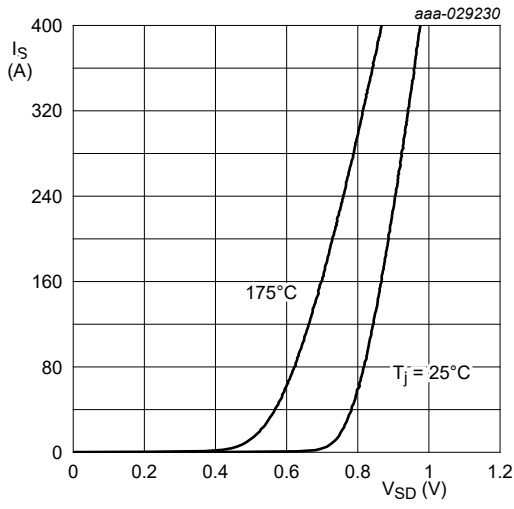
Fig. 14. Gate charge waveform definitions



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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$V_{GS} = 0$ V

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

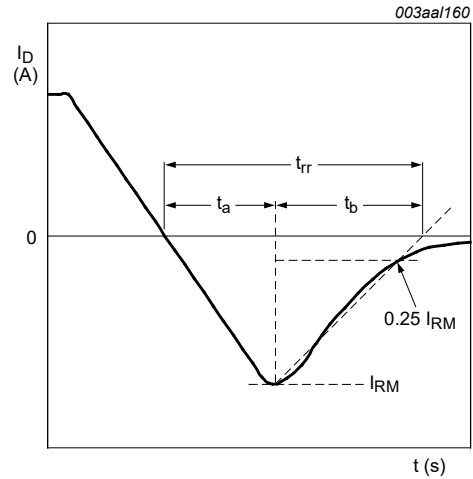


Fig. 17. Reverse recovery timing definition

10. Package outline

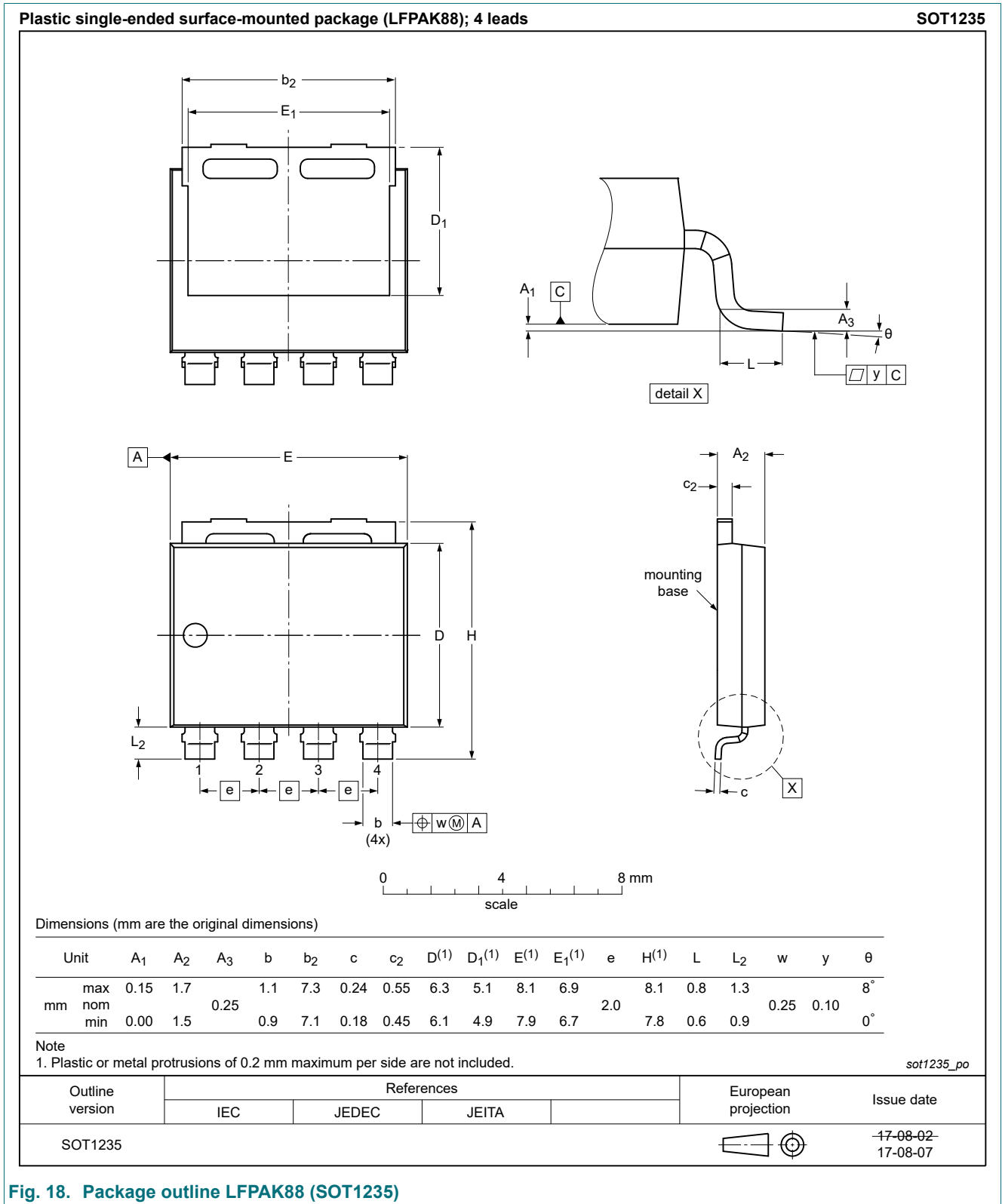


Fig. 18. Package outline LPAK88 (SOT1235)

11. Soldering

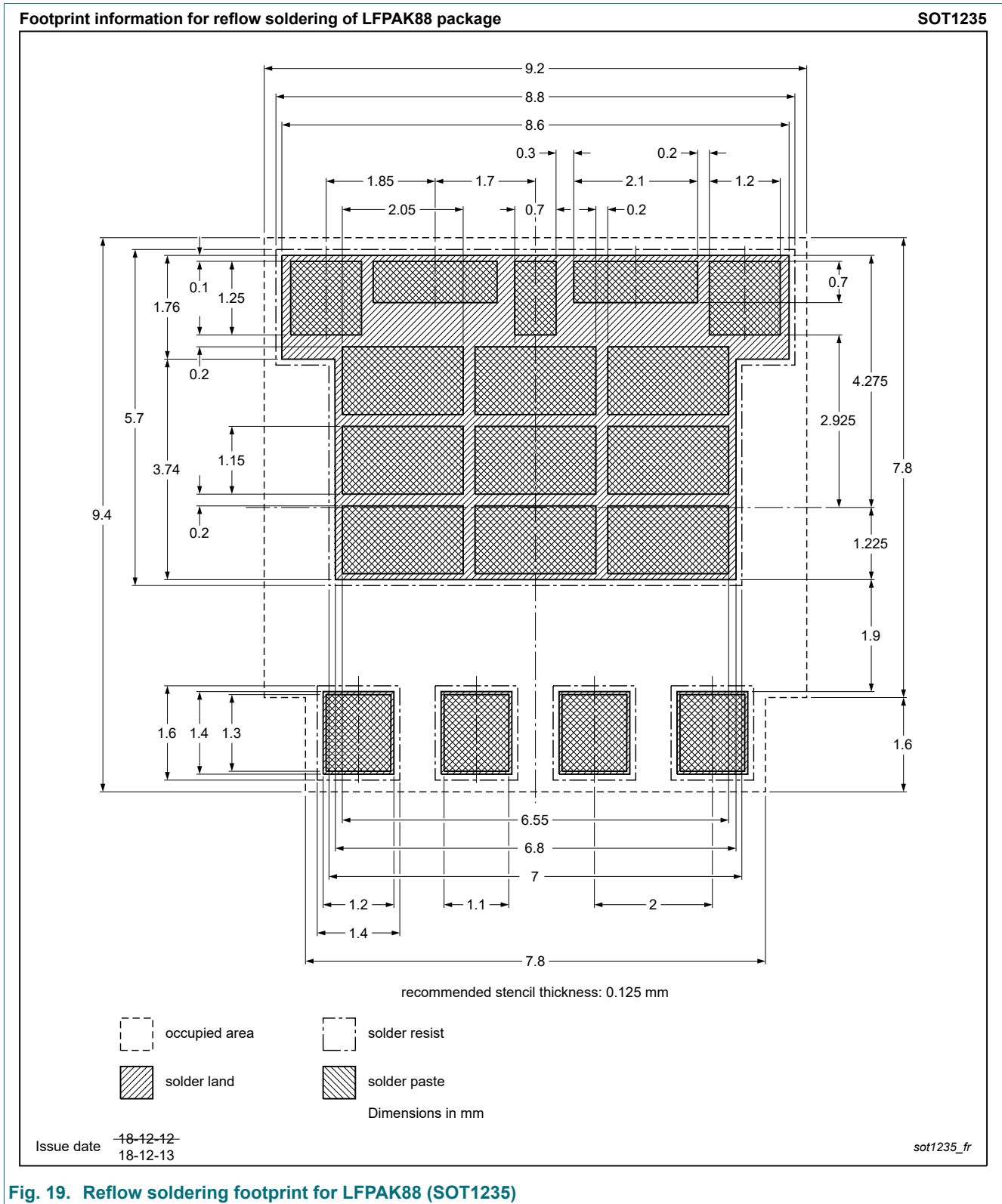


Fig. 19. Reflow soldering footprint for LPAK88 (SOT1235)

N-channel 40 V, 0.9 mΩ, 375 Amps continuous, standard level MOSFET in LPAK88 using NextPowerS3 Technology

12. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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- [2] The term 'short data sheet' is explained in section "Definitions".
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