



PSMNR90-40YLH

N-channel 40 V, 0.94 mΩ, 300 A logic level MOSFET in LPAK56E using NextPower-S3 Schottky-Plus technology

26 April 2019

Product data sheet

1. General description

300 Amp, logic level gate drive N-channel enhancement mode MOSFET in 175 °C LPAK56E package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high performance power switching applications.

2. Features and benefits

- 300 A continuous $I_{D(max)}$
- Avalanche rated, 100% tested
- NextPower-S3 technology delivers 'superfast switching with soft body-diode recovery'
- Low Q_{RR} , Q_G and Q_{GD} for high system efficiency and low EMI designs
- Schottky-Plus body-diode, gives soft switching without the associated high I_{DSS} leakage
- Strong linear-mode / SOA rating
- Optimised for 4.5 V gate drive utilising NextPower-S3 Superjunction technology
- High reliability LPAK (Power SO8) package, with copper-clip and solder die attach, qualified to 175 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints for ultimate reliability
- Low parasitic inductance and resistance

3. Applications

- High-performance synchronous rectification
- DC-to-DC converters
- High performance and high efficiency server power supply
- Brushless DC motor control
- Battery protection
- Load-switch and eFuse

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	40	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	-	300	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	333	W
T _j	junction temperature			-55	-	175	°C
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C; Fig. 10		-	0.97	1.2	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 10		-	0.76	0.94	mΩ
Dynamic characteristics							

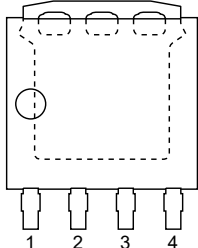
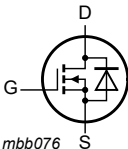
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 20\text{ V}$; $V_{GS} = 4.5\text{ V}$; Fig. 12 ; Fig. 13	-	13	26	nC
$Q_{G(tot)}$	total gate charge		-	54	76	nC

[1] 300A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56E; Power-SO8 (SOT1023)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMNR90-40YLH	LPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LPAK56); 4 leads; 1.27 mm pitch	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMNR90-40YLH	H90L40J

8. Limiting values

Table 5. Limiting values

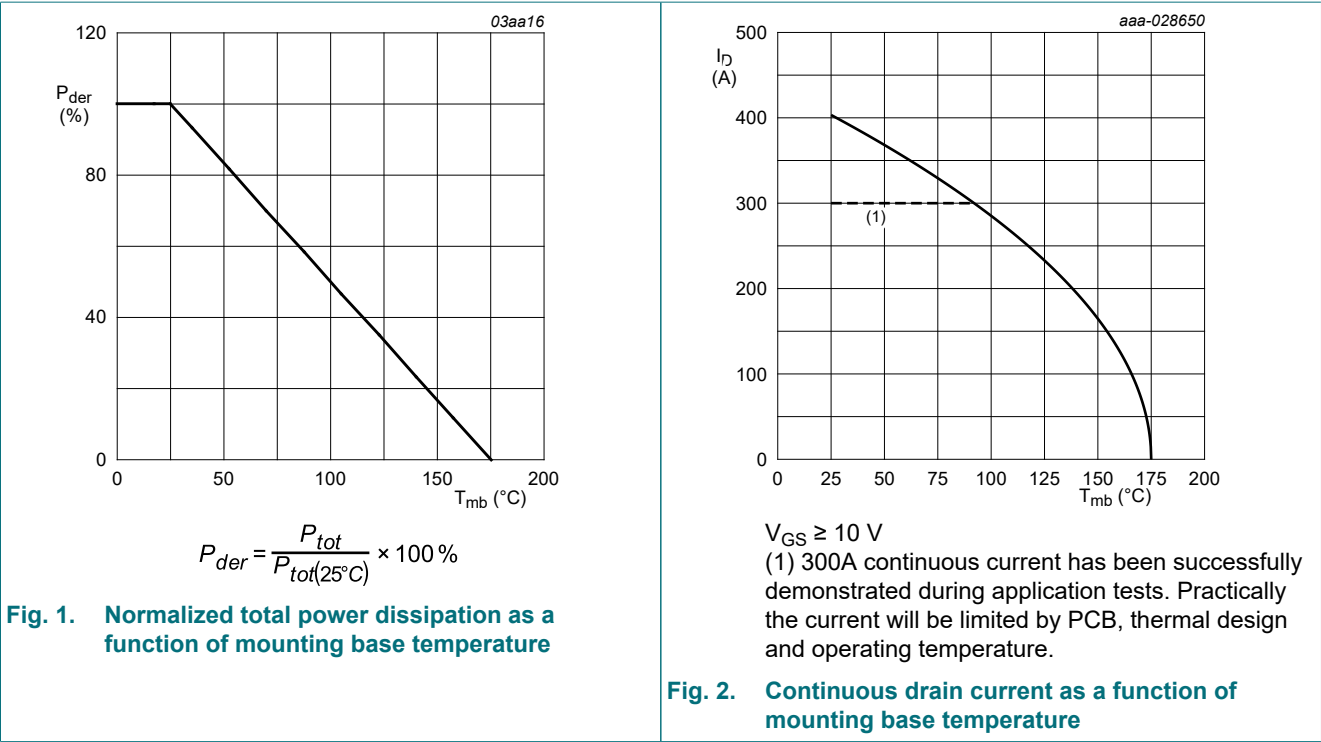
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	40	V
V_{DSM}	peak drain-source voltage	$t_p \leq 20\text{ ns}$; $f \leq 500\text{ kHz}$; $E_{DS(AL)} \leq 200\text{ nJ}$; pulsed	-	45	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	40	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	333	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	300	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	-	285	A

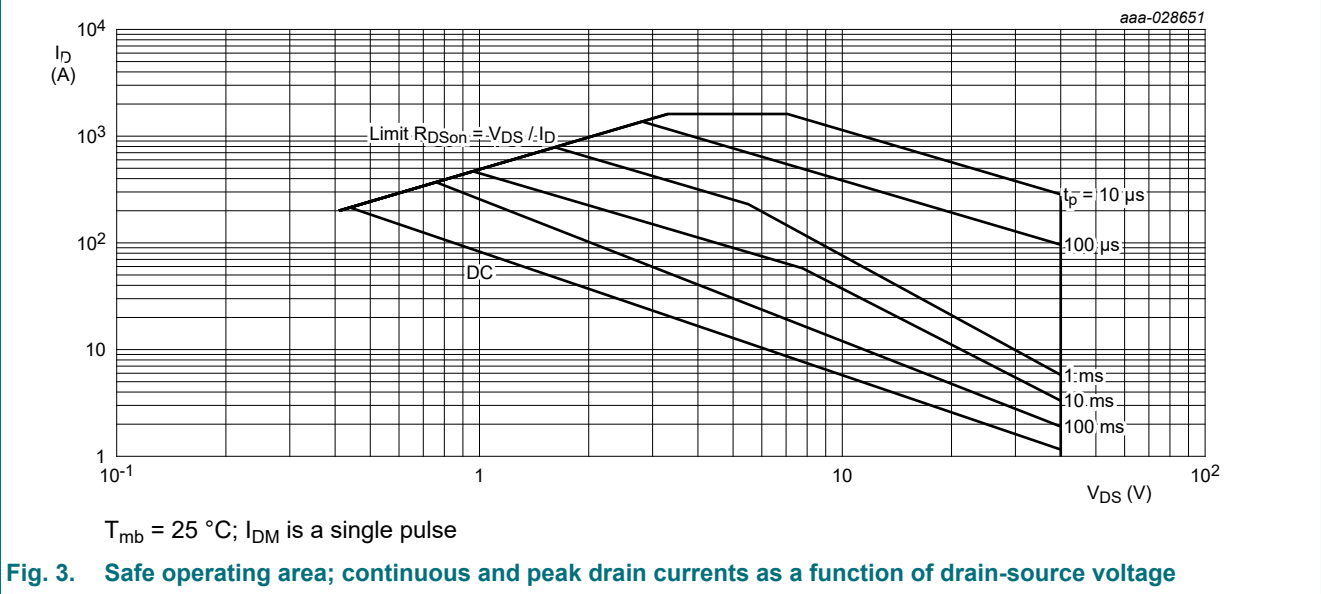
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Symbol	Parameter	Conditions		Min	Max	Unit
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	1613	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	278	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	1613	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 83 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 0.27 ms	[2]	-	577	mJ
		I _D = 25 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 4.1 ms	[2]	-	2706	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 40 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω	[2]	-	190	A

- [1] 300A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test



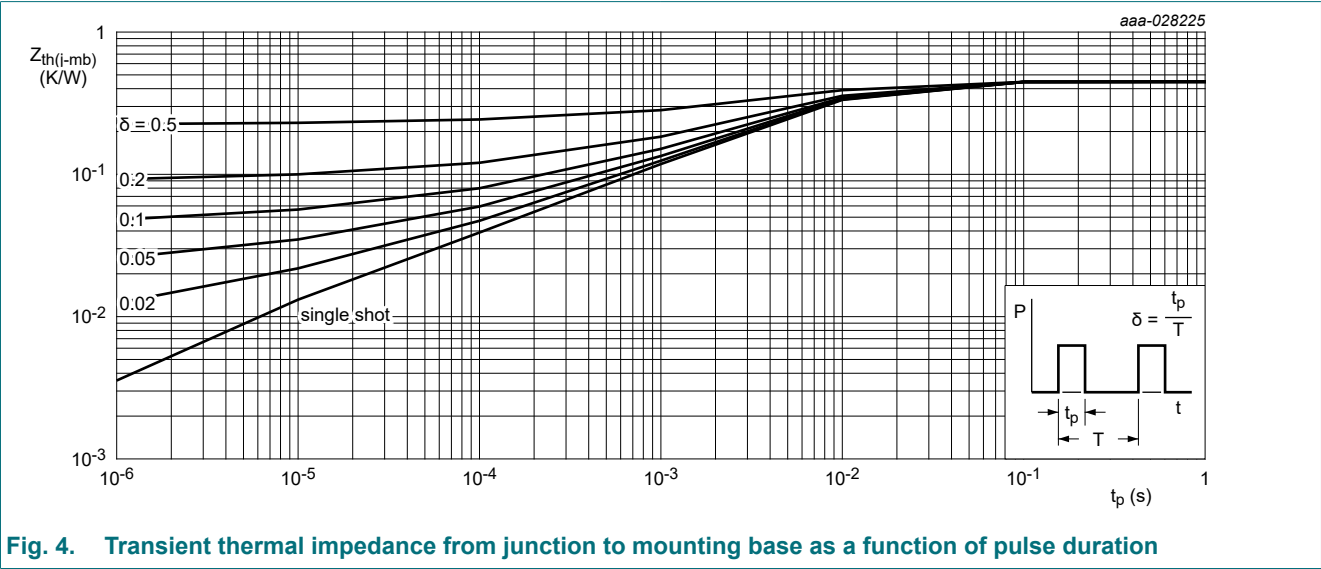
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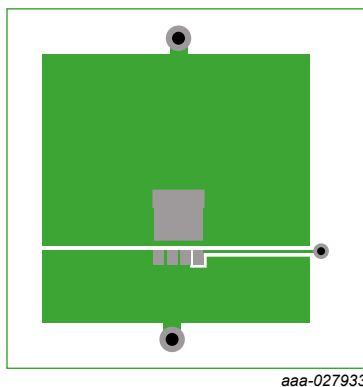
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.33	0.45	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	42	-	K/W
		Fig. 6	-	85	-	K/W

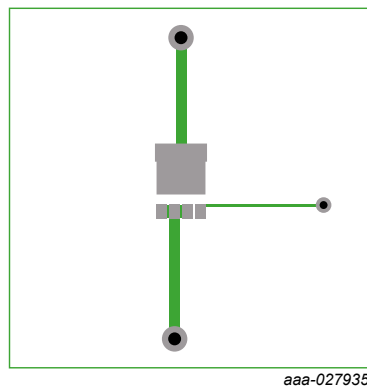


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Copper square 25.4 mm x 25.4 mm; 70 μm thick on FR4 board

Fig. 5. PCB layout for thermal resistance from junction to ambient



70 μm thick copper on FR4 board

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics

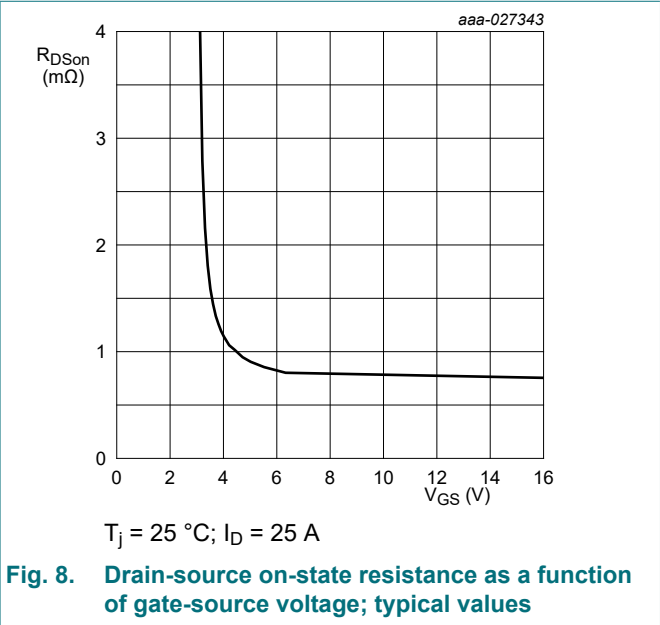
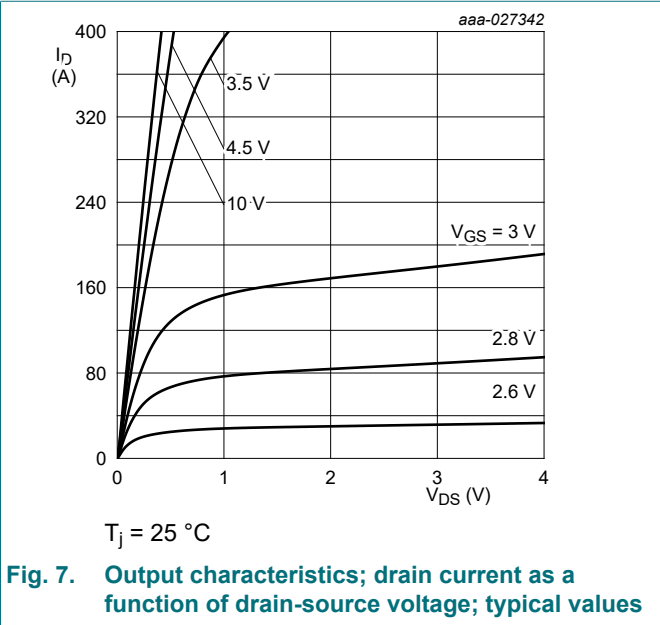
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55^\circ C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25^\circ C$	1.35	1.7	2.05	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25^\circ C \leq T_j \leq 150^\circ C$	-	-4.9	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 32 V; V_{GS} = 0 V; T_j = 25^\circ C$	-	-	1	μA
		$V_{DS} = 32 V; V_{GS} = 0 V; T_j = 125^\circ C$	-	11	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25^\circ C$	-	2	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_j = 25^\circ C$; Fig. 10	-	0.76	0.94	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_j = 175^\circ C$; Fig. 11	-	-	2	mΩ
		$V_{GS} = 4.5 V; I_D = 25 A; T_j = 25^\circ C$; Fig. 10	-	0.97	1.2	mΩ
		$V_{GS} = 4.5 V; I_D = 25 A; T_j = 175^\circ C$; Fig. 11	-	-	2.6	mΩ
R_G	gate resistance	$f = 1 MHz; T_j = 25^\circ C$	0.4	1	2.6	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A; V_{DS} = 20 V; V_{GS} = 4.5 V$; Fig. 12 ; Fig. 13	-	54	76	nC
		$I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V$; Fig. 12 ; Fig. 13	-	120	168	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	63	-	nC
Q_{GS}	gate-source charge	$I_D = 25 A; V_{DS} = 20 V; V_{GS} = 4.5 V$; Fig. 12 ; Fig. 13	-	20	30	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	12	18	nC

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	8	12	nC
Q_{GD}	gate-drain charge			-	13	26	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}$; $V_{DS} = 20\text{ V}$; Fig. 12 ; Fig. 13		-	2.7	-	V
C_{iss}	input capacitance	$V_{DS} = 20\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ °C}$; Fig. 14		-	9052	12673	pF
C_{oss}	output capacitance			-	1702	2383	pF
C_{rss}	reverse transfer capacitance			-	347	764	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20\text{ V}$; $R_L = 0.8\text{ }\Omega$; $V_{GS} = 4.5\text{ V}$; $R_{G(ext)} = 5\text{ }\Omega$		-	45	-	ns
t_r	rise time			-	46	-	ns
$t_{d(off)}$	turn-off delay time			-	59	-	ns
t_f	fall time			-	33	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ °C}$		-	57	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; Fig. 15		-	0.76	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; Fig. 16		-	45	-	ns
Q_r	recovered charge		[1]	-	53	-	nC
t_a	reverse recovery rise time			-	25	-	ns
t_b	reverse recovery fall time			-	19	-	ns

[1] includes capacitive recovery



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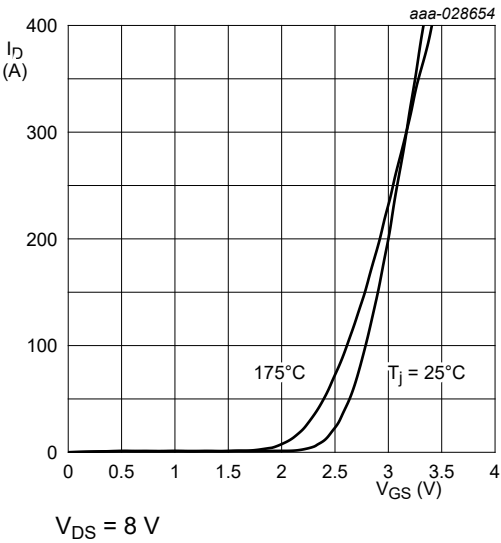


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

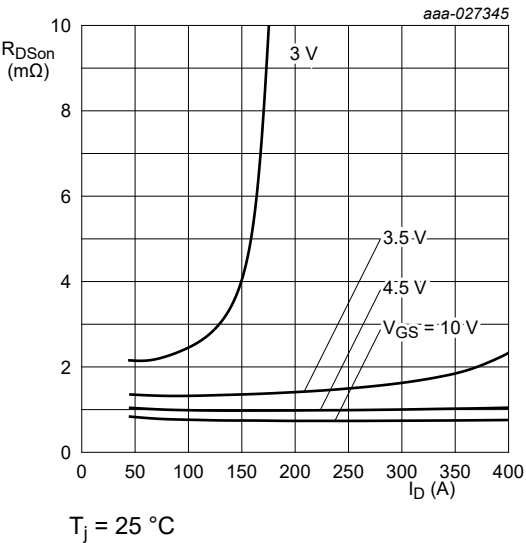


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

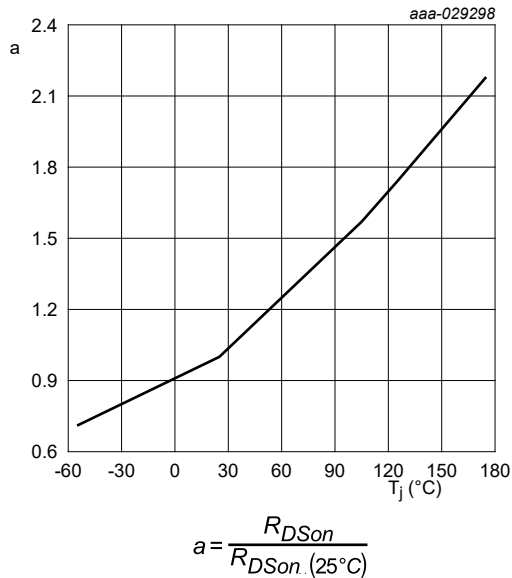


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

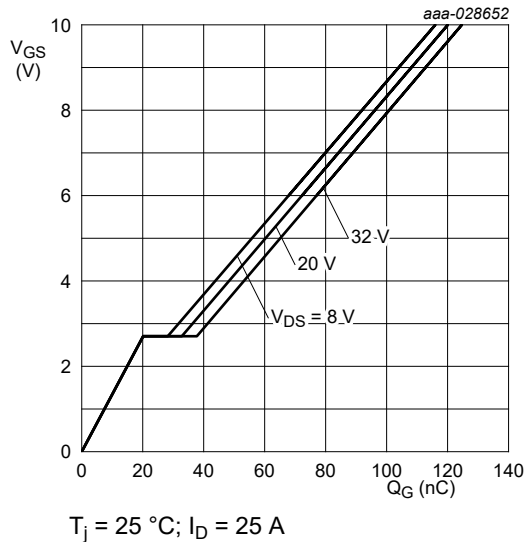
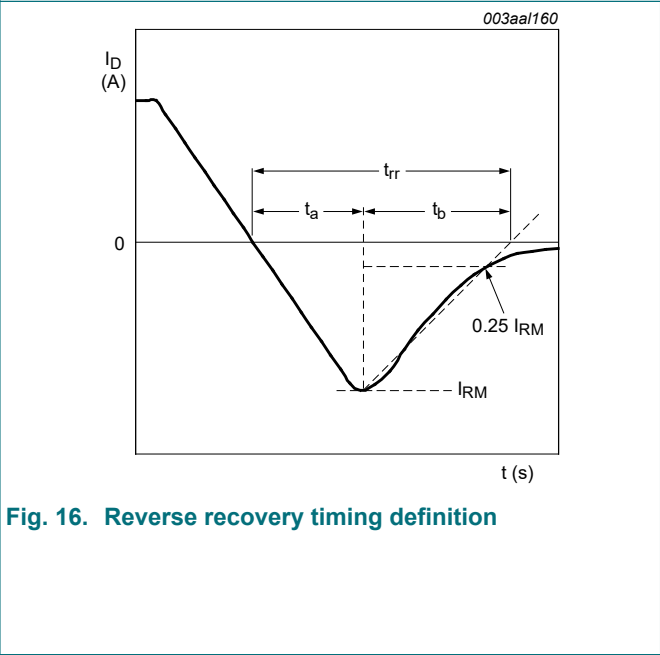
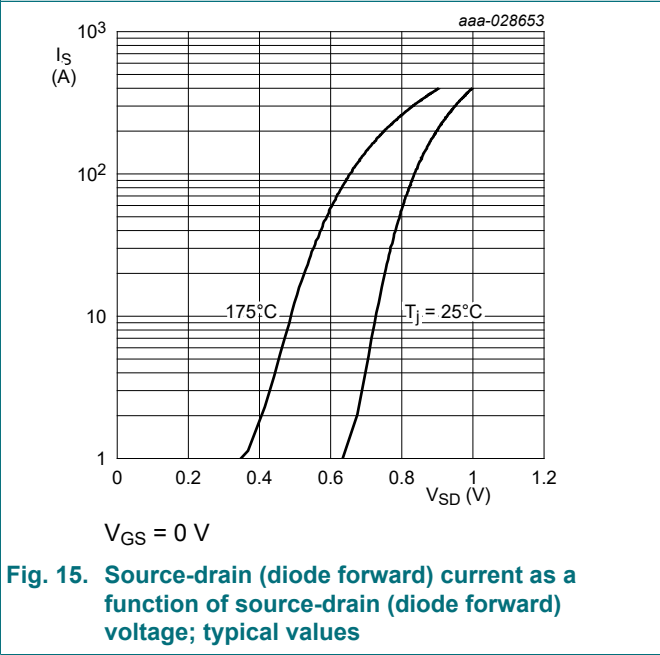
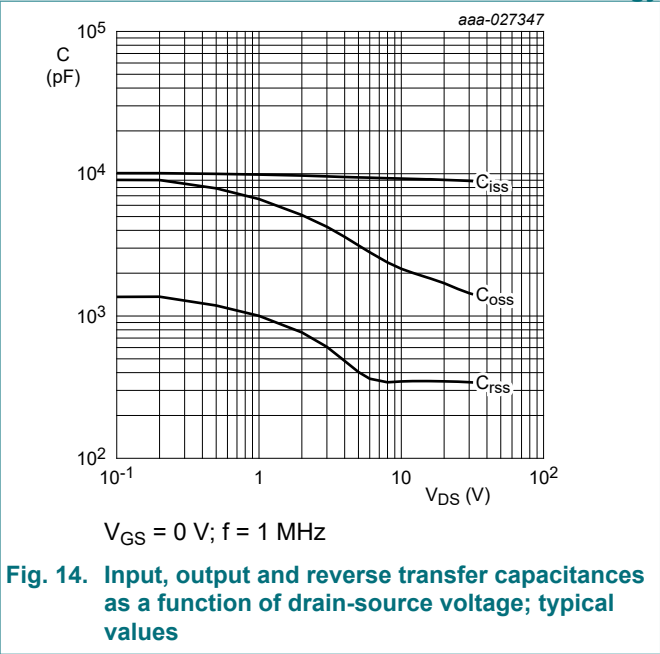
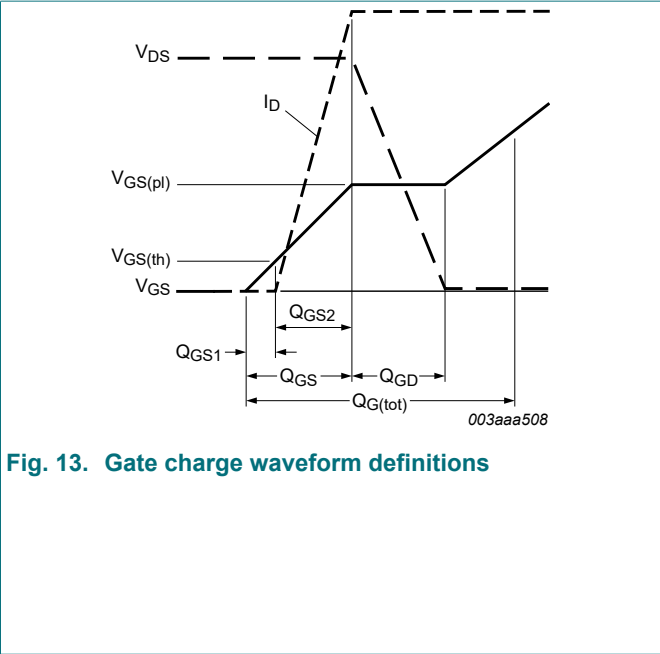


Fig. 12. Gate-source voltage as a function of gate charge; typical values

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11. Package outline

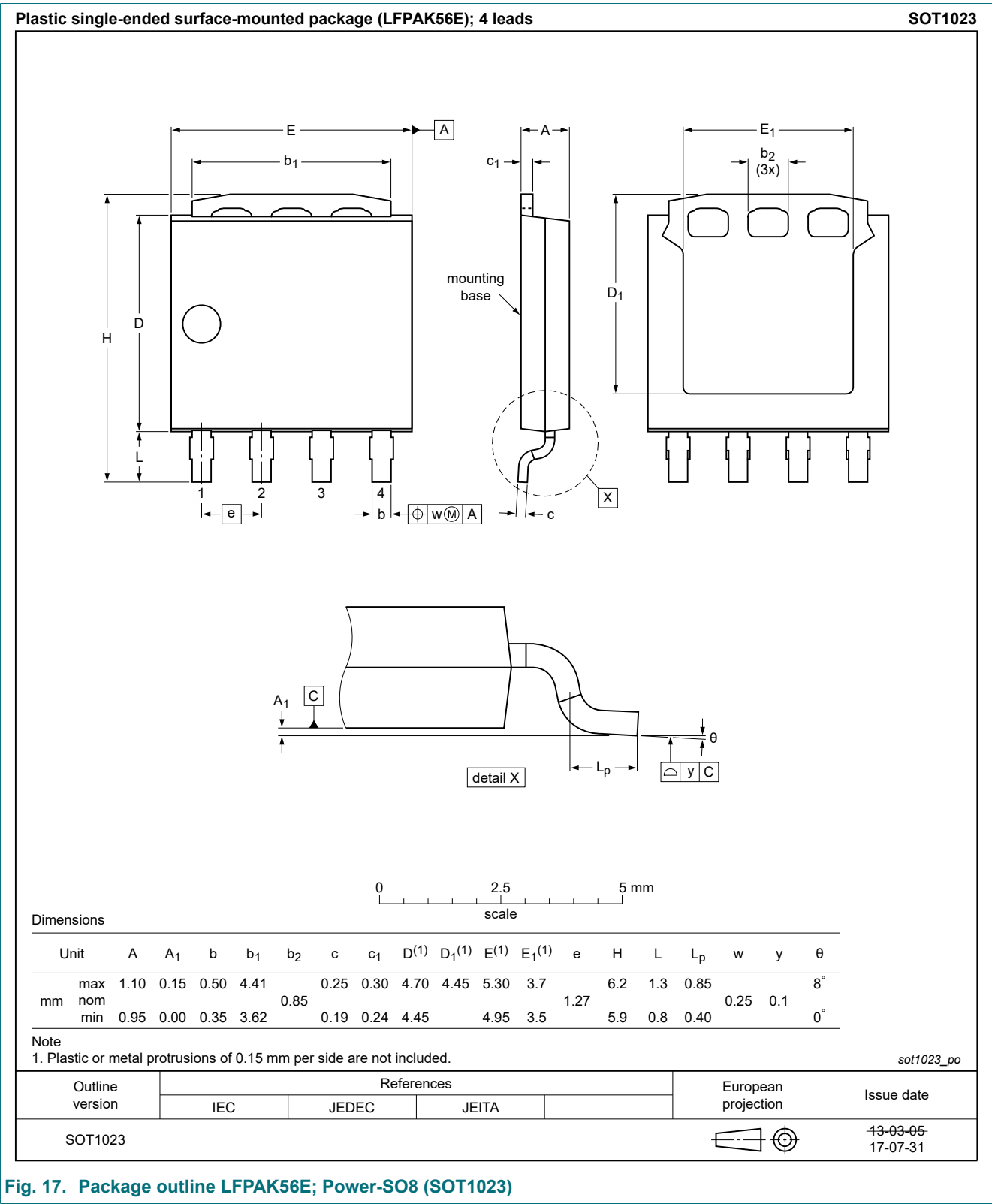


Fig. 17. Package outline LPAK56E; Power-SO8 (SOT1023)

12. Soldering

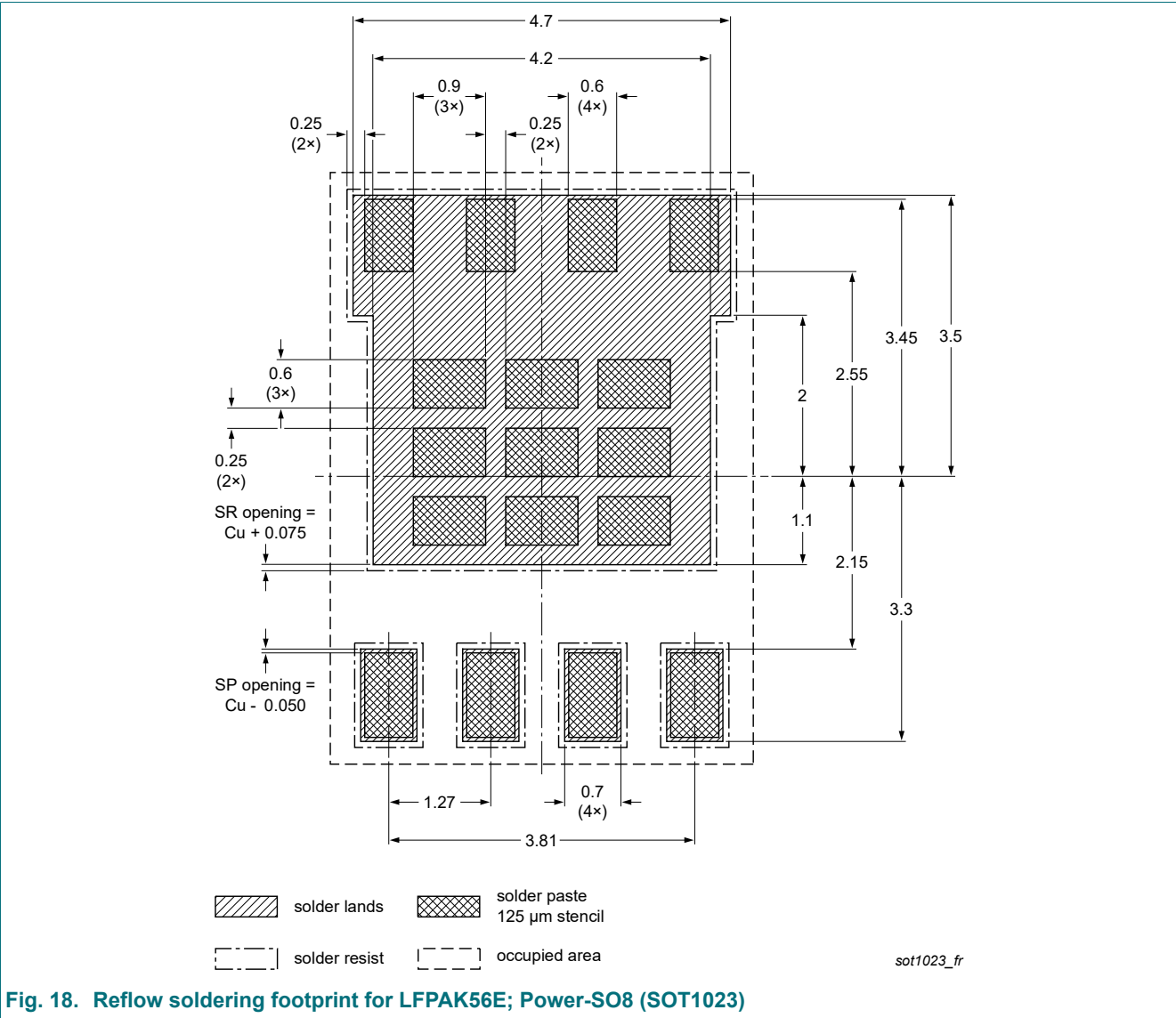


Fig. 18. Reflow soldering footprint for LPAK56E; Power-SO8 (SOT1023)

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13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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