

RCIamp0582BQ Low Capacitance TVS for Automotive Applications

PROTECTION PRODUCTS - RailClamp®

Description

The RClamp®0582BQ transient voltage suppressor is specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD (electrostatic discharge), CDE (cable discharge events), and EFT (electrical fast transients). It is rated to Grade 2 of AEC-Q100 for use in automotive applications.

The RClamp®0582BQ features high peak pulse current capability (Ipp=15A, tp=8/20us) for use in applications that require high surge immunity testing. It has a maximum capacitance of only 1.2pF (pin 1 or 2 to pin3). They may be used to meet the ESD immunity requirements of IEC 61000-4-2 (±30kV air, ±25kV contact discharge). Each device can be configured to protect 1 bidirectional line or two unidirectional lines.

These devices are in a small SC-75 (SOT-523) package and feature a lead-free, matte tin finish. They are compatible with both lead free and SnPb assembly techniques. The combination of small size, low capacitance, and high level of surge protection makes them a flexible solution for protection of USB 2.0, LVDS, and video interfaces.

Features

- ◆ Transient protection for high-speed data lines to IEC 61000-4-2 (ESD) ±30kV (air), ±25kV (contact) IEC 61000-4-4 (EFT) 40A (5/50ns)
- Qualified to AEC-Q100, Grade 2
- Protects up to two I/O lines
- ◆ Low capacitance (<1.2pF)
- ♦ High surge capability: 15A (tp=8/20us)
- Low leakage current and clamping voltage
- Low operating voltage: 5.0V
- Solid-state silicon-avalanche technology

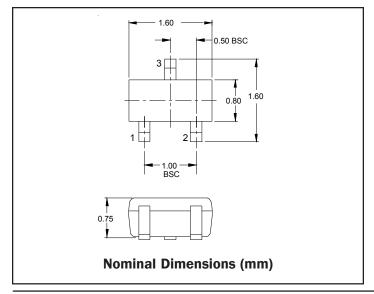
Mechanical Characteristics

- ◆ SC-75 (SOT-523) package
- ◆ Lead Finish: Matte Tin
- ◆ Pb-Free, Halogen Free, RoHS/WEEE Compliant
- ◆ Molding compound flammability rating: UL 94V-0
- Packaging: Tape and Reel

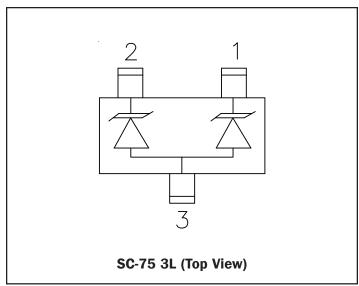
Applications

- ◆ USB 2.0
- Video Lines
- LVDS Lines

Dimensions



Schematic & PIN Configuration





Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P _{pk}	300	Watts
Peak Pulse Current (tp = 8/20µs)	I _{PP}	15	А
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V _{ESD}	30 25	kV
Operating Temperature	T _J	-40 to +105	°C
Storage Temperature	T _{STG}	-55 to +150	°C

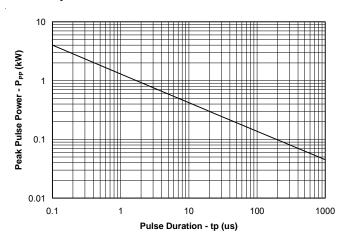
Electrical Characteristics (T=25°C)

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Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V _{RWM}	Pin 1 or Pin 2 to Pin 3			5	V
Reverse Breakdown Voltage	V _{BR}	I _t = 1mA Pin 1 or Pin 2 to Pin 3	6		11	V
Reverse Leakage Current	I _R	V _{RWM} = 5V, T=25°C Pin 1 or Pin 2 to Pin 3 and Between Pins 1 and 2			0.100	μА
Reverse Leakage Current	I _R	V _{RWM} = 5V, T=105°C Pin 1 or Pin 2 to Pin 3 and Between Pins 1 and 2			0.300	μΑ
Clamping Voltage	V _c	I _{PP} = 5A, tp = 8/20μs Pin 1 or Pin 2 to Pin 3			15	V
Clamping Voltage	V _c	I _{PP} = 15A, tp = 8/20μs Pin 1 or Pin 2 to Pin 3			20	V
Junction Capacitance	C _j	V _R = 0V, f = 1MHz Pin 1 to Pin 2		0.50	0.8	pF
Junction Capacitance	C _j	V _R = 0V, f = 1MHz Pin 1 or Pin 2 to Pin 3			1.2	pF

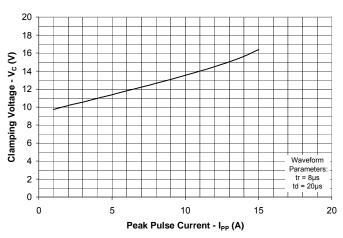


Typical Characteristics

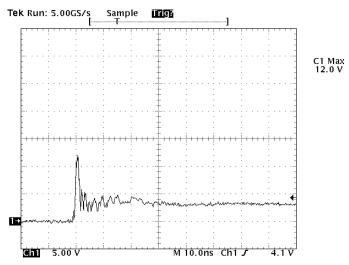
Non-Repetitive Peak Pulse Power vs. Pulse Time



Clamping Voltage vs. Peak Pulse Current Pin 1 or Pin 2 to Pin 3

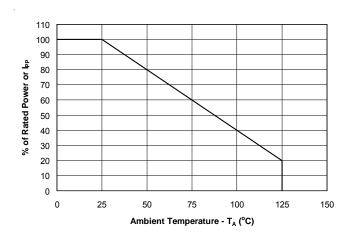


ESD Clamping - Pin 1 or Pin 2 to Pin 3 (8kV Contact per IEC 61000-4-2)

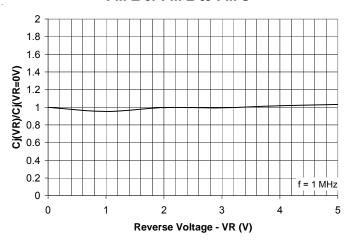


Note: Data is taken with a 10x attenuator

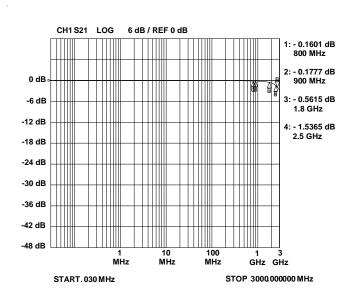
Power Derating Curve



Normalized Capacitance vs. Reverse Voltage Pin 1 or Pin 2 to Pin 3

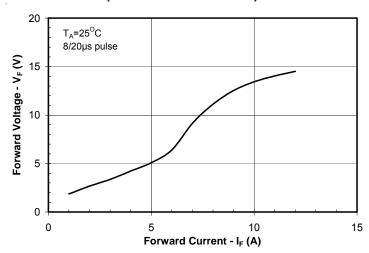


Insertion Loss S21 (Pin 1 or Pin 2 to Pin 3)

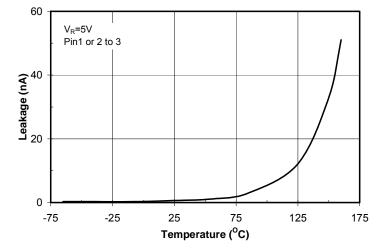




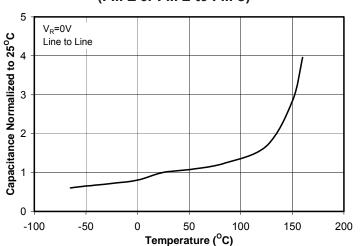
Forward Voltage vs. Forward Current (Pin 3 to Pin 1 or Pin 2)



Reverse Leakage Current vs. Temperature (Pin 1 or Pin 2 to Pin 3)



Normalized Capacitance vs. Temperature (Pin 1 or Pin 2 to Pin 3)





Applications Information

Device Connection Options

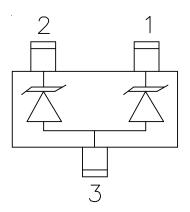
This device is optimized for protection of two high speed dta lines. The device is connected as follows:

Protection of two lines is achieved by connecting data lines at pins 1 & 2. Pin 3 is connected to ground. The connection to ground should be made directly to a ground plane. The path length should also be kept as short as possible to minimize parasitic inductance.

Matte Tin Lead Finish

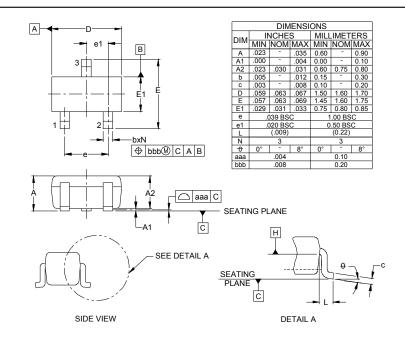
Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

Figure 1. Pin Configuration





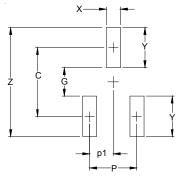
Outline Drawing -SC-75 (SOT-523)



NOTES:

- 1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
- 2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
- 3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

Land Pattern -SC-75 (SOT-523)



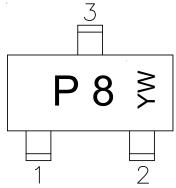
DIMENSIONS				
DIM	INCHES	MILLIMETERS		
С	(.055)	(1.40)		
Р	.039	1.00		
p1	.020	0.50		
G	.024	0.60		
Х	.016	0.40		
Υ	.031	0.80		
Z	.087	2.20		

NOTES:

THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY
CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
COMPANY'S MANUFACTURING GUIDELINES ARE MET.



Marking



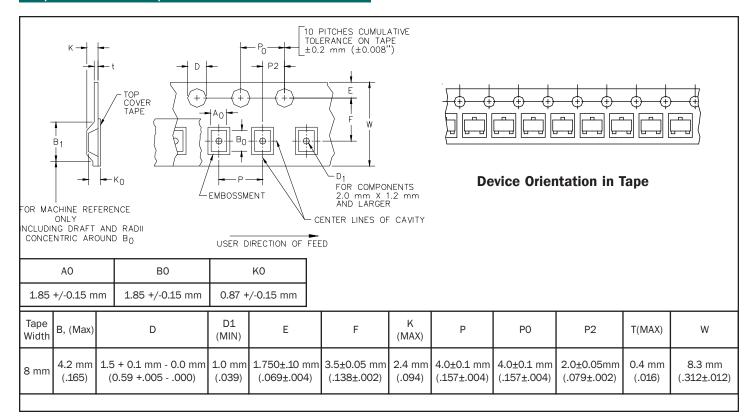
YW = Date Code

Ordering Information

Part Number	Part Number Lead Finish		Reel Size	
RClamp0582BQ.TCT	Pb Free	3,000	7 Inch	

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Tape and Reel Specification



Contact Information

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