



ON Semiconductor®

FDPC4044

Common Drain N-Channel PowerTrench® MOSFET

30 V, 27 A, 4.3 mΩ

Features

- Max $r_{S1S2(on)}$ = 4.3 mΩ at $V_{GS} = 10\text{ V}$, $I_{S1S2} = 27\text{ A}$
- Max $r_{S1S2(on)}$ = 6.4 mΩ at $V_{GS} = 4.5\text{ V}$, $I_{S1S2} = 23\text{ A}$
- Package size/height: 3.3 x 3.3 x 0.8 mm
- Low inductance packaging shortens rise/fall times, resulting in lower switching losses
- MOSFET integration enables optimum layout for lower circuit inductance and reduced switch node ringing
- RoHS Compliant

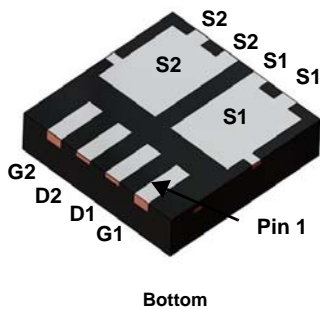


General Description

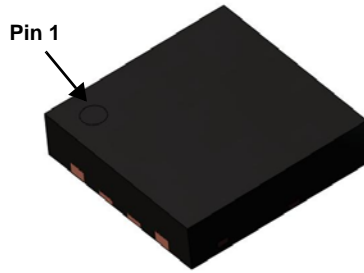
This device is designed specifically as a single package solution for Li-Ion battery pack protection circuit and other ultra-portable applications. It features two common drain N-channel MOSFETs, which enables bidirectional current flow. FDPC4044 combines ON Semiconductor's advanced PowerTrench® process with state of the art packaging process to minimize the on-state resistance.

Applications

- Battery management
- Load switch
- Battery protection

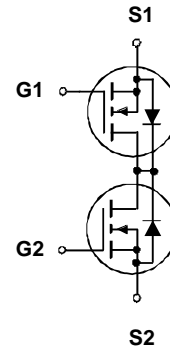


Bottom



Top

Power Clip 33



MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

| Symbol | Parameter | Conditions | Rated Value | Units |
|----------------|--|----------------------------------|-------------|-------|
| V_{S1S2} | Source1 to Source2 Voltage | | 30 | V |
| V_{GS} | Gate to Source Voltage | (Note 3) | ±20 | V |
| I_{S1S2} | Source1 to Source2 Current | -Continuous $T_A = 25\text{ °C}$ | 27 | A |
| | | -Pulsed | 120 | |
| P_D | Power Dissipation | $T_A = 25\text{ °C}$ | 2.7 | W |
| | | $T_A = 25\text{ °C}$ | 1 | |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | | -55 to +150 | °C |

Thermal Characteristics

| Symbol | Parameter | Conditions | Rated Value | Units |
|-----------------|---|------------|-------------|-------|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | (Note 1a) | 47 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | (Note 1b) | 127 | |

Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|----------------|----------|---------------|-----------|------------|------------|
| 40CF | FDPC4044 | Power Clip 33 | 13 " | 12 mm | 3000 units |

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
|--------|-----------|-----------------|-----|-----|-----|-------|

Off Characteristics

| | | | | | | |
|------------|--|---|--|--|-----|---------------|
| I_{S1S2} | Zero Gate Voltage Source1 to Source2 Current | $V_{S1S2} = 24\text{ V}, V_{GS} = 0\text{ V}$ | | | 1 | μA |
| I_{GSS} | Gate to Source Leakage Current | $V_{GS} = 20\text{ V}, V_{S1S2} = 0\text{ V}$ | | | 100 | nA |

On Characteristics

| | | | | | | |
|----------------|---|---|-----|-----|-----|------------|
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS} = V_{S1S2}, I_{S1S2} = 250\text{ }\mu\text{A}$ | 1.2 | 1.5 | 3 | V |
| $r_{S1S2(on)}$ | Static Source1 to Source2 On Resistance | $V_{GS} = 10\text{ V}, I_{S1S2} = 27\text{ A}$ | | 3.2 | 4.3 | m Ω |
| | | $V_{GS} = 4.5\text{ V}, I_{S1S2} = 23\text{ A}$ | | 4.6 | 6.4 | |
| | | $V_{GS} = 10\text{ V}, I_{S1S2} = 27\text{ A}, T_J = 125\text{ }^\circ\text{C}$ | | 4.5 | 7 | |
| g_{FS} | Forward Transconductance | $V_{S1S2} = 10\text{ V}, I_{S1S2} = 27\text{ A}$ | | 150 | | S |

Dynamic Characteristics

| | | | | | | |
|------------|------------------------------|---|--|------|------|----|
| C_{iss} | Input Capacitance | $V_{S1S2} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | | 2295 | 3215 | pF |
| C_{oss} | Output Capacitance | | | 627 | 880 | pF |
| C_{riss} | Reverse Transfer Capacitance | | | 66 | 95 | pF |

Switching Characteristics

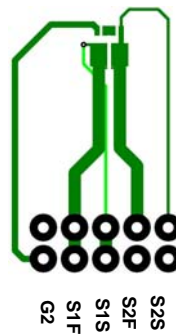
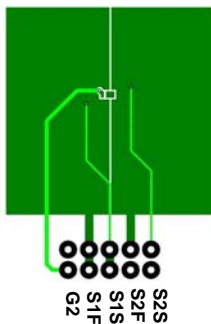
| | | | | | | |
|--------------|---------------------------------|---|--|-----|----|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{S1S2} = 15\text{ V}, I_{S1S2} = 27\text{ A}, V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$ | | 8.5 | 17 | ns |
| t_r | Rise Time | | | 4.8 | 10 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 32 | 52 | ns |
| t_f | Fall Time | | | 5.2 | 10 | ns |
| Q_g | Total Gate Charge | $V_{S1S2} = 15\text{ V}, I_{S1S2} = 27\text{ A}, V_{G1S1} = 10\text{ V}, V_{G2S2} = 0\text{ V}$ | | 35 | 49 | nC |
| Q_{gs} | Gate to Source1 Gate Charge | | | 5.7 | | nC |
| Q_{gd} | Gate to Source2 "Miller" Charge | | | 4.7 | | nC |

Source1 to Source2 Diode Characteristics

| | | | | | |
|-----------|---|--|-----|-----|---|
| I_{fss} | Maximum Continuous Source1 to Source2 Diode Forward Current | | | 1 | A |
| V_{fss} | Source1 to Source2 Diode Forward Voltage | $V_{G1S1} = 0\text{ V}, V_{G2S2} = 4.5\text{ V}, I_{fss} = 27\text{ A}$ (Note 2) | 0.8 | 1.2 | V |

Notes:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

- As an N-ch device, the negative V_{gs} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

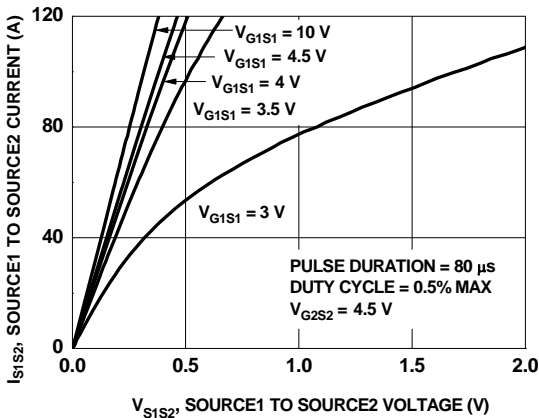


Figure 1. On-Region Characteristics

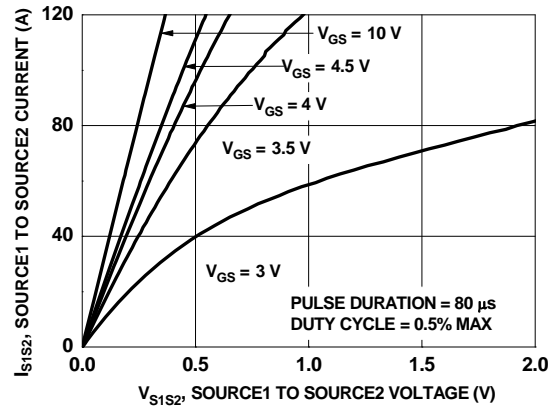


Figure 2. On-Region Characteristics

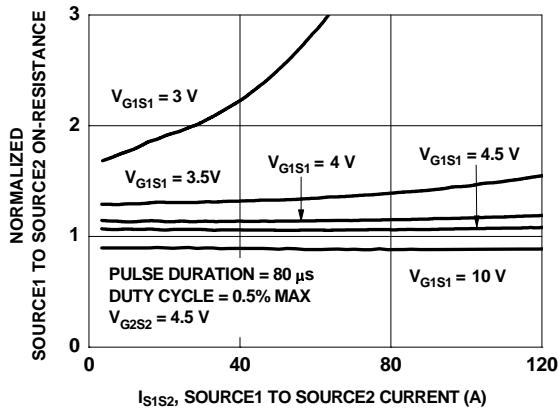


Figure 3. Normalized On-Resistance vs Source1 to Source2 Current and Gate Voltage

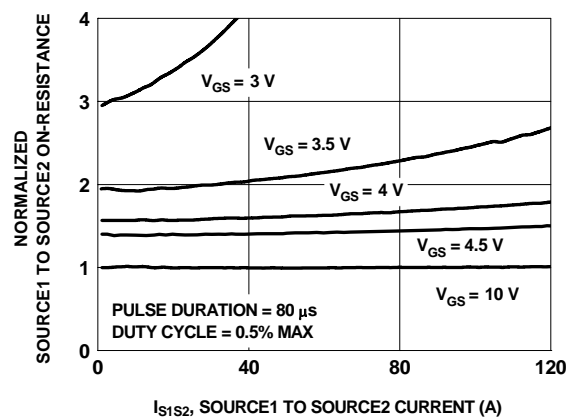


Figure 4. Normalized On-Resistance vs Source1 to Source2 Current and Gate Voltage

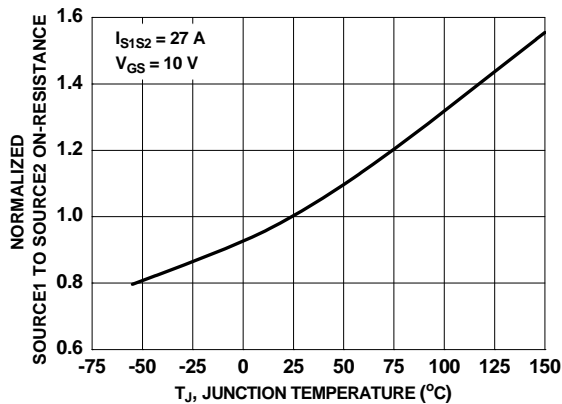


Figure 5. Normalized On-Resistance vs Junction Temperature

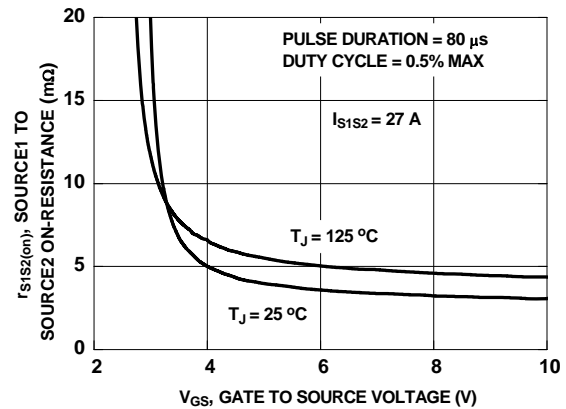


Figure 6. On-Resistance vs Gate to Source Voltage

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

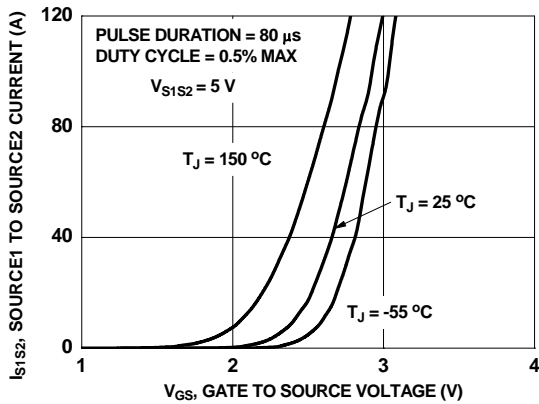


Figure 7. Transfer Characteristics

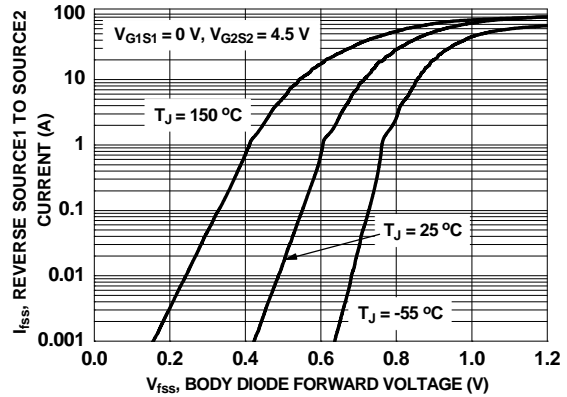


Figure 8. Source1 to Source2 Diode Forward Voltage vs Source Current

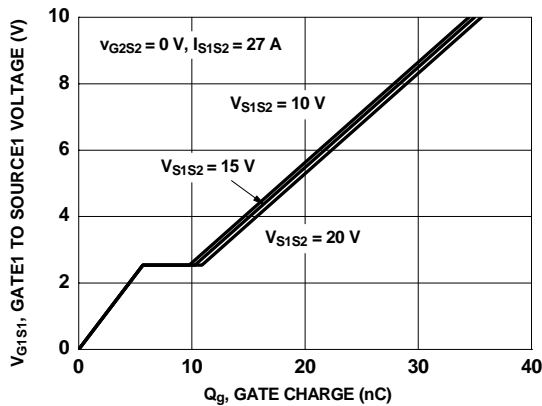


Figure 9. Gate Charge Characteristics

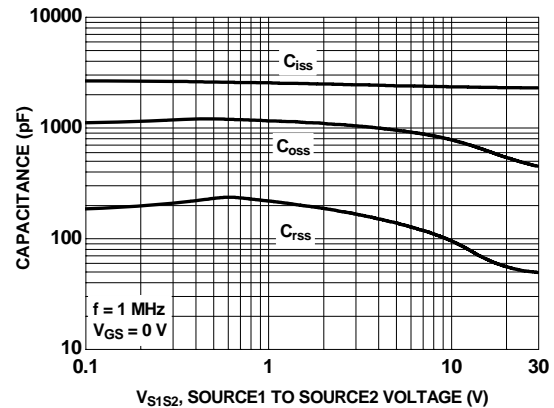


Figure 10. Capacitance vs Source1 to Source2 Voltage

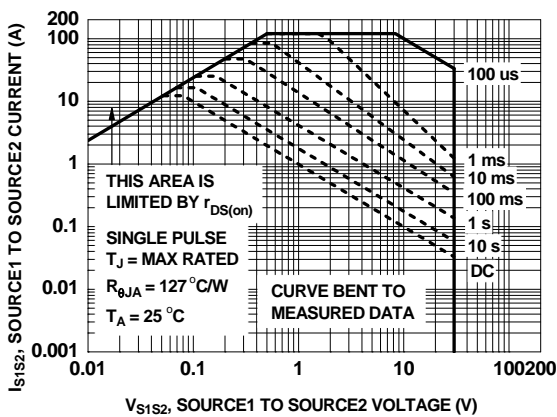


Figure 11. Forward Bias Safe Operating Area

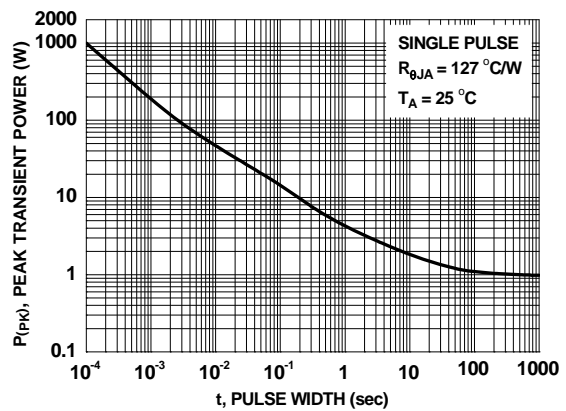


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

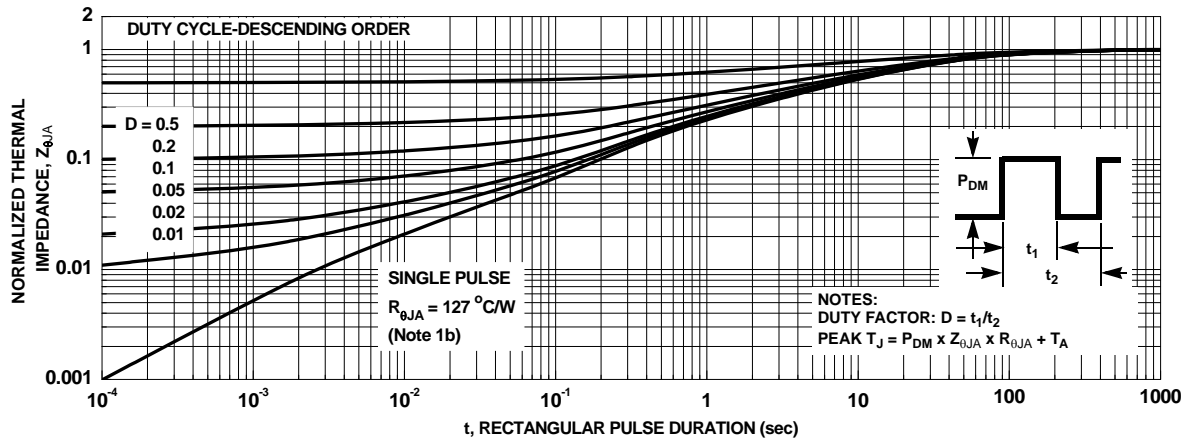
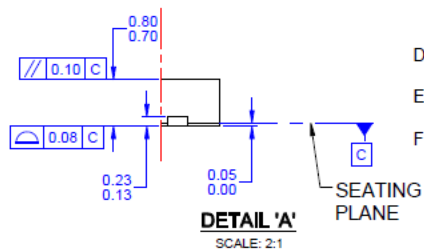
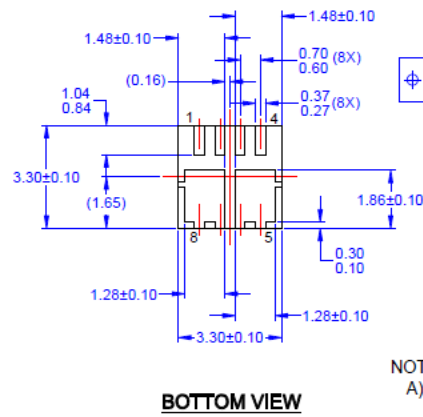
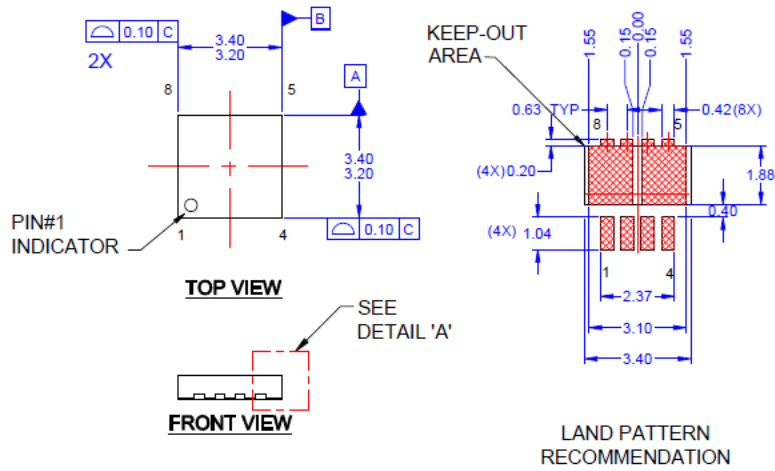



Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



- NOTES: UNLESS OTHERWISE SPECIFIED
- DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-229, DATED 08/2012
 - ALL DIMENSIONS ARE IN MILLIMETERS.
 - DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
 - DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
 - DRAWING FILE NAME: MKT-PQFN08LREV2

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