

1. General description

Planar passivated very sensitive gate Silicon Controlled Rectifier in a SOT54 (TO-92) plastic package.

2. Features and benefits

- Planar passivated for voltage ruggedness and reliability
- Very sensitive gate

3. Applications

- Ignition circuits
- Low power latching circuits
- Protection / shut-down circuits: lighting ballasts
- Protection / shut-down circuits: Switched Mode Power Supplies

4. Quick reference data

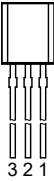
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RRM}	repetitive peak reverse voltage		-	-	400	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 83\text{ °C}$; Fig. 1	-	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq 83\text{ °C}$; Fig. 2 ; Fig. 3	-	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 8.3\text{ ms}$	-	-	9	A
		half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5	-	-	8	A
T_j	junction temperature		-	-	125	°C
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 25\text{ °C}$; Fig. 7	-	-	50	μA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 268\text{ V}$; $T_j = 125\text{ °C}$; $R_{GK} = 1\text{ k}\Omega$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; Fig. 12	500	800	-	V/μs

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		$V_{DM} = 268\text{ V}$; $T_j = 125\text{ }^{\circ}\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit; Fig. 12		-	25	-	V/ μs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	A	anode	 TO-92 (SOT54)	
2	G	gate		
3	K	cathode		

6. Ordering information

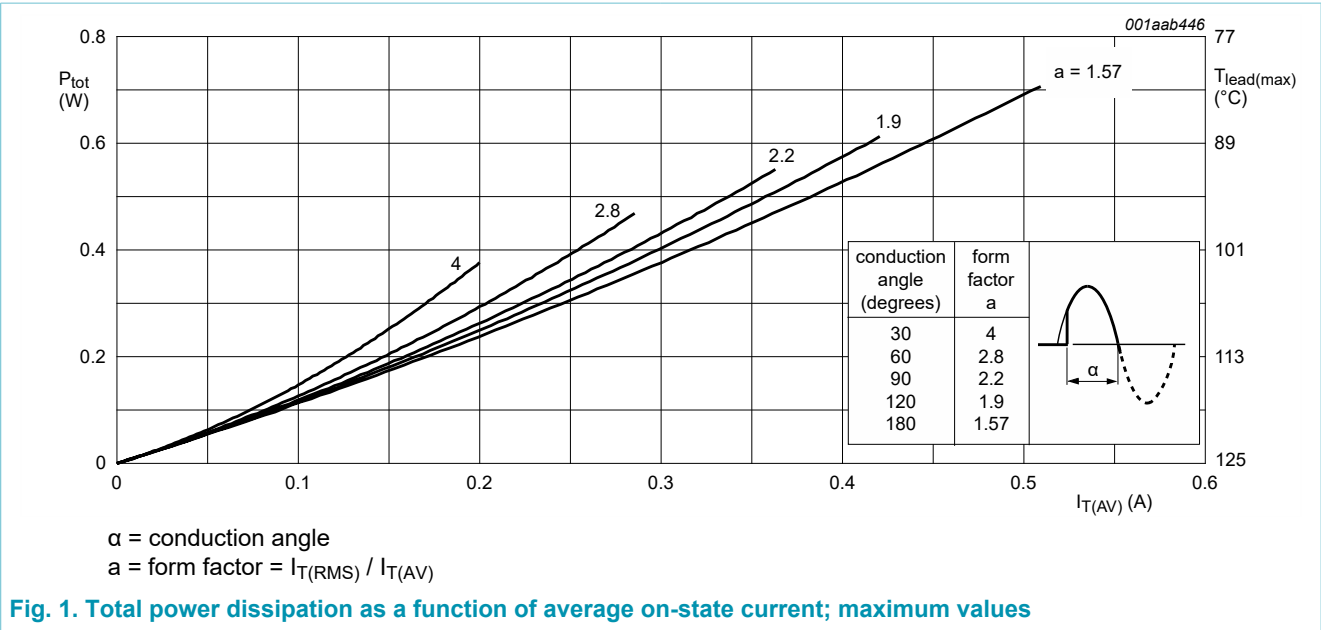
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT169D-L	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	400	V
V_{RRM}	repetitive peak reverse voltage		-	400	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 83\text{ }^{\circ}\text{C}$; Fig. 1	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq 83\text{ }^{\circ}\text{C}$; Fig. 2; Fig. 3	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $t_p = 8.3\text{ ms}$	-	9	A
		half sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $t_p = 10\text{ ms}$; Fig. 4; Fig. 5	-	8	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN	-	0.32	A^2s
dl_T/dt	rate of rise of on-state current	$I_T = 2\text{ A}$; $I_G = 10\text{ mA}$; $dl_G/dt = 100\text{ mA}/\mu\text{s}$	-	50	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	1	A
V_{RGM}	peak reverse gate voltage		-	5	V
P_{GM}	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	150	$^{\circ}\text{C}$
T_j	junction temperature		-	125	$^{\circ}\text{C}$



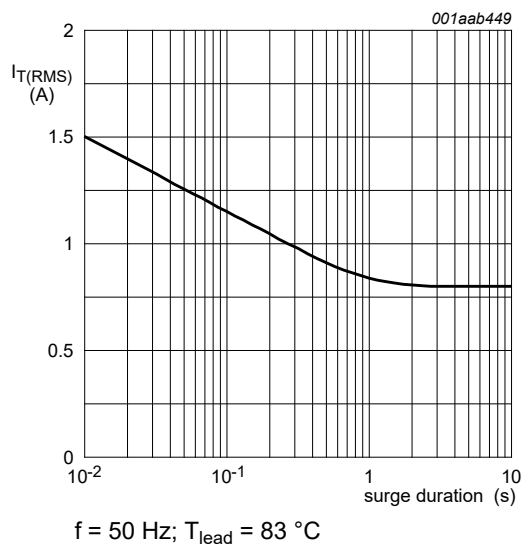


Fig. 2. RMS on-state current as a function of surge duration for sinusoidal currents

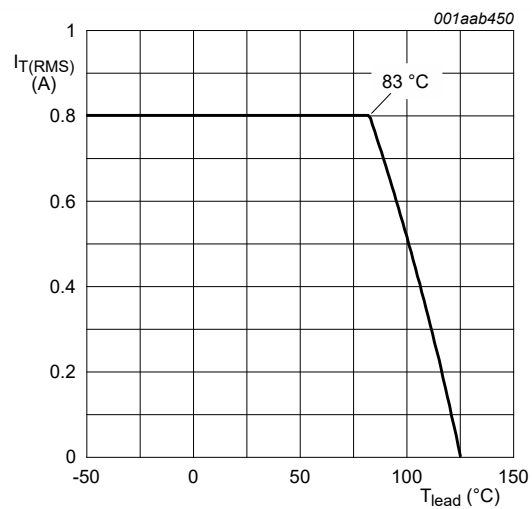


Fig. 3. RMS on-state current as a function of lead temperature; maximum values

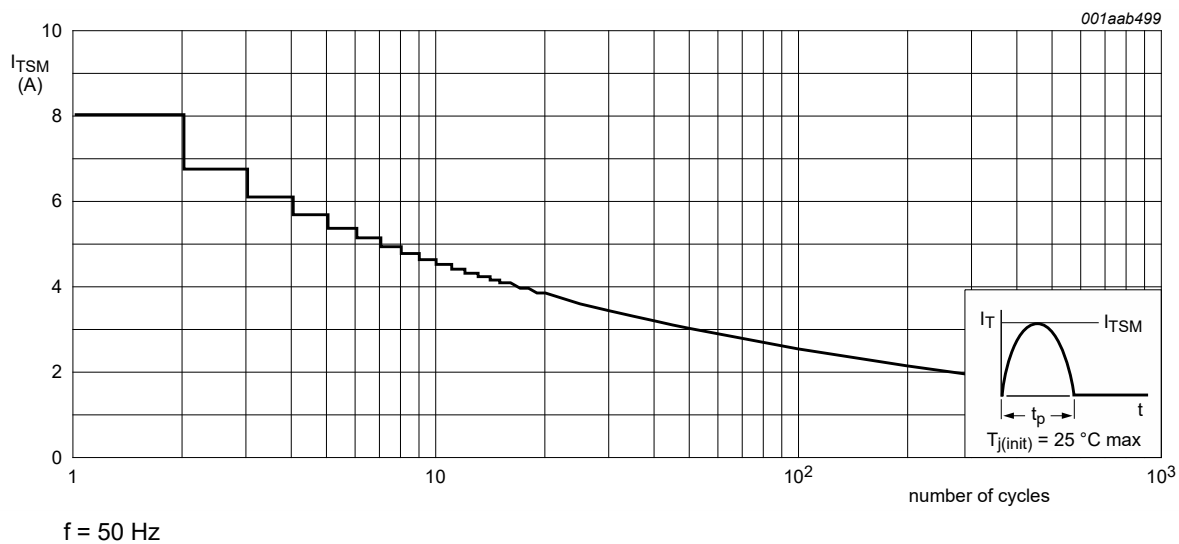
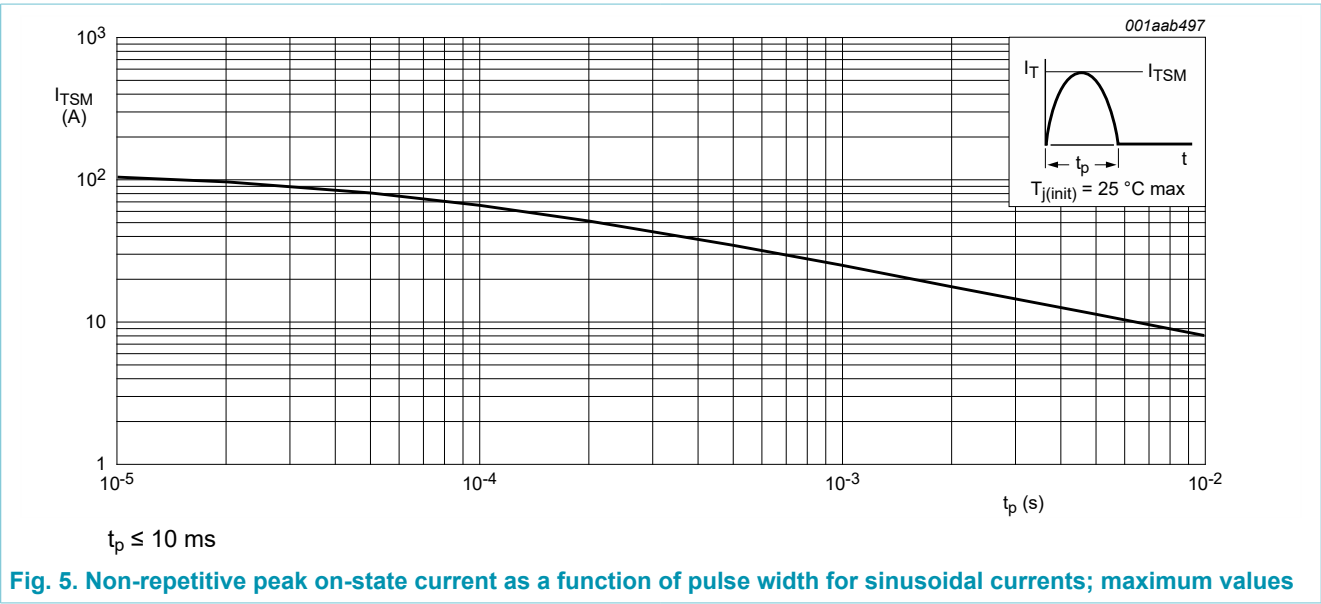


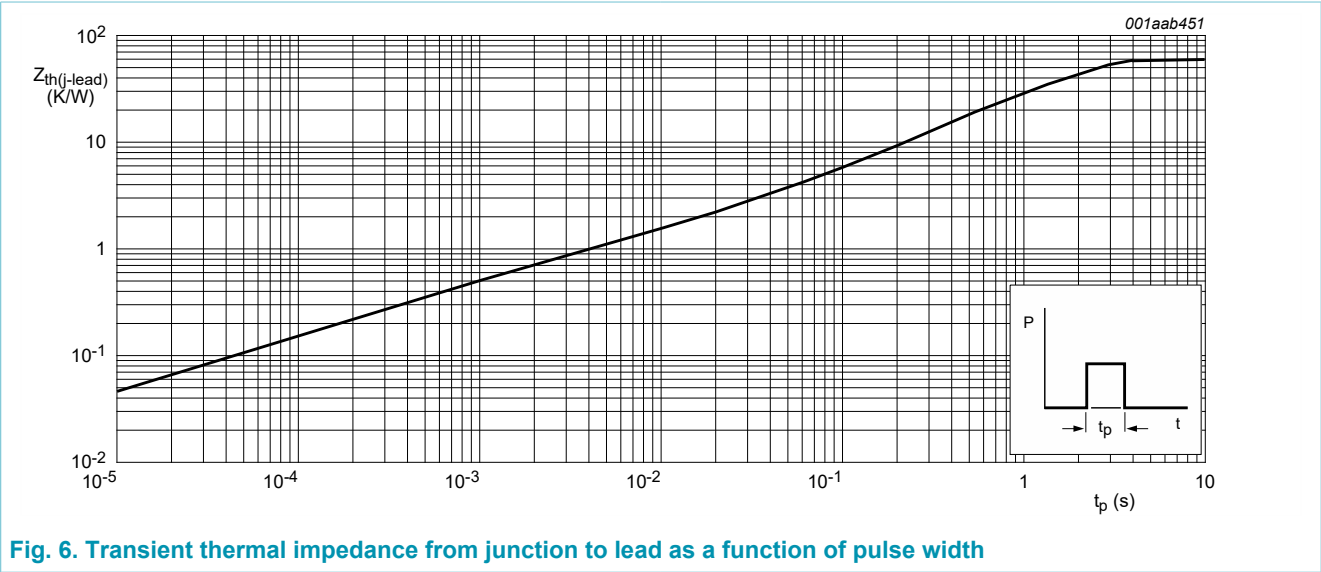
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	Fig. 6	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board mounted: lead length = 4 mm	-	150	-	K/W



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I _{GT}	gate trigger current	V _D = 12 V; I _T = 10 mA; T _j = 25 °C; Fig. 7		-	-	50	μA
I _L	latching current	V _D = 12 V; I _G = 0.5 mA; T _j = 25 °C; Fig. 8		-	2	4	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; Fig. 9		-	0.4	1	mA
V _T	on-state voltage	I _T = 1.2 A; T _j = 25 °C; Fig. 10		-	1.25	1.7	V
V _{GT}	gate trigger voltage	V _D = 12 V; I _T = 10 mA; T _j = 25 °C; Fig. 11		-	0.5	0.8	V
		V _D = 12 V; I _T = 10 mA; T _j = 125 °C; Fig. 11		0.2	0.3	-	V
I _D	off-state current	V _D = 400 V; R _{GK(ext)} = 1 kΩ; T _j = 25 °C		-	-	2	μA
		V _D = 400 V; R _{GK(ext)} = 1 kΩ; T _j = 125 °C		-	0.05	0.1	mA
I _R	reverse current	V _R = 400 V; T _j = 25 °C; R _{GK(ext)} = 1 kΩ		-	0.05	2	μA
		V _R = 400 V; T _j = 125 °C; R _{GK(ext)} = 1 kΩ		-	0.05	0.1	mA
Dynamic characteristics							
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 268 V; T _j = 125 °C; R _{GK} = 1 kΩ; (V _{DM} = 67% of V _{DRM}); exponential waveform; Fig. 12		500	800	-	V/μs
		V _{DM} = 268 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit; Fig. 12		-	25	-	V/μs

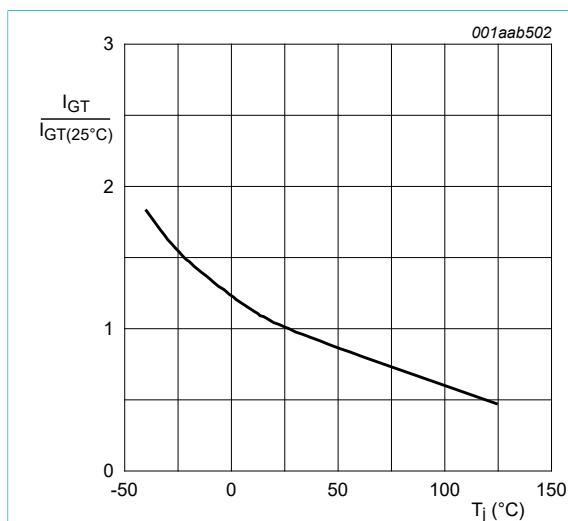


Fig. 7. Normalized gate trigger current as a function of junction temperature

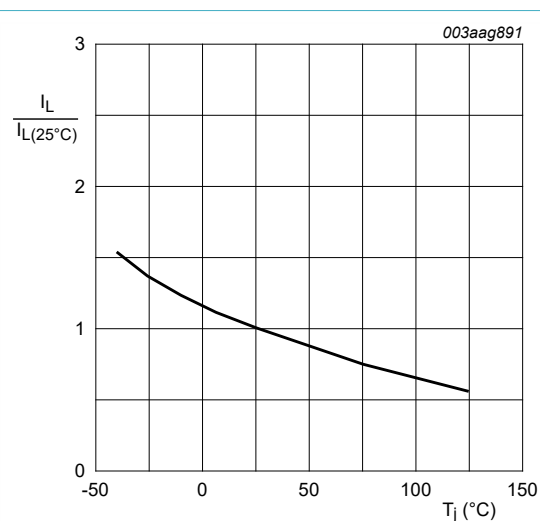


Fig. 8. Normalized latching current as a function of junction temperature

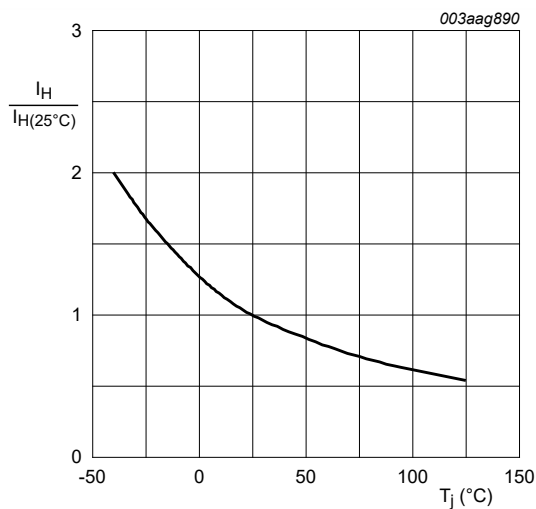
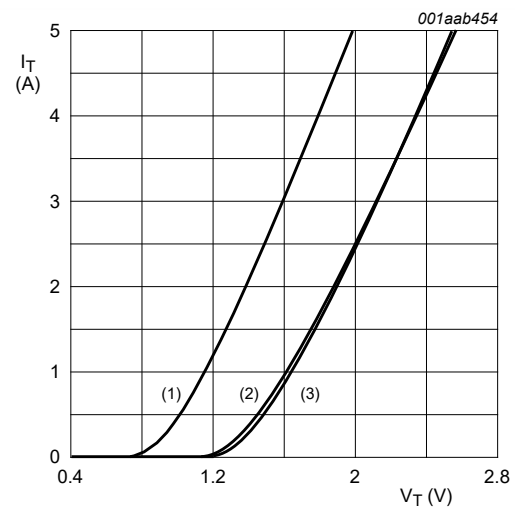


Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 1.067 \text{ V}; R_s = 0.187 \Omega$
(1) $T_j = 125^{\circ}\text{C}$; typical values
(2) $T_j = 125^{\circ}\text{C}$; maximum values
(3) $T_j = 25^{\circ}\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

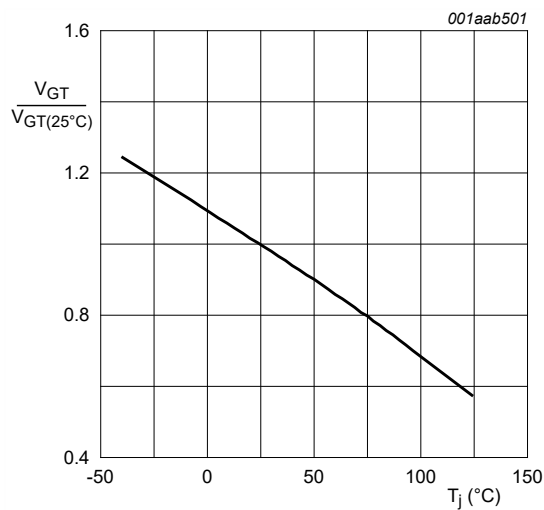
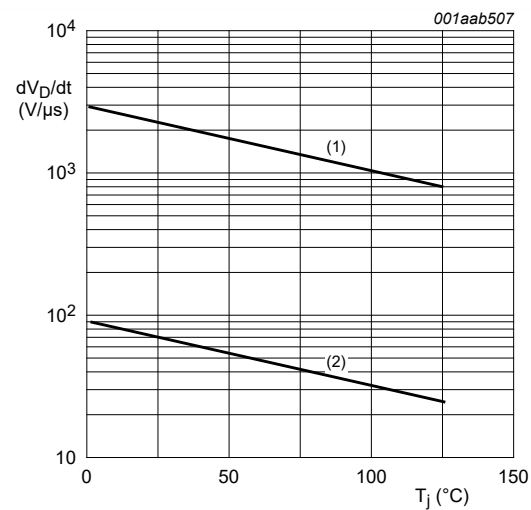


Fig. 11. Normalized gate trigger voltage as a function of junction temperature



(1) $R_{GK} = 1 \text{ k}\Omega$
(2) gate open circuit

Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

10. Package outline

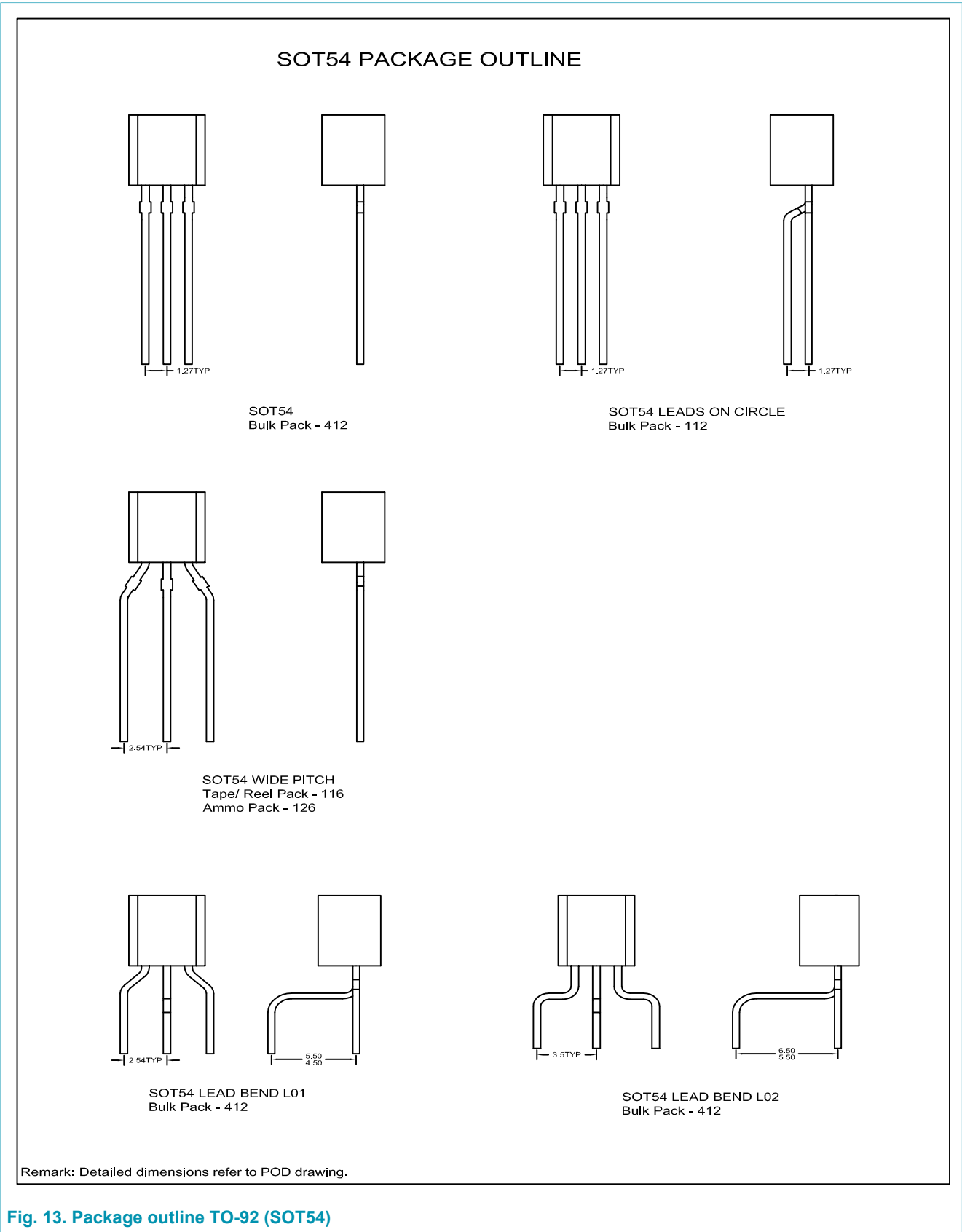


Fig. 13. Package outline TO-92 (SOT54)

11. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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