



TFT DISPLAY MODULE

Product Specification

Customer	Standard		
Product Number	DMT028QVHXCMI-1A		
Customer Part Number			
Customer Approval		Date:	

Internal Approvals		
Product Mgr	Doc. Control	Electr. Eng
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Date: 01/07/17	Date: 01/07/17	Date: 01/07/17

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1.0 Main Features

Item	Contents
Screen Size	2.8" Diagonal
Display Format	240 x RGB x 320 Dots
N° of Colour	65K/262K
Active Area	43.20 mm (V) x 57.60 mm (H)
PCT View Area	44.20 (V) x 58.60 mm (H)
LCD Type	TFT
Mode	Transmissive / Normally Black
Viewing Direction	ALL
TFT Interface	8/9/16/18 bit 8080 MCU 3/4-wire SPI 3/4-wire SPI+16/18 bit RGB
PCT Interface	I2C
TFT Driver IC	ST7789V
PCT Driver IC	FT6236
Simultaneous Touch Points	1
Backlight Type	LED
Operating Temperature	-20°C ~ +70°C
Storage Temperature	-30°C ~ +80°C
RoHS compliant	Yes

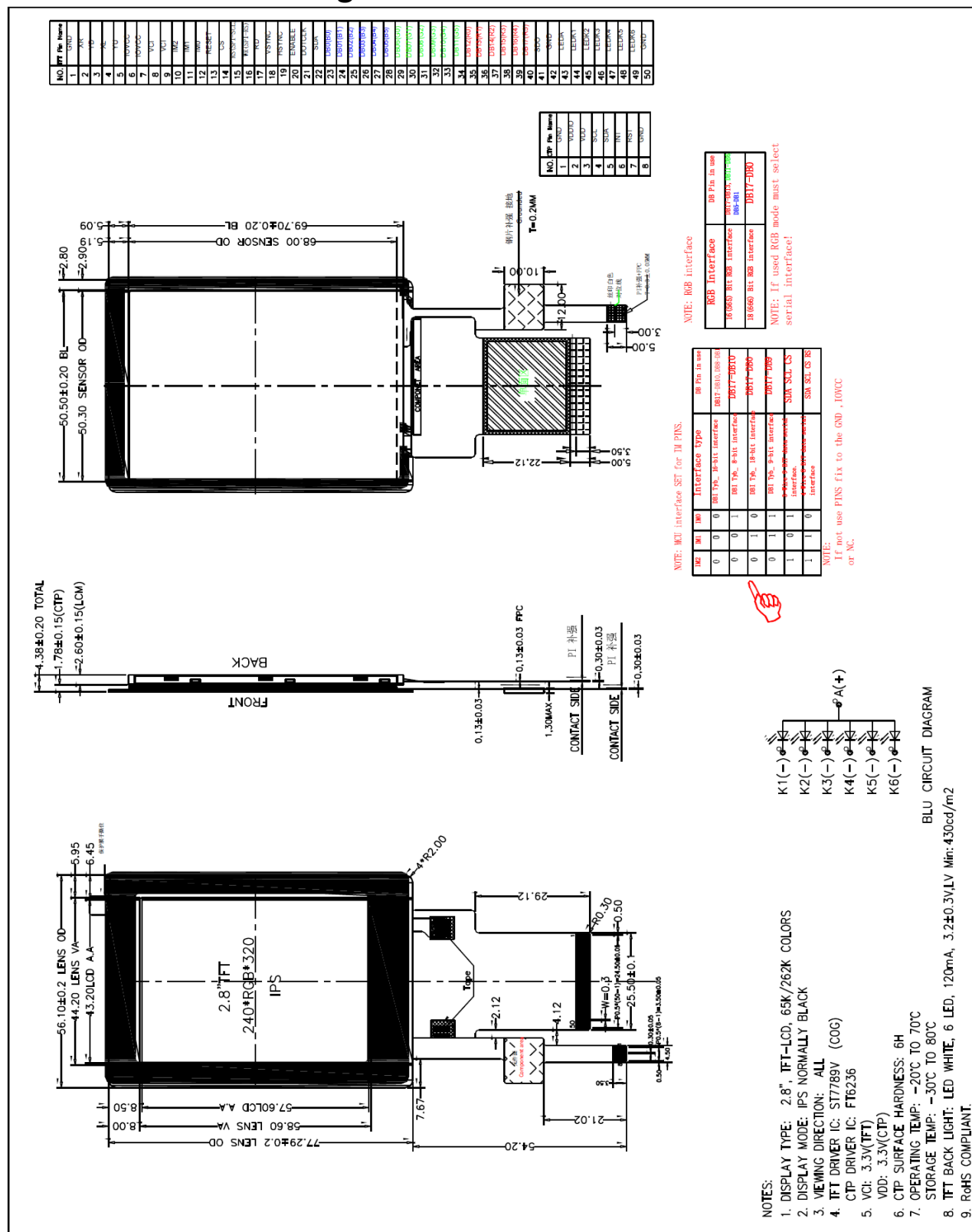
2.0 Mechanical Specification

2.1 Mechanical Characteristics

Item	Characteristic	Unit
Overall Dimensions	56.10 mm (H) x 77.29 mm (V) x 4.38 mm (D)	mm
pixel Pitch	180 (H) x 180 (V)	μm
Weight	TBD	g

Product N°: DMT028QVHXCMI-1A REV 1.0

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3.0 Electrical Specification

3.1 Absolute Maximum Ratings

3.1.1 TFT

Item	Symbol	Condition	Min	Max	Unit	Note
Power Supply Voltage LCM	VCI		-0.3	4.6	V	
Digital Interface Supply Voltage	IOVCC		-0.3	4.6	V	
Operating Temperature	TOP		-20	70	°C	1
Storage Temperature	TST		-30	80	°C	1,2,3

Note 1. 90 % RH Max for Ta<50 °C, and 60% RH for Ta≥50°C.

Note 2. In case of below 0°C, the response time of liquid crystal (LC) becomes slower and the colour of panel becomes darker than normal one. Level of retardation depends on temperature, because of LC's characteristic.

Note 3. Only operation is guaranteed at operating temperature. Contrast, response time, another display quality are evaluated at +25°C.

3.1.2 PCT

Item	Symbol	Condition	Min	Max	Unit	Note
Power Supply Voltage	VDD		-0.3	3.6	V	4
Operating Temperature	TOP		-20	70	°C	-
Storage Temperature	TST		-30	80	°C	-

Note 4. If used beyond the absolute maximum ratings, FT6236 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

3.2 Electrical Characteristics

3.2.1 TFT

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Voltage	VCI	Ta=25°C	2.4	2.8	3.3	V	
Digital Interface Supply Voltage	IOVCC	Ta=25°C	1.65	1.8	3.3		
Input Voltage for Logic	VIH		0.7IOVCC	-	IOVCC	V	
	GND		GND	-	0.3 IOVCC	V	
Output Voltage for Logic	VOH		0.8IOVCC	-	IOVCC	V	
	VOL		GND	-	0.2IOVCC	V	
Current Consumption	IDD		-	6.8	-	mA	1

Note 1: The specified power consumption is under the conditions of VDD=3.3V.

3.2.2 PCT

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Voltage	VDD		2.8	3.3	3.6	V	
Input Voltage for Logic	VIH		0.7 VDDIO	-	VDDIO	V	
	VIL		-0.3	-	0.3 VDDIO	V	
Output Voltage for Logic	VOH	IOH = 01.mA	0.7 VDDIO	-	-	V	
	VOL		-	-	0.3 VDDIO	V	
Normal operation mode Current Consumption	IOPR	VDD=2.8V Ta=25°C MCLK= 17.5MHz	-	4	-	mA	
Monitor mode Current Consumption	IMON		-	1.5	-	mA	
Sleep mode Current Consumption	ISLP		-	50	-	uA	

3.3 Interface Pin Assignment

3.3.1 TFT Pin Assignment

No.	Symbol	Function
1	GND	Ground.
2	XR(NC)	Touch panel Right Glass Terminal
3	YD(NC)	Touch panel Bottom Film Terminal
4	XL(NC)	Touch panel LIFT Glass Terminal
5	YU(NC)	Touch panel Top Film Terminal
6	IOVCC	Supply voltage for IO (1.8-3.3V). Supply voltage for IO (1.8-3.3V). Supply voltage (3.3V).
7	IOVCC	Red data input.
8	VCI	Red data input.
9	VCI	Supply voltage (3.3V).
10	IM2	MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface. Fix this pin at IOVCC and GND.
11	IM1	Line synchronizing signal for RGB Interface mode. If not used, please connect to GND or IOVCC.
12	IM0	Pixel clock signal for RGB Interface mode. If not used, please connect to GND or IOVCC.
13	RESET	This signal will reset the device and must be applied to properly initialize the chip.
14	CS	Chip select input pin ("Low" enable). Fix this pin at IOVCC or GND when not in use.
15	RS(SPI-SCL)	This pin is used to select "Data or Command" in the parallel interface. When D/CX = '1', data is selected. When D/CX = '0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. Fix this pin at IOVCC or GND when not in use.
16	WR(SPI-RS)	The data is applied on the rising edge of the SCL signal. Fix this pin at IOVCC or GND when not in use.
17	RD	Serves as a read signal and MCU read data at the rising edge. Fix this pin at IOVCC or GND when not in use
18	VSYNC	Frame synchronizing signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use.
19	HSYNC	Line synchronizing signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use.

No.	Symbol	Function
20	ENABLE	Data enable signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use.
21	DOTCLK	Dot clock signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use.
22	SDA	Serial input signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at IOVCC or GND.
23-40	DB0-DB7	Data bus. If not used pin, fix this pin to GND.
41	SDO	SPI interface output pin. -The data is output on the falling edge of the SCL signal. -If not used, let this pin open.
42	GND	Ground.
43	LEDA	Anode pin of backlight
44	LEDK1	Cathode pin OF backlight
45	LEDK2	Cathode pin OF backlight
46	LEDK3	Cathode pin OF backlight
47	LEDK4	Cathode pin OF backlight
48	LEDK5	Cathode pin OF backlight
49	LEDK6	Cathode pin OF backlight
50	GND	Ground.

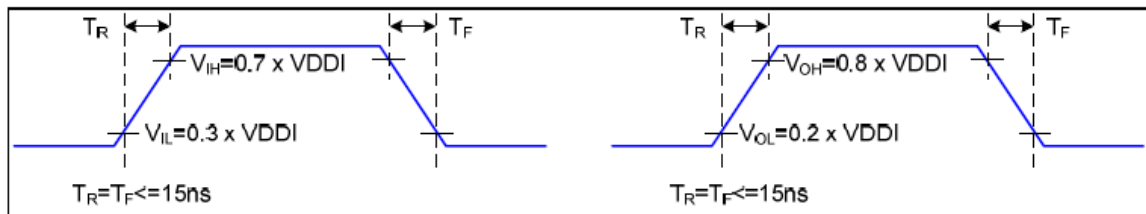
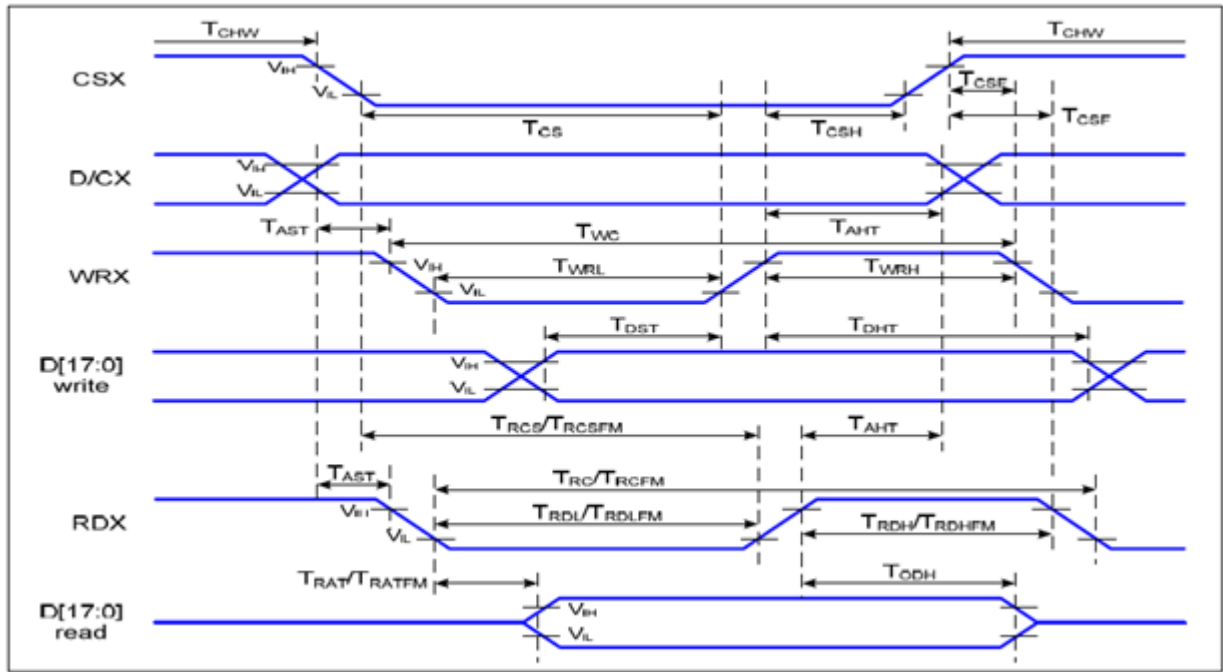
3.3.2 PCT PIN ASSIGNMENT

NO.	SYMBOL	DISCRIPTION
1	GND	Ground.
2	VDDIO	I/O power supply voltage
3	VDD	Supply voltage.
4	SCL	I2C clock input.
5	SDA	I2C data input and output
6	INT	External interrupt to the host.
7	RST	External Reset, Low is active.
8	GND	Ground.

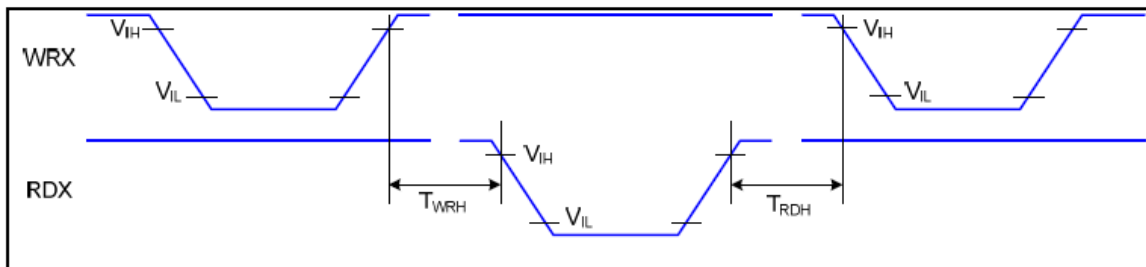
3.4 Timing Characteristics

3.4.1 AC Characteristics

8080 Series MCU parallel interface timing characteristics: 18/16/9/8-bit bus



Rising and Falling Timing for I/O Signal



Write-to-Read and Read-to-Write Timing

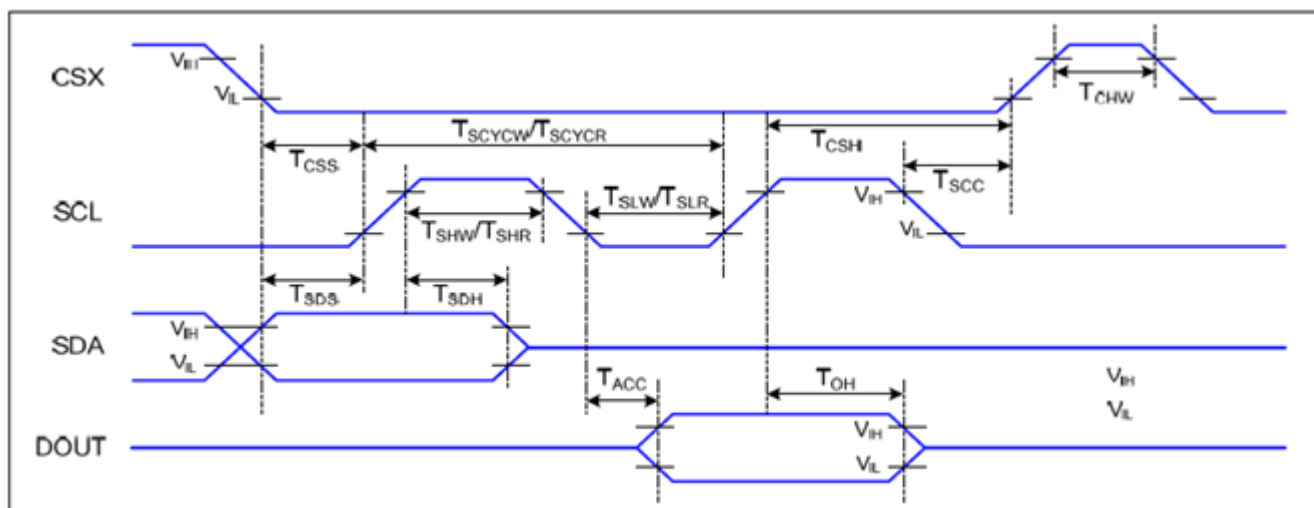
Note: The rising time and falling time (T_R , T_F) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of V_{DDI} for Input signals.

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T _{AST}	Address setup time	0		ns	-
	T _{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T _{CHW}	Chip select "H" pulse width	0		ns	-
	T _{CS}	Chip select setup time (Write)	15		ns	
	T _{RCS}	Chip select setup time (Read ID)	45		ns	
	T _{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T _{CSF}	Chip select wait time (Write/Read)	10		ns	
	T _{CSH}	Chip select hold time	10		ns	
WRX	T _{WC}	Write cycle	66		ns	
	T _{WRH}	Control pulse "H" duration	15		ns	
	T _{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T _{RC}	Read cycle (ID)	160		ns	When read ID data
	T _{RDH}	Control pulse "H" duration (ID)	90		ns	
	T _{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T _{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T _{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T _{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T _{DST}	Data setup time	10		ns	For CL=30pF
	T _{DHT}	Data hold time	10		ns	
	T _{RAT}	Read access time (ID)		40	ns	
	T _{RATFM}	Read access time (FM)		340	ns	
	T _{ODH}	Output disable time	20	80	ns	

3.4.2 Display Serial Interface Timing Characteristics

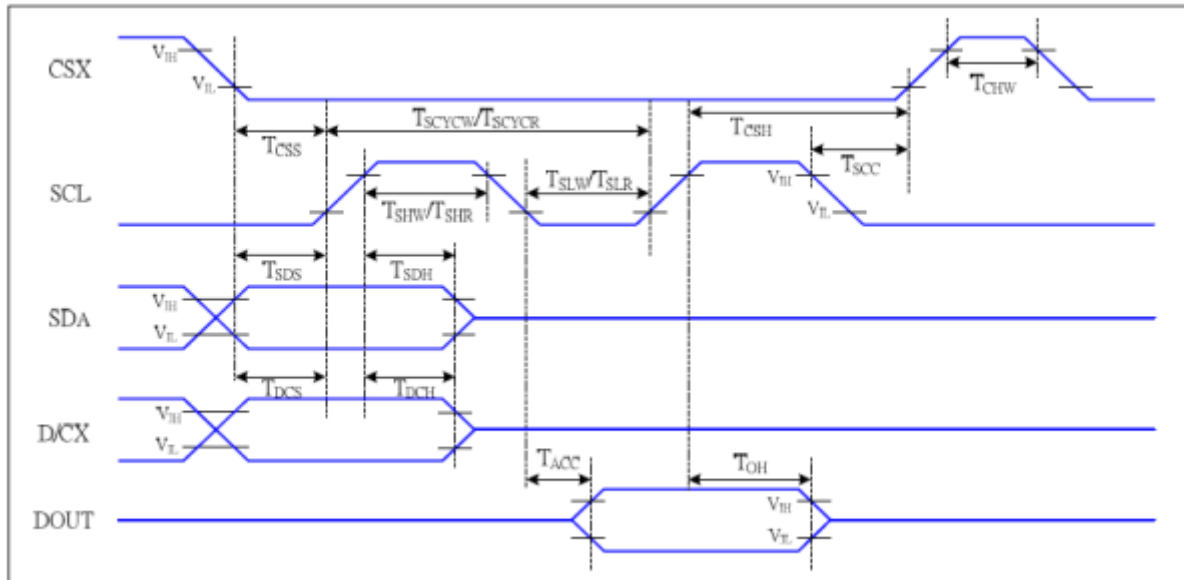
$IOVCC = 1.65 \text{ to } 3.3V$ $VCI = 2.4 \text{ to } 3.3V$ $AGND = DGND = 0V$ $Ta = -30 \text{ to } 70^{\circ}C$

3-line SPI system



Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum $CL=30pF$
	T_{OH}	Output disable time	15	50	ns	For minimum $CL=8pF$

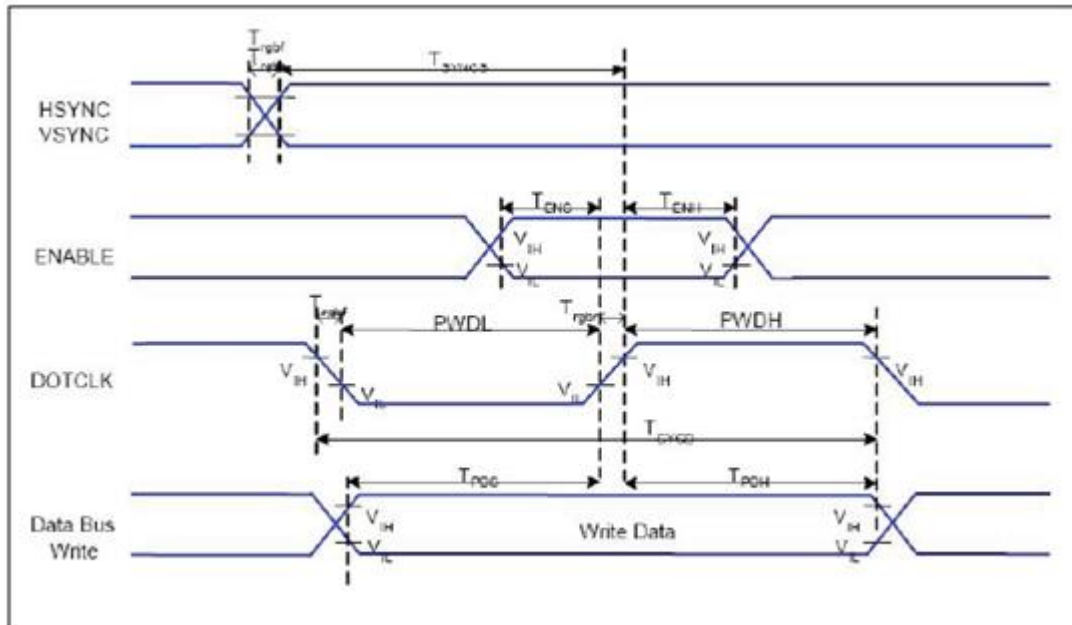
4-line SPI system



Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

3.4.3 Parallel RGB Interface Timing Characteristics

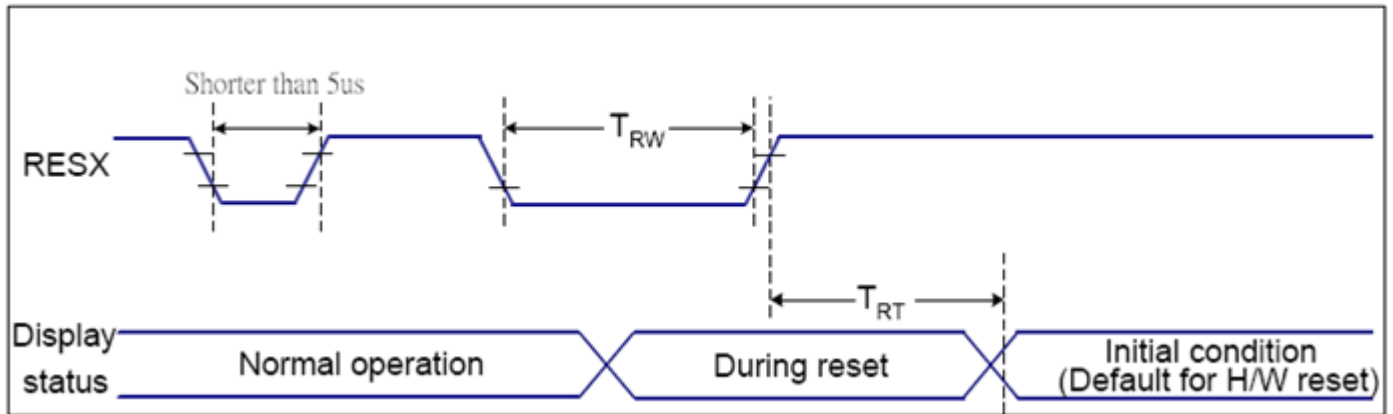
$IOVCC = 1.65 \text{ to } 3.3V$ $VCI = 2.4 \text{ to } 3.3V$ $AGND = DGND = 0V$ $Ta = -30 \text{ to } 70^{\circ}C$



Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{syncs}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	$Trghf$, $Trghf$	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

3.4.4 Reset Timing Characteristics

$IOVCC = 1.65 \text{ to } 3.3V$ $VCI = 2.4 \text{ to } 3.3V$ $AGND = DGND = 0V$ $Ta = -30 \text{ to } 70^{\circ}C$



Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Note:

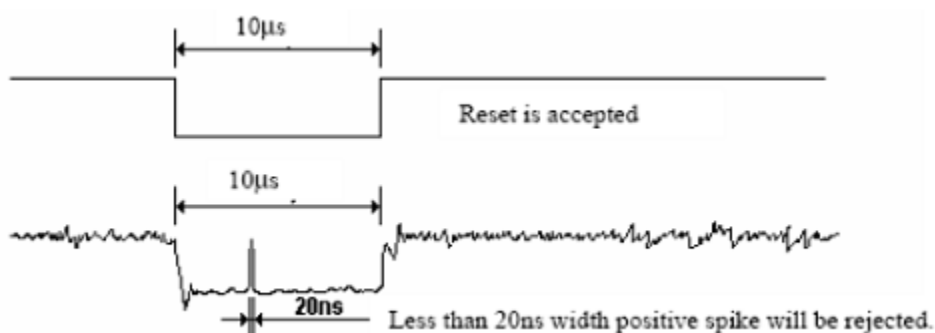
1. The reset cancel includes required time for loading the ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is a HW reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system resets according to the table below:

RESX Pulse	Action
Shorter than 5 μ s	Reset Rejected
Longer than 9 μ s	Reset
Between 5 μ s and 9 μ s	Reset starts

3. During the reset period, the display will be blank (Maximum time 120 ms, when reset starts in sleep out mode. The display remains in a blank state in sleep in mode). It will then return to the default condition for a hardware reset.

4. Spike rejection also applies during a valid reset pulse as shown below:



5. Reset is applied during sleep in mode.

6. Reset applied during sleep out mode

7. It is necessary to wait 5msec after releasing RESX before sending commands. The sleep out command cannot be sent for 120msec.

3.5.1 I2C Interface

The I2C is always configured in the Slave mode. The data transfer format is shown in Figure4-1:

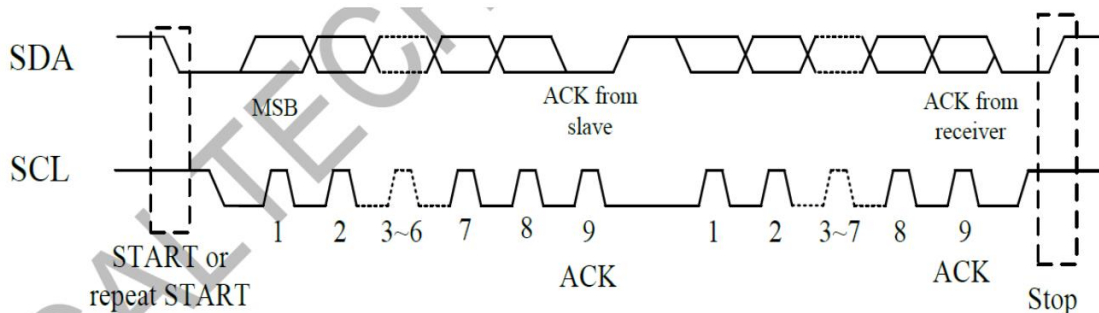


Figure 4-1 I2C Serial Data Transfer Format

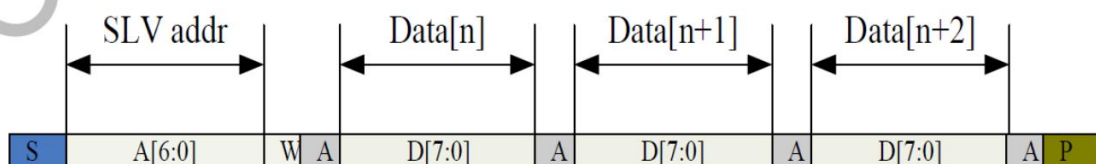


Figure 4-2 I2C master write, slave read

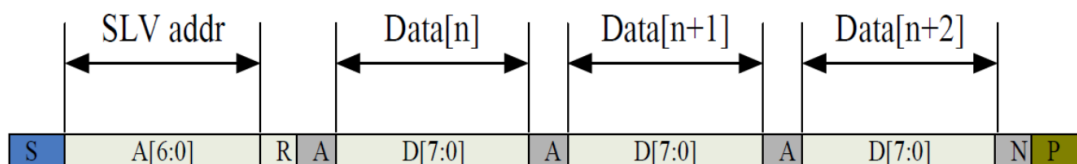


Figure 4-3 I2C master read, slave write

Table4-3 lists the meanings of the mnemonics used in the above figures.

Table 4-3 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0' for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table4-4.

Table 4-4 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	10	400	KHz
Bus free time between a STOP and START condition	4.7	\	us
Hold time (repeated) START condition	4.0	\	us
Data setup time	250	\	ns
Setup time for a repeated START condition	4.7	\	us
Setup Time for STOP condition	4.0	\	us

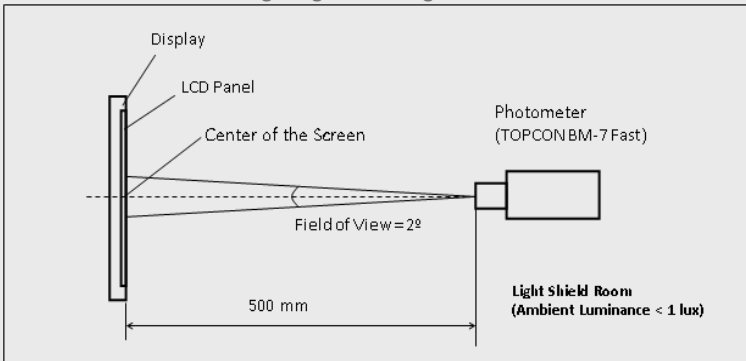
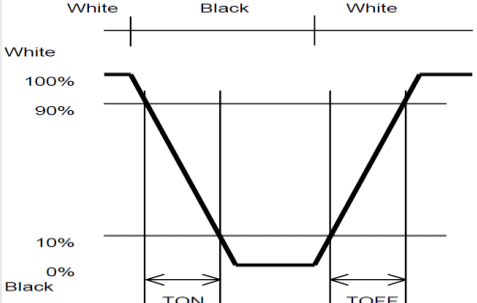
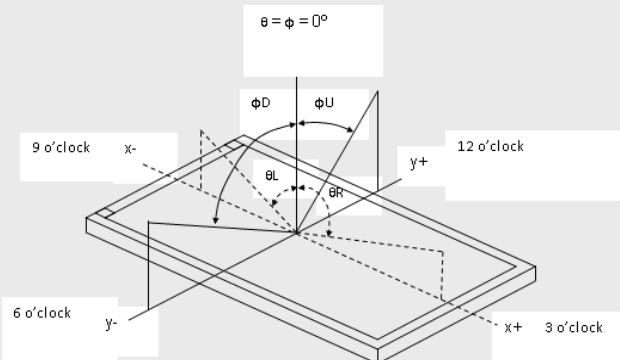
4.0 Optical Specification

4.1 Optical Characteristics

Measuring instruments : LCD-5100, Eldim, Topcon BM-7
 Driving condition: VDD = 3.3V, VSS = 0V
 Backlight: IF=40mA
 Measured temperature: Ta = 25 °C

Item		Symbol	Condition	Min	Typ	Max	Unit	Note
Response Time		TR+TF	$\theta=\phi=0^\circ$ Normal Viewing Angle	-	30	40	ms	2
Contrast Ratio		CR		600	800	-		3
Viewing Angle	Left	θ_L	$CR \geq 10$	-	80	-	deg	4
	Right	θ_R		-	80	-	deg	
	Up	ϕ_U		-	80	-	deg	
	Down	ϕ_D		-	80	-	deg	
Colour Chromaticity	Red	Rx	$CR \geq 10$	0.613	0.633	0.653	-	5
		Ry		0.325	0.345	0.365	-	
	Green	Gx		0.311	0.331	0.351	-	
		Gy		0.600	0.620	0.640	-	
	Blue	Bx		0.125	0.145	0.165	-	
		By		0.048	0.068	0.088	-	
	White	Wx		0.268	0.308	0.348	-	
		Wy		0.288	0.328	0.368	-	
Centre Brightness				580	630	-	cd/m ²	6
Brightness Distribution				80	-	-	%	7

4.1.1 Test Method

Note	Item	Test Method
1	Setup	The display should be stabilised at a given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilise the luminance, measurements should be executed after lighting the backlight for 30 minutes in a windless room. 
2	Response time	Measure output signal waveform by the luminance meter when raster of window pattern is changed from white to black and from black to white. 
3	Contrast ratio	Measure maximum brightness and minimum brightness at the centre of the screen by displaying raster or window pattern. Then calculate the ratio between these two values. $\text{Contrast Ratio (CR)} = \frac{\text{Brightness of unselected position (white)}}{\text{Brightness of selected position (black)}}$
4	Viewing angle Horizontal θ Vertical ϕ	Move the luminance meter from right to left and up and down and determinate the angles where contrast ratio is 10 
5	Colour chromaticity	Measure chromaticity coordinates x and y of CIE1931 colorimetric system
6	Centre brightness	Measure the brightness at the centre of the screen
7	Brightness distribution	(Brightness distribution) = $100 \times B/A \%$ A: max. brightness of the 9 points B: min. brightness of the 9 points

5.0 Backlight Specification

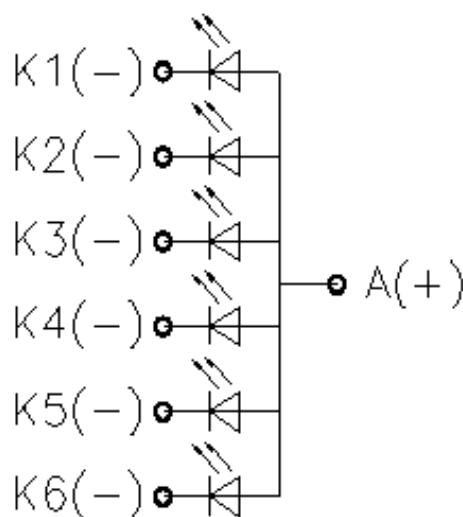
5.1 LED Driving Conditions

Item	Symbol	Condition	Min	Typ	Max	Unit
Forward Current	IF	Ta=25 °C	90	120	-	mA
Forward Voltage	VF	Ta= 25°C		3.2		V
LED life time	Hr				50k	hour

Note:

- The lifetime of the LED is defined as a period till the brightness of the LED decreases to the half of its initial value.
- This figure is given as a reference purpose only, and not a guarantee.
- This figure is estimated for an LED operating alone.
The performance of an LED may differ when assembled as a monitor together with a TFT panel due to different environmental temperature.
- Estimated lifetime could vary on a different temperature and usually higher temperature could reduce the life significantly.

5.2 LED Circuit



BLU CIRCUIT DIAGRAM

LED Circuit Drawing

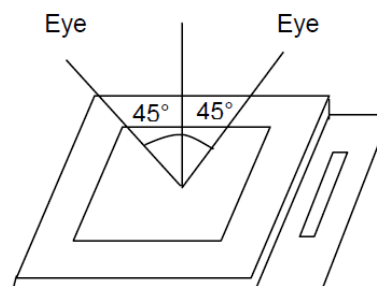
6.0 Quality Assurance Specification

6.1 Delivery Inspection Standards

6.1.1 Inspection Conditions

Inspection distance: 30 cm $\pm$ 2 cm

Viewing angle: $\pm 45^\circ$



6.1.2 Environmental Conditions

Ambient temperature: 25°C $\pm$ 5°C

Ambient humidity: 65 $\pm$ 10% RH

Ambient illumination: 300~700 lux

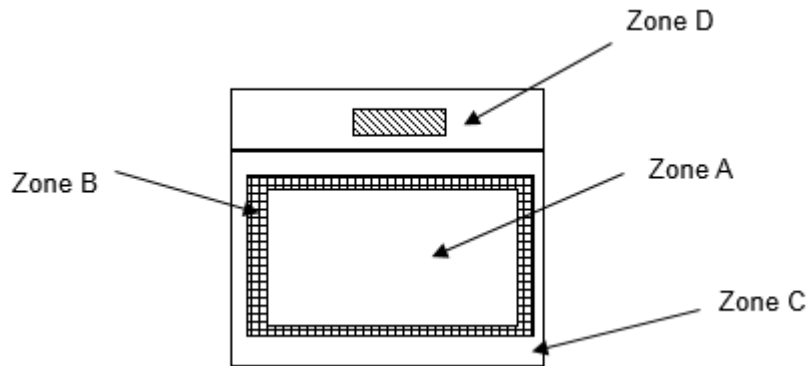
6.1.3 Sampling Conditions

1. Lot size: quantity of shipment lot per model
2. Sampling method:

Sampling Plan		GB/T 2828-2003
		Normal inspection, Class II
AQL	Major Defect	0.65%
	Minor Defect	1.5%

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot Line defect	Light dot , Dim spot,Polarizer Bubble ; Polarizer accidented spot.	
6	Soldering appearance	Good soldering , Peeling off is not allowed.	

6.1.4 Definition of Area



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Zone D : IC Bonding Area

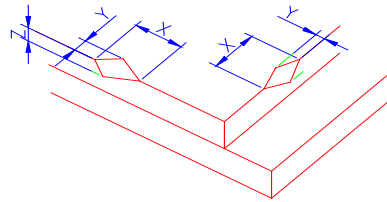
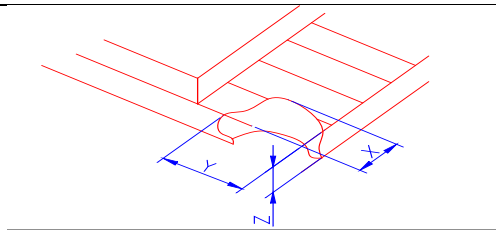
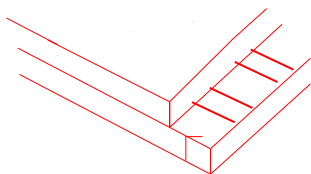
Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

6.1.5 Basic Principle

A set of sample to indicate the limit of acceptable quality level shall be discussed should a dispute occur.

6.1.6 Inspection Criteria

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of ITO, T: Height of LCD	(1) The edge of LCD broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
	X	Y	Z					
	≤3.0mm	<Inner border line of the seal	≤T					
(2)LCD corner broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	≤L	≤T	
X	Y	Z						
≤3.0mm	≤L	≤T						
(3) LCD crack	 Crack Not allowed							

2.0

Spot defect

① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain)

Zone Size (mm)	Acceptable Qty			
	A	B	C	
$\Phi \leq 0.10$	Ignore		Ignore	
$0.10 < \Phi \leq 0.25$	3(distance $\geq 10\text{mm}$)			
$0.25 < \Phi \leq 0.3$	2			
$\Phi > 0.35$	0			

② Dim spot (LCD/TP/Polarizer dim dot, light leakage、dark spot)

Zone Size (mm)	Acceptable Qty			
	A	B	C	
$\Phi \leq 0.1$	Ignore		Ignore	
$0.10 < \Phi \leq 0.25$	3(distance $\geq 10\text{mm}$)			
$0.25 < \Phi \leq 0.3$	2			
$\Phi > 0.35$	0			

③ Polarizer accidented spot

Zone Size (mm)	Acceptable Qty			
	A	B	C	
$\Phi \leq 0.2$	Ignore		Ignore	
$0.3 < \Phi \leq 0.5$	2(distance $\geq 10\text{mm}$)			
$\Phi > 0.5$	0			

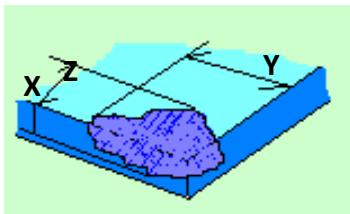
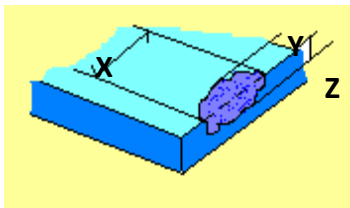
④ Pixel bad points (light dot , Dim dot, color dot)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.1$	Ignore	Ignore	
$0.15 < \Phi \leq 0.25$	2(distance $\geq 10\text{mm}$)		
$\Phi > 0.3$	0		

⑤ Polarizer Bubble

Zone Size (mm)	Acceptable Qty			
	A	B	C	
$\Phi \leq 0.2$	Ignore		Ignore	
$0.3 < \Phi \leq 0.4$	3(distance $\geq 10\text{m}$)			
$0.5 < \Phi \leq 0.6$	2			
$0.6 < \Phi$	0			

3.0	Line defect (LCD/TP /Polarizer backlight black/white line, scratch, stain)	Width(mm)		Length(mm)	Acceptable Qty		
					A	B	C
		Φ≤0.05		Ignore	Ignore		Ignore
		0.05<W≤0.06		L≤4.0	N≤3		
		0.07<W≤0.08		L≤3.0	N≤2		
0.08<W		Define as spot defect					
4.0	Electronic Components SMT	Not allow missing parts， solderless connection， cold solder joint， mismatch， The positive and negative polarity opposite					
5.0	Display color& Brightness	1. Color: Measuring the color coordinates, The measurement standard according to the datasheet or samples. 2. Brightness: Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.					
6.0	PCT Related	PCT Cover sensor accidented black/white spot	Size Φ(mm)	Acceptable Qty			
				A	B	C	
			Φ≤0.1	Ignore		Ignore	
			0.1<Φ≤0.2	3(distance ≥ 10mm)			
			0.20<Φ≤0.25	2			
		Φ > 0.3	0				
		PCT Cover scratch	Width(mm)	Ignore(mm)	Acceptable Qty		
					A	B	C
			Φ≤0.05	Ignore	Ignore		
			0.05<W≤0.06	L≤4.0	N≤3		
			0.07<W≤0.08	L≤3.0	N≤2		
		0.08<W	Define as spot defect				
		PCT Cover Pinhole/ Lack of ink	Zone Size (mm)	Acceptable Qty			
				C			
			Φ≤0.1	Ignore			
			0.1<Φ≤0.2	3(distance ≥ 10mm)			
			0.25<Φ≤0.3	2			
		Φ>0.35	0				
		PCT Bonding bubble/ accidented spot	Size Φ(mm)	Acceptable Qty			
				A		B	
			Φ≤0.1	Ignore			
			0.15<Φ≤0.2	3(distance ≥ 10mm)			
			0.2<Φ≤0.25	2			
		Φ>0.25	0				

		Assembly deflection	beyond the edge of backlight $\leq 0.2\text{mm}$								
		TP cover broken X : length Y : width Z : height	<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>$X \leq 0.5\text{mm}$</td><td>$Y \leq 0.5\text{mm}$</td><td>$Z < \text{cover thickness}$</td></tr></table>	X	Y	Z	$X \leq 0.5\text{mm}$	$Y \leq 0.5\text{mm}$	$Z < \text{cover thickness}$		
X	Y	Z									
$X \leq 0.5\text{mm}$	$Y \leq 0.5\text{mm}$	$Z < \text{cover thickness}$									
		TP cover broken X : length Y : width Z : height	<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>$X \leq 0.3\text{mm}$</td><td>$Y \leq 0.3\text{mm}$</td><td>$Z < \text{LCD thickness}$</td></tr></table>	X	Y	Z	$X \leq 0.3\text{mm}$	$Y \leq 0.3\text{mm}$	$Z < \text{LCD thickness}$		
X	Y	Z									
$X \leq 0.3\text{mm}$	$Y \leq 0.3\text{mm}$	$Z < \text{LCD thickness}$									

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

6.1.7 Classification of Defects

Visual defects (except no or wrong label) are treated as minor defects, while electrical defects are treated as major defects.

Two minor defects are equal to one major defect in lot sampling inspection.

6.1.8 Identification / marking criteria

Any unit with illegible / wrong / double or no marking / label shall be rejected.

6.2 Dealing with Customer Complaints

6.2.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample. After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.

If the analysis cannot be completed on time, Densitron must inform the purchaser.

6.2.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.

Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.

Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

7.0 Reliability Specification

7.1 Reliability Tests

Test Item		Test Condition		Sample Size
Durability Test	High Temperature Operation	Ta= 70°C	96h	3pcs
	Low Temperature Operation	Ta=-20°C	96h	3pcs
	High Temperature Storage	Tp= 80°C	96h	3pcs
	Low Temperature Storage	Tp= -30°C	96h	3pcs
	ESD Test	150pF, 330Ω, ±6KV (Contact)/±8KV (Air), 5 Points/panel, 10 times/point		3pcs
	Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: LTS for 30 minutes -> normal temperature for 5 minutes -> HTS for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours		3pcs
	Box Drop Test	1 Corner 3 Edges 6 faces, 80 cm (Medium Box)		1 box

Note: Ta=ambient temperature Tp= Panel temperature

Notes:

1. No dew condensation to be observed.
2. The function test shall be conducted after 4 hours storage at the normal temperature and humidity after removed from the test chamber.
3. No cosmetic or functional defects should be allowed.
4. Total current consumption should be less than twice the initial value.

8.0 Handling Precautions

Safety

If the LCD panel breaks, be careful not to get the liquid crystal fluid in your mouth or in your eyes.

If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design

Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.

When assembling with a zebra connector, clean the surface of the pads with alcohol and keep the surrounding air very clean.

Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during LCD cleaning

Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotrifluoroethane.

Do not wipe the display surface with dry or hard materials that will damage the polariser surface.

Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge

As the display uses C-MOS LSI drivers, connect any unused input terminal to VDD or VSS. Do not input any signals before power is turned on. Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging

Displays use LCD elements, and must be treated as such. Avoid strong shock and drop from a height. To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation

It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life. Direct current causes an electrochemical reaction with remarkable deterioration of the display quality. Give careful consideration to prevent direct current during ON/OFF timing and during operation. Response time is extremely delayed at temperatures lower than the operating temperature range while, at high temperatures, displays become dark. However, this phenomenon is reversible and does not mean a malfunction or a display that has been permanently damaged. If the display area is pushed on hard during operation, some graphics will be abnormally displayed but returns to a normal condition after turning off the display once. Even a small amount of condensation on the contact pads (terminals) can cause an electro-chemical reaction which causes missing rows and columns. Give careful attention to avoid condensation.

Storage

Store the display in a dark place where the temperature is $25^{\circ}\text{C} \pm 10^{\circ}\text{C}$ and the humidity below 50%RH. Store the display in a clean environment, free from dust, organic solvents and corrosive gases. Do not crash, shake or jolt the display (including accessories).