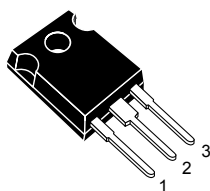
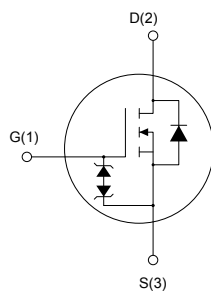


## N-channel 1200 V, 1.65 $\Omega$ typ., 6 A, MDmesh K5 Power MOSFET in a TO-247 package



TO-247



AM01476v1\_No\_label

### Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ | $P_{TOT}$ |
|------------|----------|-------------------|-------|-----------|
| STW8N120K5 | 1200 V   | 2.00 $\Omega$     | 6 A   | 130 W     |

- Industry's lowest  $R_{DS(on)}$  x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

#### Product status link

[STW8N120K5](#)

#### Product summary

|            |            |
|------------|------------|
| Order code | STW8N120K5 |
| Marking    | 8N120K5    |
| Package    | TO-247     |
| Packing    | Tube       |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol         | Parameter                                                         | Value      | Unit               |
|----------------|-------------------------------------------------------------------|------------|--------------------|
| $V_{GS}$       | Gate-source voltage                                               | $\pm 30$   | V                  |
| $I_D$          | Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$  | 6          | A                  |
|                | Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$ | 3.5        | A                  |
| $I_{DM}^{(1)}$ | Drain current pulsed                                              | 12         | A                  |
| $P_{TOT}$      | Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$           | 130        | W                  |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope                                 | 4.5        | V/ns               |
| $dv/dt^{(3)}$  | MOSFET $dv/dt$ ruggedness                                         | 50         |                    |
| $T_j$          | Operating junction temperature range                              | -55 to 150 | $^{\circ}\text{C}$ |
| $T_{stg}$      | Storage temperature range                                         |            |                    |

1. Pulse width limited by safe operating area
2.  $I_{SD} \leq 6\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ,  $V_{DS\text{ peak}} \leq V_{(BR)DSS}$
3.  $V_{DS} \leq 960\text{ V}$

**Table 2. Thermal data**

| Symbol         | Parameter                           | Value | Unit                        |
|----------------|-------------------------------------|-------|-----------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case    | 0.96  | $^{\circ}\text{C}/\text{W}$ |
| $R_{thj-amb}$  | Thermal resistance junction-ambient | 50    | $^{\circ}\text{C}/\text{W}$ |

**Table 3. Avalanche characteristics**

| Symbol   | Parameter                                                                                                                 | Value | Unit |
|----------|---------------------------------------------------------------------------------------------------------------------------|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive<br>(pulse width limited by $T_{jmax}$ )                                   | 1.7   | A    |
| $E_{AS}$ | Single-pulse avalanche energy<br>(starting $T_J = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 415   | mJ   |

## 2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

**Table 4. On-/off-states**

| Symbol        | Parameter                         | Test conditions                                                                                        | Min. | Typ. | Max.     | Unit          |
|---------------|-----------------------------------|--------------------------------------------------------------------------------------------------------|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$                                                            | 1200 |      |          | V             |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 1200\text{ V}$                                                       |      |      | 1        | $\mu\text{A}$ |
|               |                                   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 1200\text{ V}$<br>$T_C = 125\text{ }^{\circ}\text{C}$ <sup>(1)</sup> |      |      | 50       | $\mu\text{A}$ |
| $I_{GSS}$     | Gate body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$                                                     |      |      | $\pm 10$ | $\mu\text{A}$ |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$                                                     | 3    | 4    | 5        | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 2.5\text{ A}$                                                          |      | 1.65 | 2.00     | $\Omega$      |

1. Defined by design, not subject to production test.

**Table 5. Dynamic characteristics**

| Symbol            | Parameter                             | Test conditions                                                         | Min. | Typ. | Max. | Unit     |
|-------------------|---------------------------------------|-------------------------------------------------------------------------|------|------|------|----------|
| $C_{iss}$         | Input capacitance                     | $V_{DS} = 100\text{ V}$ , $V_{GS} = 0\text{ V}$ ,<br>$f = 1\text{ MHz}$ | -    | 505  | -    | pF       |
| $C_{oss}$         | Output capacitance                    |                                                                         | -    | 44   | -    | pF       |
| $C_{rss}$         | Reverse transfer capacitance          |                                                                         | -    | 0.4  | -    | pF       |
| $C_{o(tr)}^{(1)}$ | Time-related equivalent capacitance   | $V_{DS} = 0\text{ to }960\text{ V}$ , $V_{GS} = 0\text{ V}$             | -    | 70   | -    | pF       |
| $C_{o(er)}^{(2)}$ | Energy-related equivalent capacitance |                                                                         | -    | 24   | -    | pF       |
| $R_g$             | Intrinsic gate resistance             | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$                                 | -    | 7.7  | -    | $\Omega$ |
| $Q_g$             | Total gate charge                     | $V_{DD} = 960\text{ V}$ , $I_D = 5\text{ A}$                            | -    | 13.7 | -    | nC       |
| $Q_{gs}$          | Gate-source charge                    | $V_{GS} = 0\text{ to }10\text{ V}$                                      | -    | 3.6  | -    | nC       |
| $Q_{gd}$          | Gate-drain charge                     | (see Figure 14. Test circuit for gate charge behavior )                 | -    | 7.1  | -    | nC       |

- $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

| Symbol       | Parameter           | Test conditions                                                                                                                                                                                                   | Min. | Typ. | Max. | Unit |
|--------------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 600\text{ V}$ , $I_D = 2.5\text{ A}$ ,<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$<br>(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | -    | 15.5 | -    | ns   |
| $t_r$        | Rise time           |                                                                                                                                                                                                                   | -    | 11   | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time |                                                                                                                                                                                                                   | -    | 40   | -    | ns   |
| $t_f$        | Fall time           |                                                                                                                                                                                                                   | -    | 27   | -    | ns   |

**Table 7. Source-drain diode**

| Symbol          | Parameter                     | Test conditions                                                                                                                                                                                                   | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                                                                                                   | -    |      | 6    | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                                                                                                   | -    |      | 12   | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 5\text{ A}$ , $V_{GS} = 0\text{ V}$                                                                                                                                                                     | -    |      | 1.5  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 5\text{ A}$ , $V_{DD} = 60\text{ V}$ ,<br>$di/dt = 100\text{ A}/\mu\text{s}$<br>(see Figure 15. Test circuit for inductive load switching and diode recovery times)                                     | -    | 327  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                   | -    | 3    |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                   | -    | 18.4 |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 5\text{ A}$ , $V_{DD} = 60\text{ V}$ ,<br>$di/dt = 100\text{ A}/\mu\text{s}$ , $T_j = 150\text{ }^\circ\text{C}$<br>(see Figure 15. Test circuit for inductive load switching and diode recovery times) | -    | 485  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                   | -    | 3.9  |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                   | -    | 16   |      | A             |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

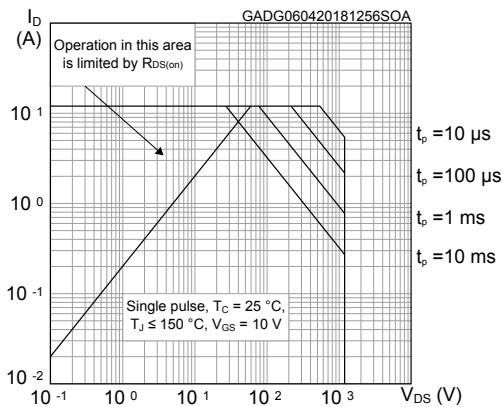
**Table 8. Gate-source Zener diode**

| Symbol        | Parameter                     | Test conditions                                 | Min.     | Typ. | Max | Unit |
|---------------|-------------------------------|-------------------------------------------------|----------|------|-----|------|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS} = \pm 1\text{ mA}$ , $I_D = 0\text{ A}$ | $\pm 30$ | -    | -   | V    |

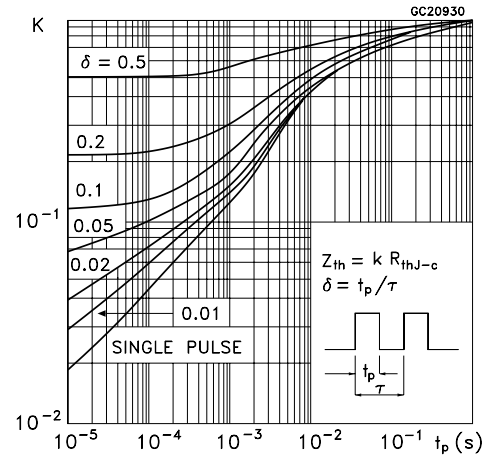
The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.1 Electrical characteristics (curves)

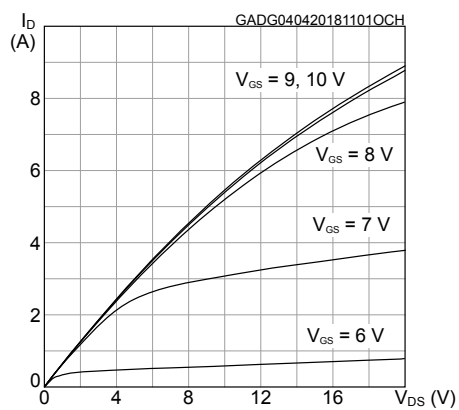
**Figure 1. Safe operating area**



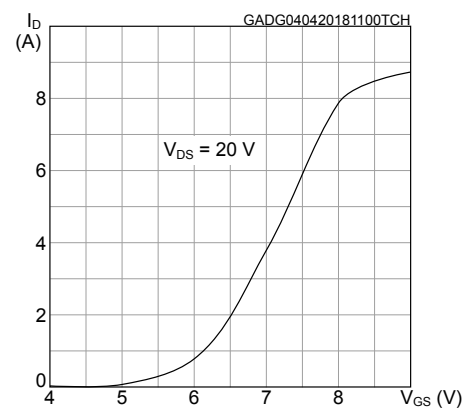
**Figure 2. Thermal impedance**



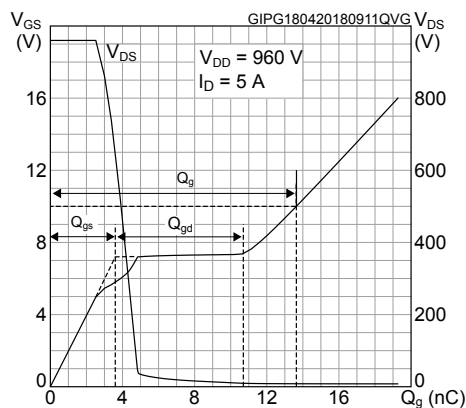
**Figure 3. Output characteristics**



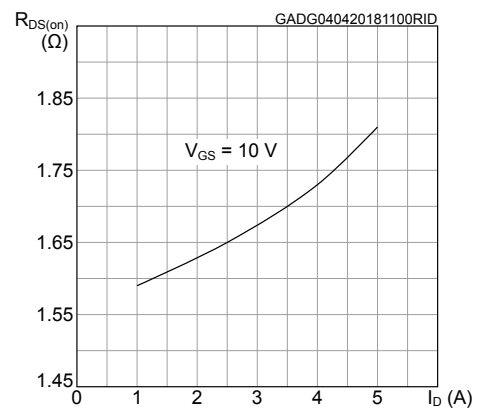
**Figure 4. Transfer characteristics**



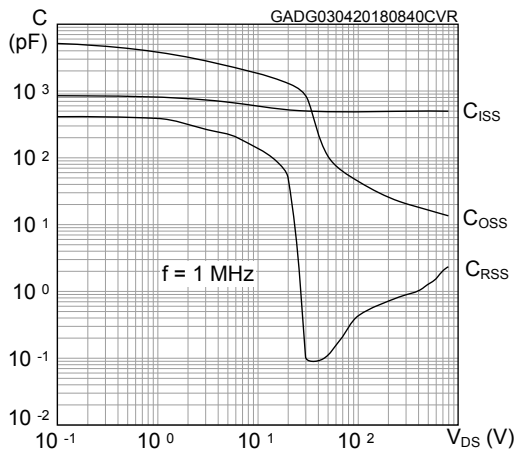
**Figure 5. Gate charge vs gate-source voltage**



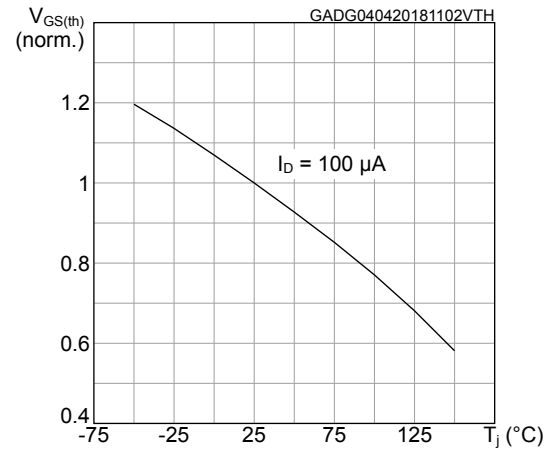
**Figure 6. Static drain-source on-resistance**



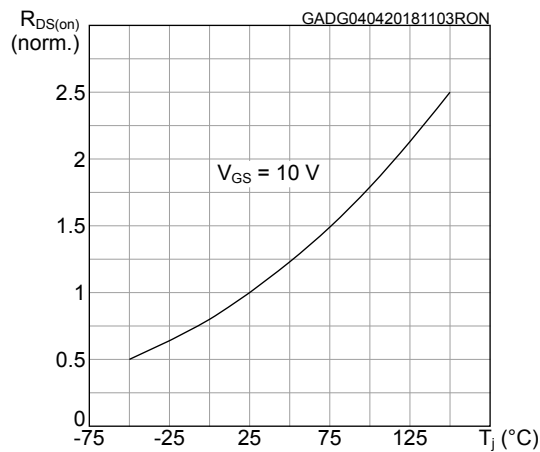
**Figure 7. Capacitance variations**



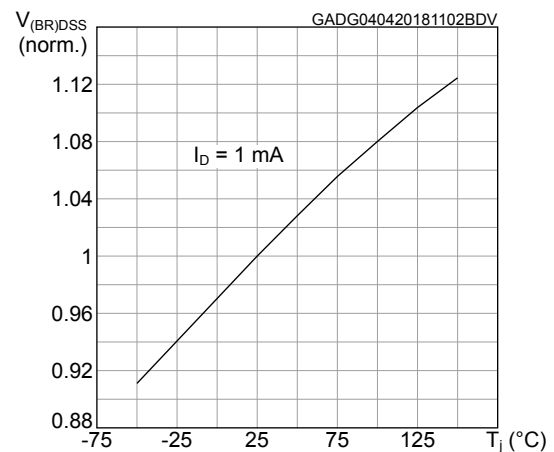
**Figure 8. Normalized gate threshold voltage vs temperature**



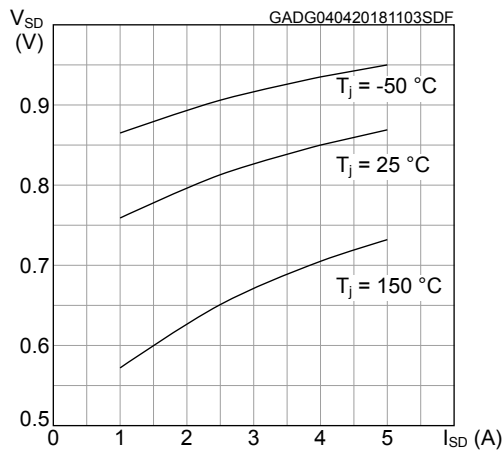
**Figure 9. Normalized on-resistance vs temperature**



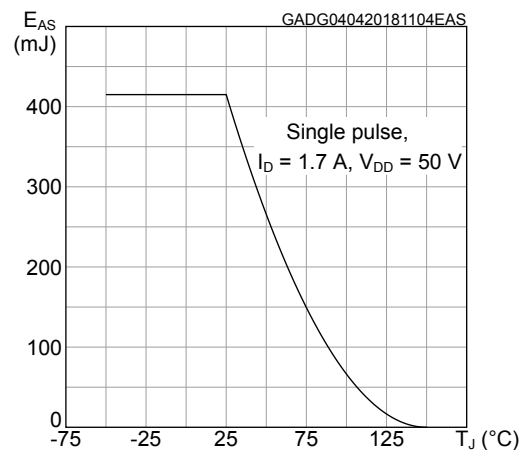
**Figure 10. Normalized  $V_{(BR)DSS}$  vs temperature**



**Figure 11. Source-drain diode forward characteristics**

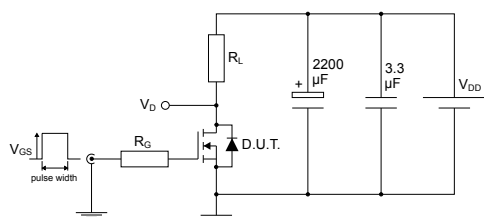


**Figure 12. Maximum avalanche energy vs starting  $T_J$**



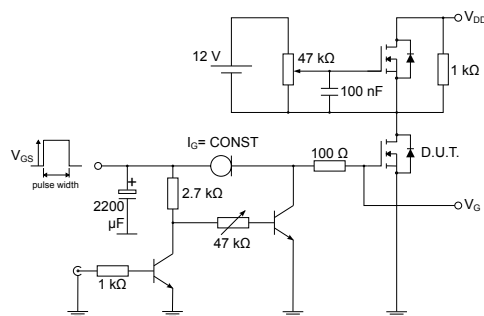
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**



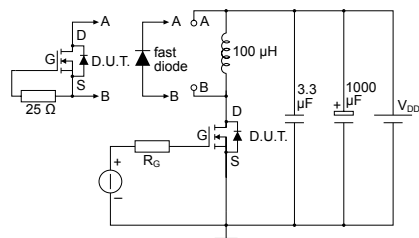
AM01468v1

**Figure 14. Test circuit for gate charge behavior**



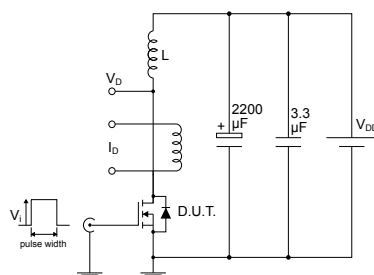
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**Figure 15. Test circuit for inductive load switching and diode recovery times**



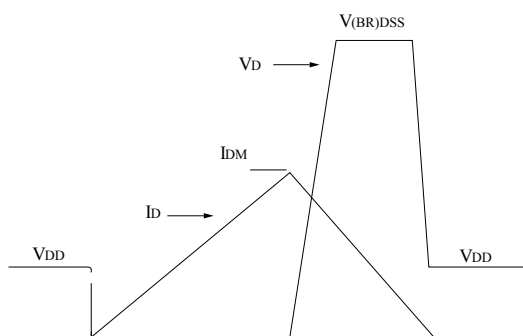
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**Figure 16. Unclamped inductive load test circuit**



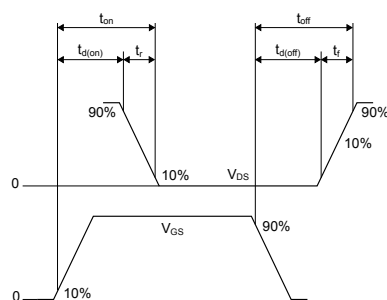
AM01471v1

**Figure 17. Unclamped inductive waveform**



AM01472v1

### Figure 18. Switching time waveform



AM01473v1

## **4 Package information**

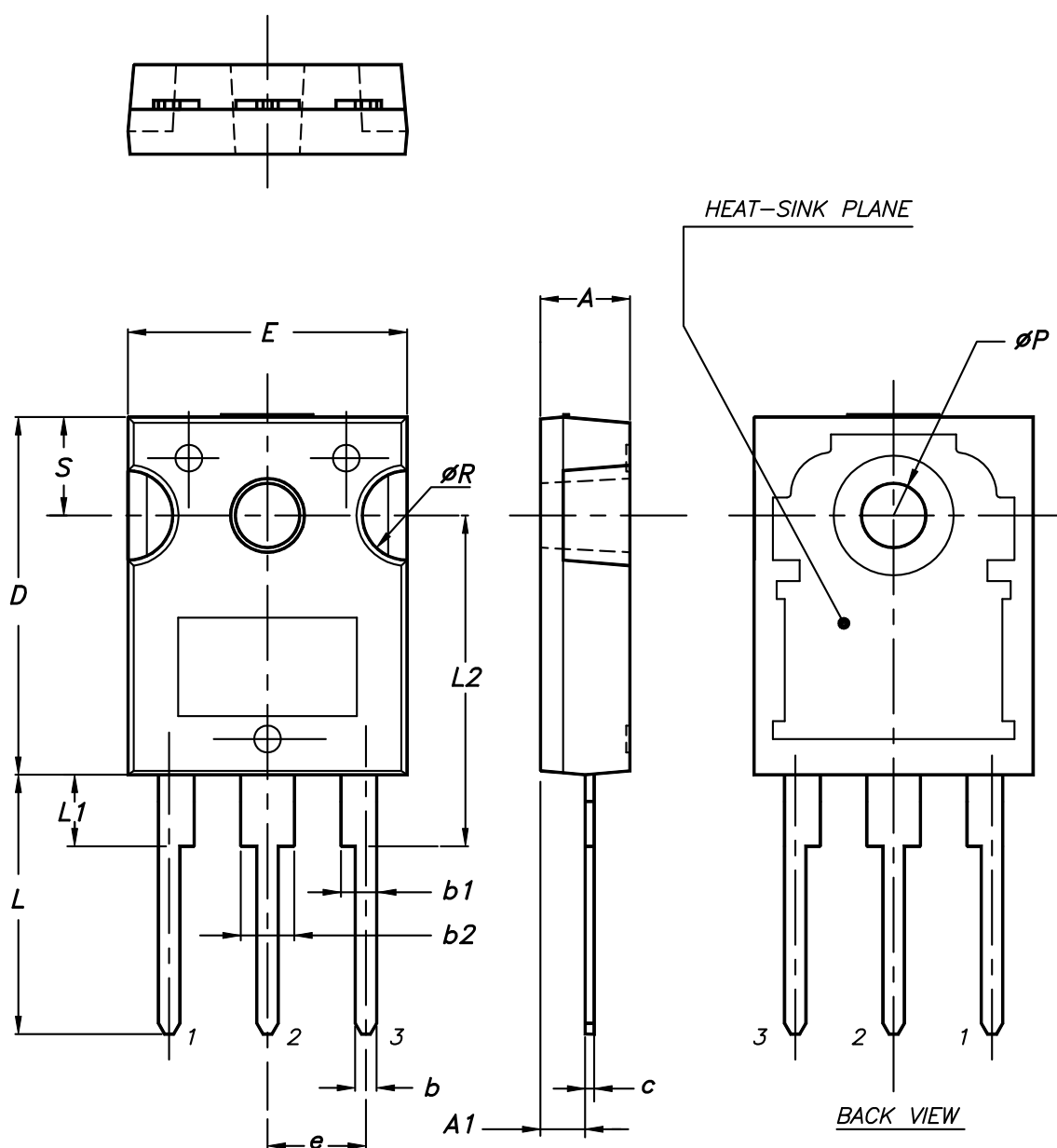
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## 4.1 TO-247 package information

Figure 19. TO-247 package outline



0075325\_9

**Table 9.** TO-247 package mechanical data

| Dim. | mm    |       |       |
|------|-------|-------|-------|
|      | Min.  | Typ.  | Max.  |
| A    | 4.85  |       | 5.15  |
| A1   | 2.20  |       | 2.60  |
| b    | 1.0   |       | 1.40  |
| b1   | 2.0   |       | 2.40  |
| b2   | 3.0   |       | 3.40  |
| c    | 0.40  |       | 0.80  |
| D    | 19.85 |       | 20.15 |
| E    | 15.45 |       | 15.75 |
| e    | 5.30  | 5.45  | 5.60  |
| L    | 14.20 |       | 14.80 |
| L1   | 3.70  |       | 4.30  |
| L2   |       | 18.50 |       |
| ØP   | 3.55  |       | 3.65  |
| ØR   | 4.50  |       | 5.50  |
| S    | 5.30  | 5.50  | 5.70  |

## Revision history

**Table 10. Document revision history**

| Date        | Version | Changes                                                                                                                                             |
|-------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 09-Apr-2018 | 1       | Initial release. The document status is preliminary data.                                                                                           |
| 17-Apr-2018 | 2       | Modified <a href="#">Table 5. Dynamic characteristics</a> and <a href="#">Figure 5. Gate charge vs gate-source voltage</a> .<br>Minor text changes. |
| 30-May-2018 | 3       | Document status promoted from preliminary to production data.                                                                                       |

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