

N-Channel Enhancement-Mode Vertical DMOS FET

Features

- Free from Secondary Breakdown
- Low Power Drive Requirement
- Ease of Paralleling
- Low C_{ISS} and Fast Switching Speeds
- Excellent Thermal Stability
- Integral Source-Drain Diode
- High Input Impedance and High Gain

Applications

- Logic-Level Interfaces (Ideal for TTL and CMOS)
- Solid-State Relays
- Battery-Operated Systems
- Photovoltaic Drives
- Analog Switches
- General Purpose Line Drivers
- Telecommunication Switches

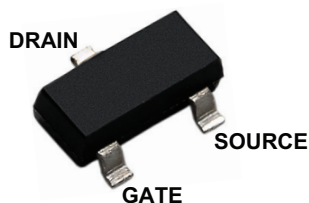
General Description

The TN2124 low-threshold Enhancement-mode (normally-off) transistor uses a vertical Diffusion Metal-Oxide Semiconductor (DMOS) structure and a well-proven silicon gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in Metal-Oxide Semiconductor (MOS) devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS Field-Effect Transistors (FETs) are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance and fast switching speeds are desired.

Package Type

3-lead SOT-23
(Top view)



See [Table 3-1](#) for pin information.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	$\pm 20V$
Operating Ambient Temperature, T_A	$-55^{\circ}C$ to $+150^{\circ}C$
Storage Temperature, T_S	$-55^{\circ}C$ to $+150^{\circ}C$

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $T_A = 25^{\circ}C$ unless otherwise specified. All DC parameters are 100% tested at $25^{\circ}C$ unless otherwise stated. Pulse test: 300 μs pulse, 2% duty cycle

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	240	—	—	V	$V_{GS} = 0V$, $I_D = 1\text{ mA}$
Gate Threshold Voltage	$V_{GS(th)}$	0.8	—	2	V	$V_{GS} = V_{DS}$, $I_D = 1\text{ mA}$
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	-5.5	mV/ $^{\circ}C$	$V_{GS} = V_{DS}$, $I_D = 1\text{ mA}$ (Note 1)
Gate Body Leakage Current	I_{GSS}	—	0.1	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
Zero-Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	$V_{GS} = 0V$, $V_{DS} = \text{Maximum rating}$
		—	—	100	μA	$V_{DS} = 0.8 \text{ Maximum rating}$, $V_{GS} = 0V$, $T_A = 125^{\circ}C$ (Note 1)
On-State Drain Current	$I_{D(ON)}$	140	—	—	mA	$V_{GS} = 4.5V$, $V_{DS} = 25V$
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	—	30	Ω	$V_{GS} = 3V$, $I_D = 25\text{ mA}$
		—	—	15	Ω	$V_{GS} = 4.5V$, $I_D = 120\text{ mA}$
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	0.7	1	%/ $^{\circ}C$	$V_{GS} = 4.5V$, $I_D = 120\text{ mA}$ (Note 1)

Note 1: Specification is obtained by characterization and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $T_A = 25^\circ\text{C}$ unless otherwise specified. Specification is obtained by characterization and is not 100% tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G_{FS}	100	170	—	mmho	$V_{DS} = 25\text{V}$, $I_D = 120\text{ mA}$
Input Capacitance	C_{ISS}	—	38	50	pF	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{ MHz}$
Common Source Output Capacitance	C_{OSS}	—	9	15	pF	
Reverse Transfer Capacitance	C_{RSS}	—	3	5	pF	
Turn-On Delay Time	$t_{d(ON)}$	—	4	7	ns	$V_{DD} = 25\text{V}$, $I_D = 140\text{ mA}$, $R_{GEN} = 25\Omega$
Rise Time	t_r	—	2	5	ns	
Turn-Off Delay Time	$t_{d(OFF)}$	—	7	10	ns	
Fall Time	t_f	—	9	12	ns	

DIODE PARAMETER

Diode Forward Voltage Drop	V_{SD}	—	—	1.8	V	$V_{GS} = 0\text{V}$, $I_{SD} = 120\text{ mA}$ (Note 1)
Reverse Recovery Time	t_{rr}	—	400	—	ns	$V_{GS} = 0\text{V}$, $I_{SD} = 120\text{ mA}$

Note 1: Unless otherwise stated, all DC parameters are 100% tested at $+25^\circ\text{C}$. Pulse test: 300 μs pulse, 2% duty cycle

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified, for all specifications $T_A = T_J = +25^\circ\text{C}$.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	-55	—	+150	$^\circ\text{C}$	
Storage Temperature	T_S	-55	—	+150	$^\circ\text{C}$	
PACKAGE THERMAL RESISTANCE						
3-lead SOT-23	θ_{JA}	—	203	—	$^\circ\text{C/W}$	

THERMAL CHARACTERISTICS

Package	I_D (Note 1) (Continuous) (mA)	I_D (Pulsed) (mA)	Power Dissipation at $T_A = 25^\circ\text{C}$ (W)	I_{DR} (Note 1) (mA)	I_{DRM} (mA)
3-lead SOT-23	134	250	0.36	134	250

Note 1: I_D (continuous) is limited by maximum T_J .

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

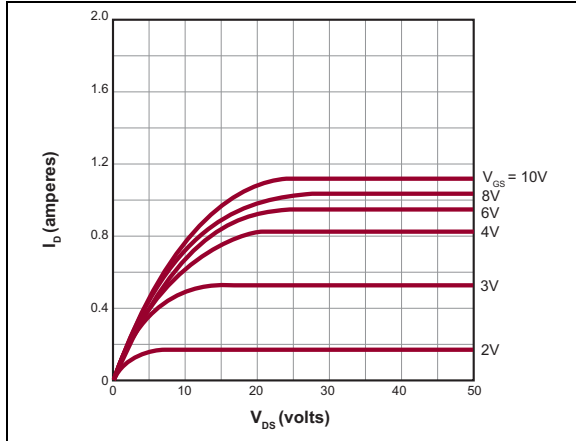


FIGURE 2-1: Output Characteristics.

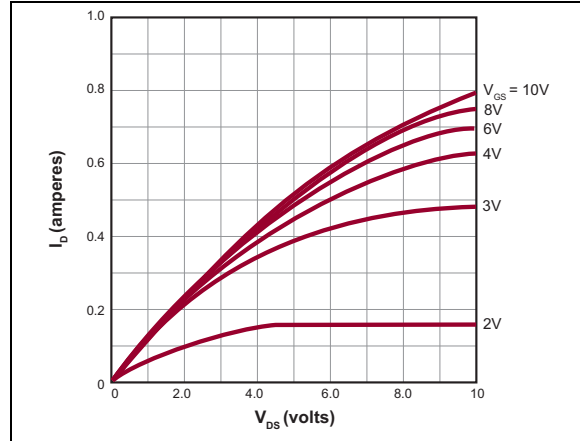


FIGURE 2-4: Saturation Characteristics.

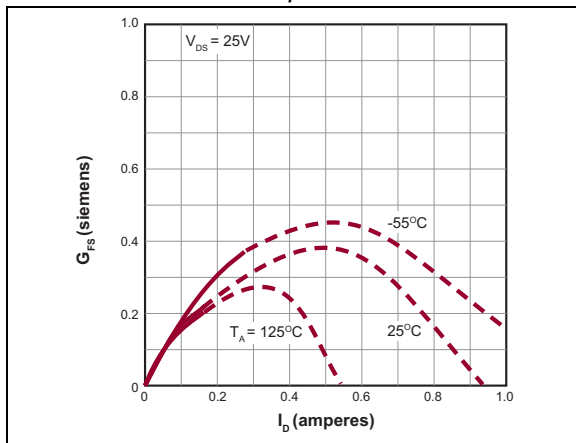


FIGURE 2-2: Transconductance vs. Drain Current.

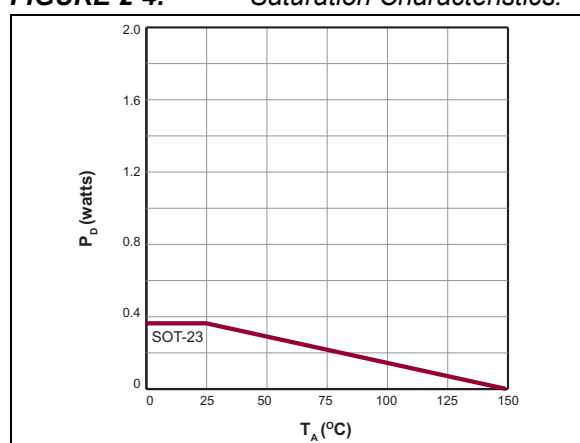


FIGURE 2-5: Power Dissipation vs. Temperature.

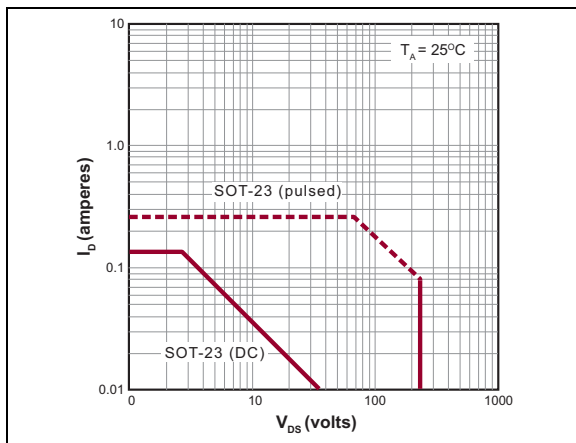


FIGURE 2-3: Maximum Rated Safe Operating Area.

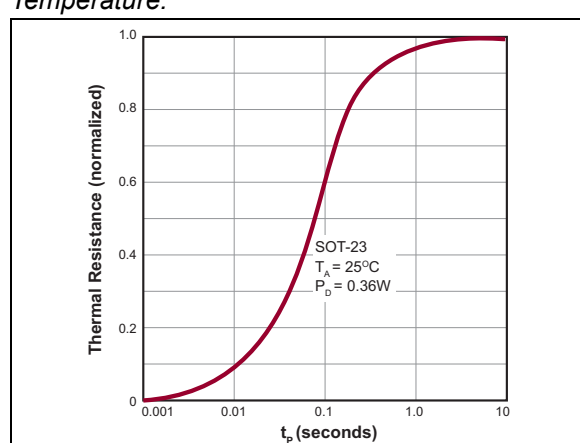


FIGURE 2-6: Thermal Response Characteristics.

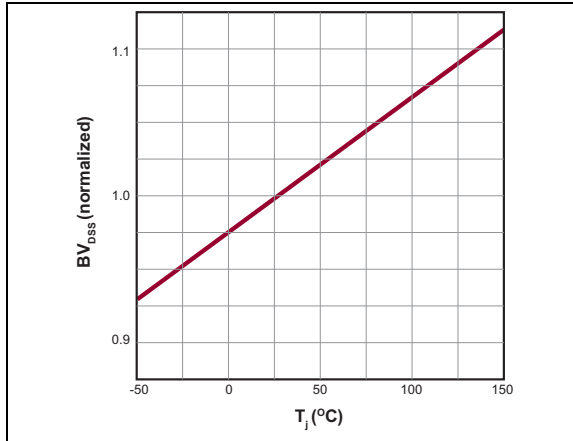


FIGURE 2-7: BV_{DSS} Variation with Temperature.

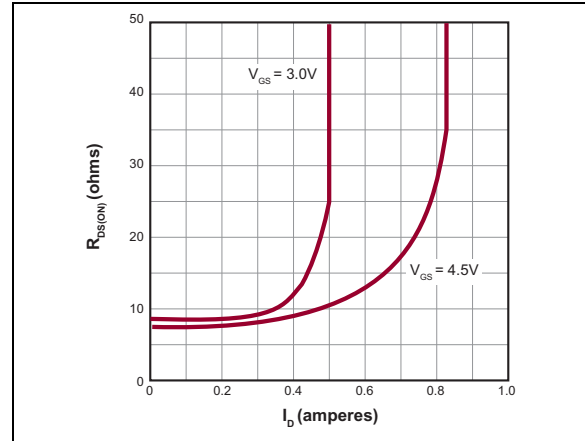


FIGURE 2-10: On-resistance vs. Drain Current.

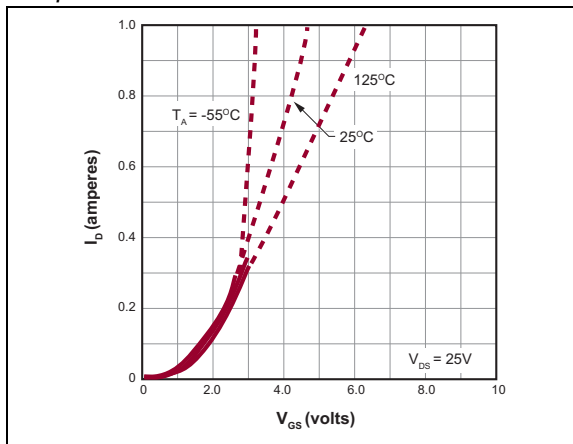


FIGURE 2-8: Transfer Characteristics.

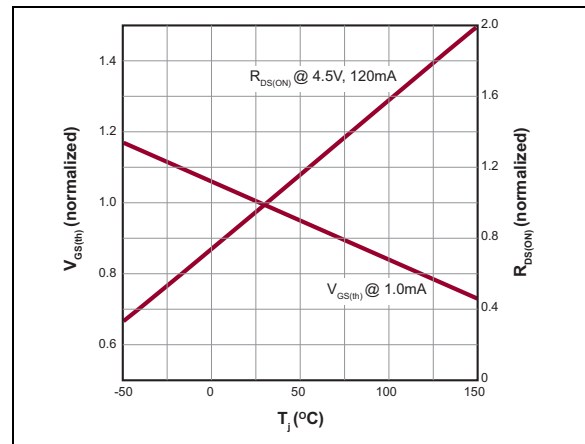


FIGURE 2-11: $V_{(th)}$ and R_{DS} Variation with Temperature.

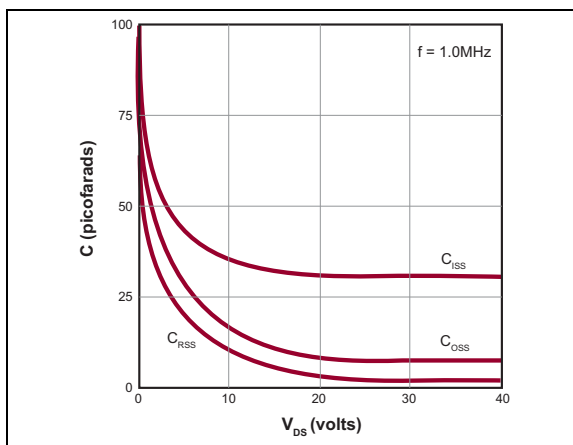


FIGURE 2-9: Capacitance vs. Drain-to-Source Voltage.

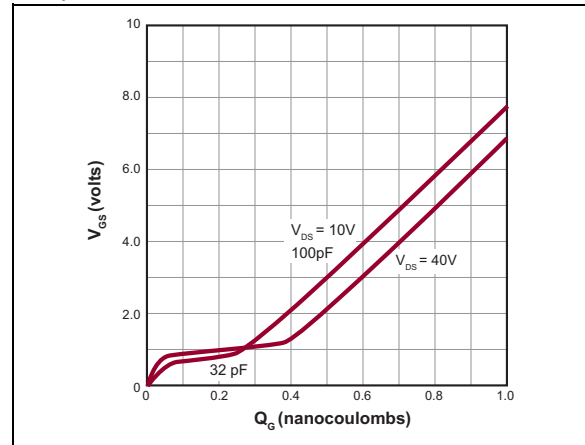


FIGURE 2-12: Gate Drive Dynamic Characteristics.

3.0 PIN DESCRIPTION

The details on the pins of TN2124 are listed on [Table 3-1](#). Refer to [Package Type](#) for the location of pins.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Gate	Gate
2	Source	Source
3	Drain	Drain

4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for TN2124.

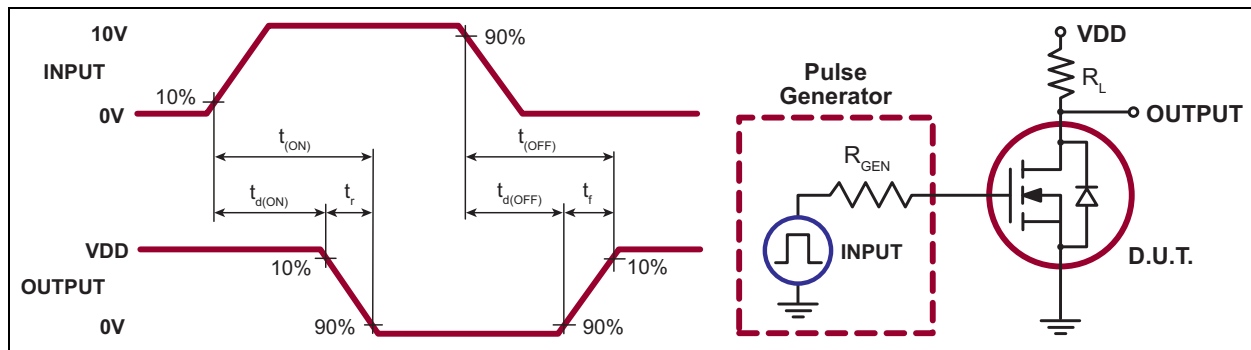


FIGURE 4-1: Switching Waveforms and Test Circuit.

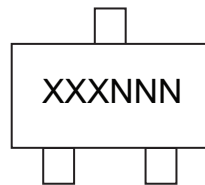
TABLE 4-1: PRODUCT SUMMARY

BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (Maximum) (Ω)	$V_{GS(th)}$ (Maximum) (V)
240	15	2

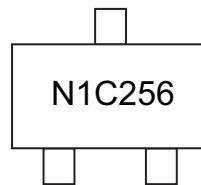
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

3-lead SOT-23



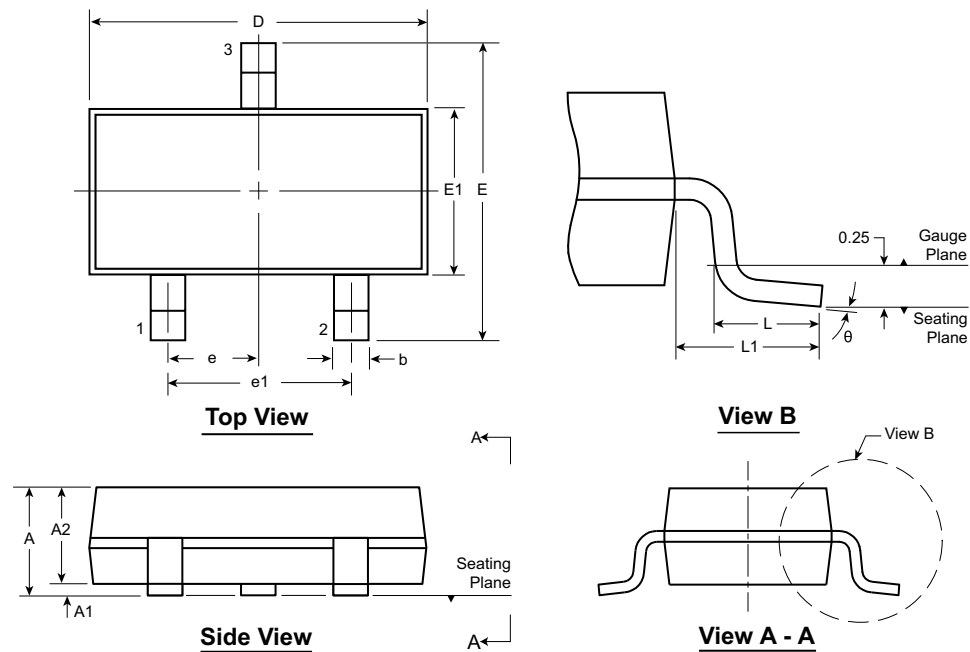
Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC [®] designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

3-Lead TO-236AB (SOT-23) Package Outline (K1/T) 2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	θ
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.20 [†]	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30			0.50		-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40			0.60		8°

JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.

[†] This dimension differs from the JEDEC drawing.

Drawings not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (April 2018)

- Converted Supertex Doc# DSFP-TN2124 to Microchip DS20005698A
- Added some sections to comply with the standard Microchip format
- Changed the package marking format
- Made minor text changes throughout the document

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ISBN: 978-1-5224-2937-1

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