



IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

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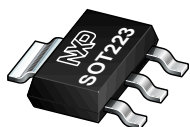
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Thank you for your cooperation and understanding,

WeEn Semiconductors



BT168GW

SCR

17 March 2014

Product data sheet

1. General description

Planar passivated SCR with sensitive gate in a SOT223 surface mountable plastic package. This SCR is designed to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Direct triggering from low power drivers and logic ICs
- Surface mountable package

3. Applications

- Circuit breakers
- RCD/GFI/LCCB applications

4. Quick reference data

Table 1. Quick reference data

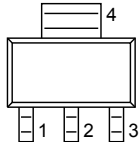
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		[1]	-	-	600	V
V_{RRM}	repetitive peak reverse voltage			-	-	600	V
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 10\text{ ms}$; Fig. 4; Fig. 5		-	-	8	A
$I_{\text{T(AV)}}$	average on-state current	half sine wave; $T_{\text{sp}} \leq 112\text{ }^{\circ}\text{C}$; Fig. 1		-	-	0.63	A
$I_{\text{T(RMS)}}$	RMS on-state current	half sine wave; $T_{\text{sp}} \leq 112\text{ }^{\circ}\text{C}$; Fig. 2; Fig. 3		-	-	1	A
Static characteristics							
I_{GT}	gate trigger current	$V_{\text{D}} = 12\text{ V}$; $I_{\text{T}} = 10\text{ mA}$; $T_{\text{j}} = 25\text{ }^{\circ}\text{C}$; Fig. 9		20	50	200	μA

[1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the thyristor may switch to the on-state.



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 SC-73 (SOT223)	 sym037
2	A	anode		
3	G	gate		
4	mb	mb; connected to anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT168GW	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		[1]	-	600	V
V_{RRM}	repetitive peak reverse voltage			-	600	V
$I_{\text{T(AV)}}$	average on-state current	half sine wave; $T_{\text{sp}} \leq 112\text{ }^{\circ}\text{C}$; Fig. 1		-	0.63	A
$I_{\text{T(RMS)}}$	RMS on-state current	half sine wave; $T_{\text{sp}} \leq 112\text{ }^{\circ}\text{C}$; Fig. 2 ; Fig. 3		-	1	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 10\text{ ms}$; Fig. 4 ; Fig. 5		-	8	A
		half sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 8.3\text{ ms}$		-	9	A
I^2t	I^2t for fusing	$t_{\text{p}} = 10\text{ ms}$; SIN		-	0.32	A^2s
di_{T}/dt	rate of rise of on-state current	$I_{\text{T}} = 2\text{ A}$; $I_{\text{G}} = 10\text{ mA}$; $di_{\text{G}}/dt = 100\text{ mA}/\mu\text{s}$		-	50	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current			-	1	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	2	W
$P_{\text{G(AV)}}$	average gate power	over any 20 ms period		-	0.1	W
T_{stg}	storage temperature			-40	150	$^{\circ}\text{C}$
T_{j}	junction temperature			-	125	$^{\circ}\text{C}$

[1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the thyristor may switch to the on-state.

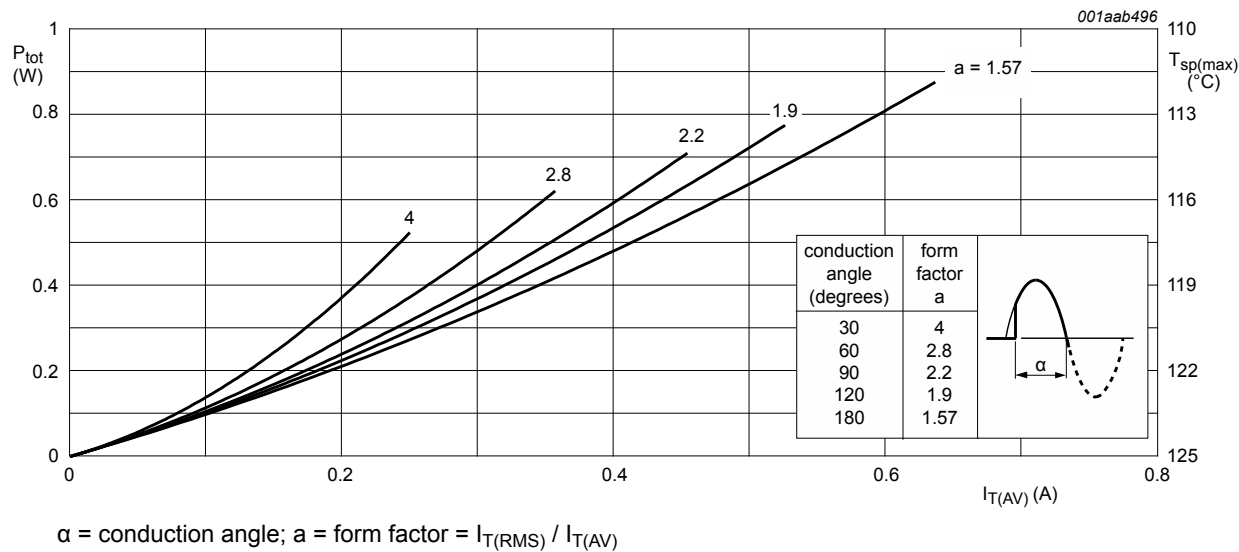


Fig. 1. Total power dissipation as a function of average on-state current; maximum values

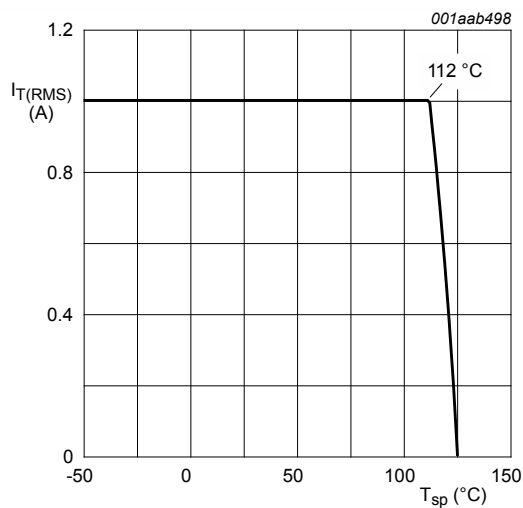
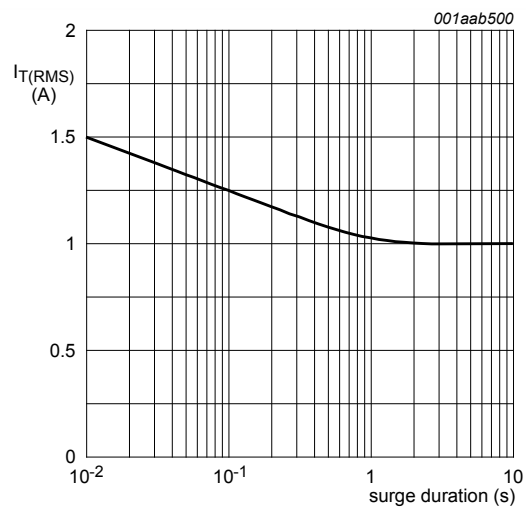


Fig. 2. RMS on-state current as a function of solder point temperature; maximum values



$f = 50 \text{ Hz}$; $T_{sp} = 112 \text{ }^{\circ}C$

Fig. 3. RMS on-state current as a function of surge duration; maximum values

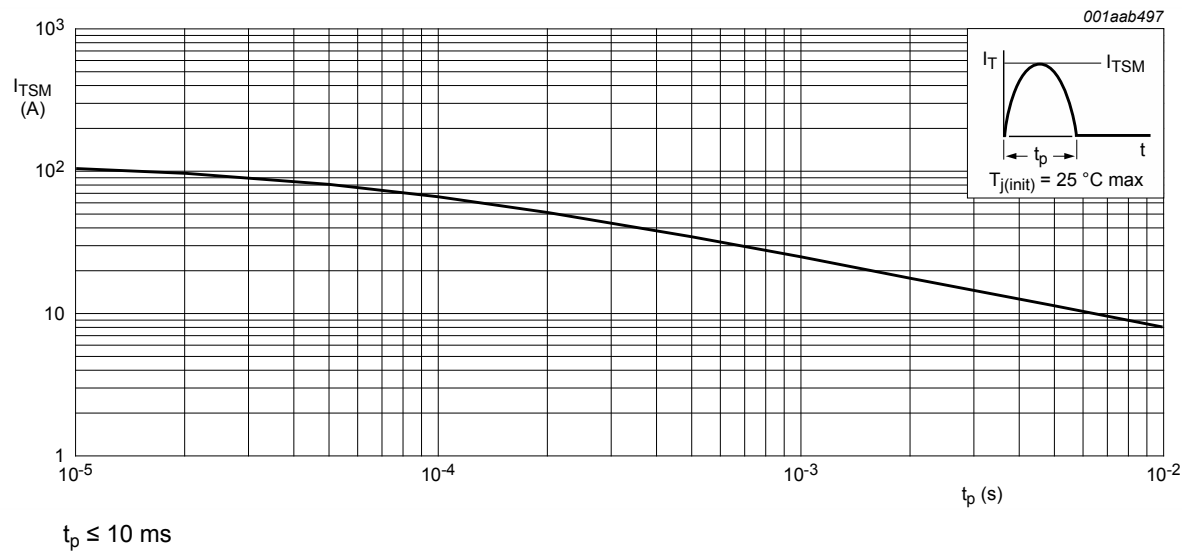


Fig. 4. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

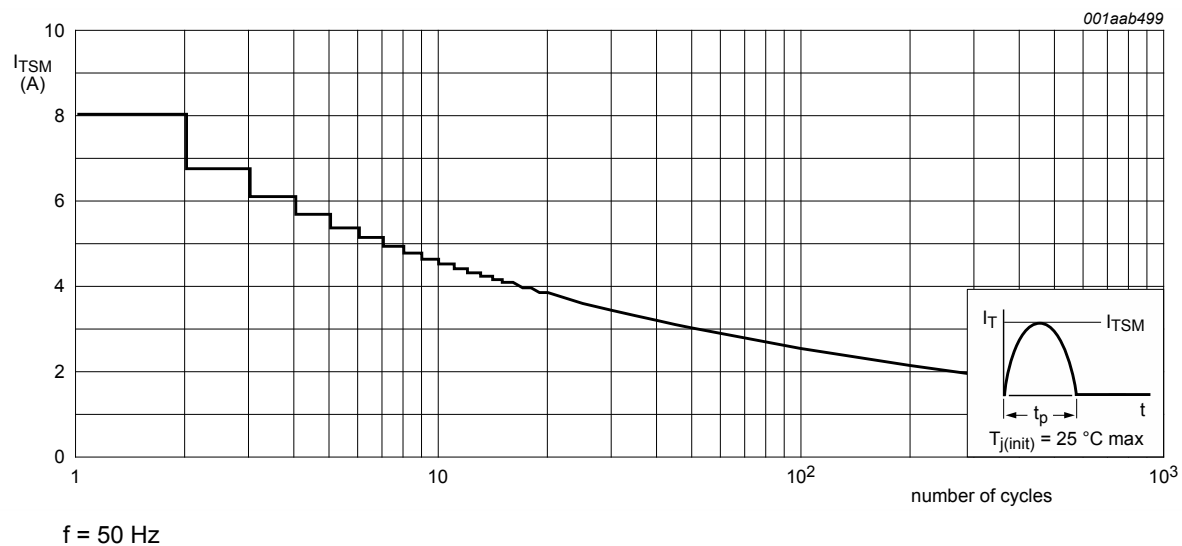
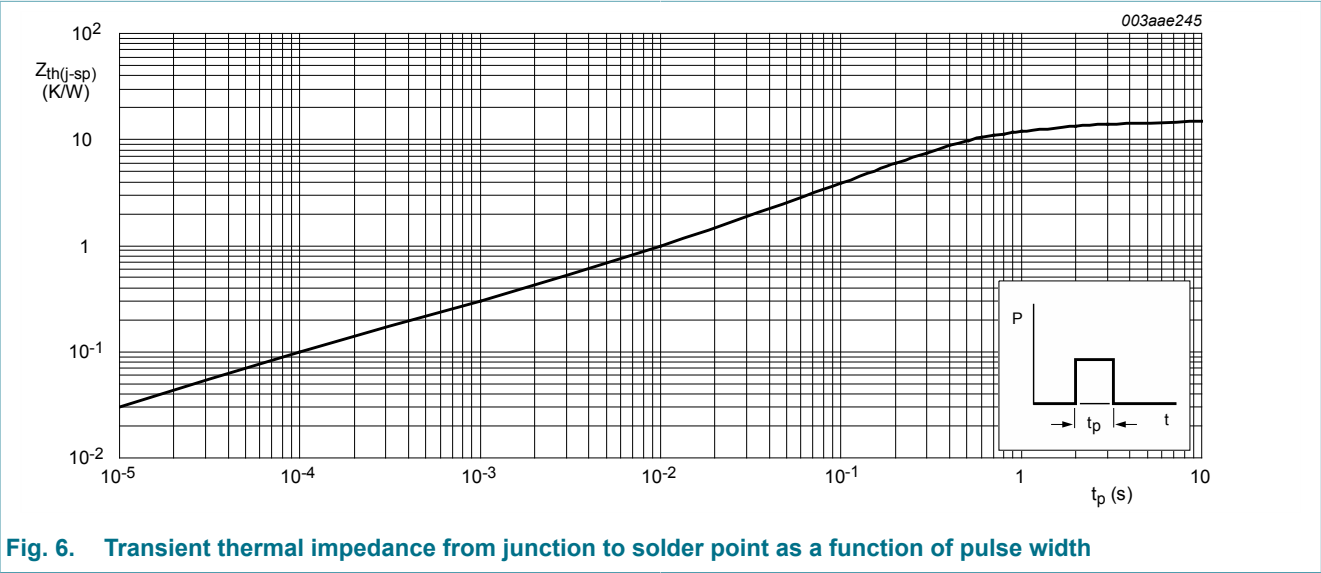


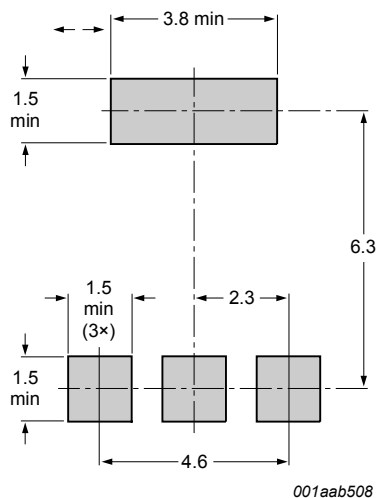
Fig. 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

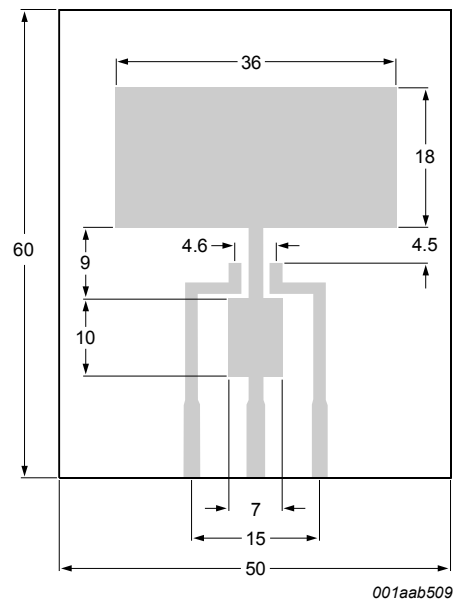
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Fig. 6		-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed circuit board mounted; minimum footprint; Fig. 7		-	156	-	K/W
		printed circuit board mounted; pad area; Fig. 8		-	70	-	K/W





All dimensions are in mm

Fig. 7. Minimum footprint SOT223



All dimensions are in mm

Printed circuit board:

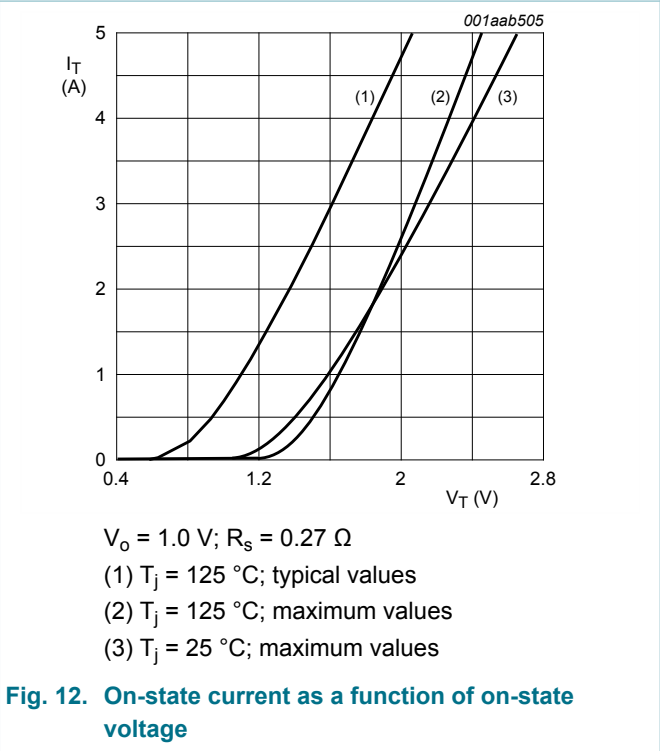
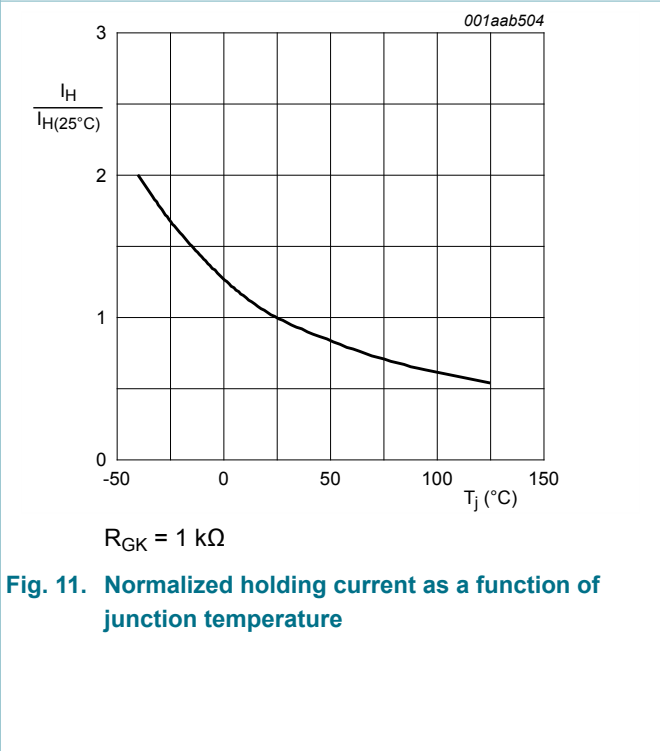
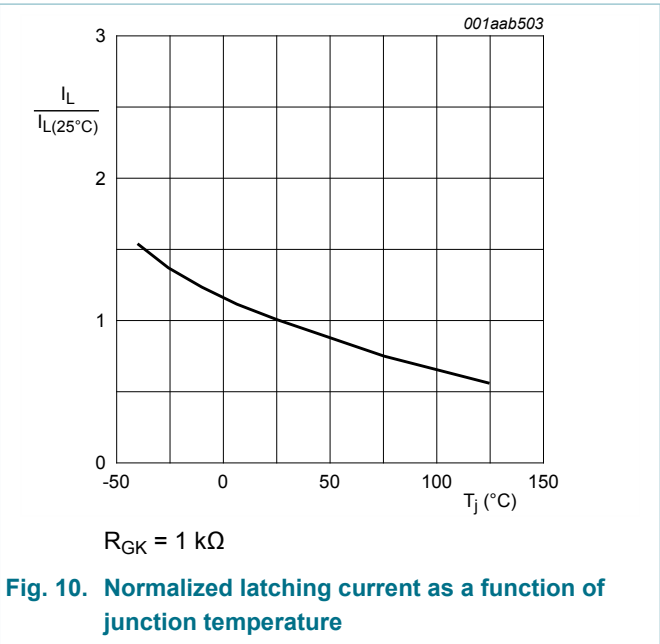
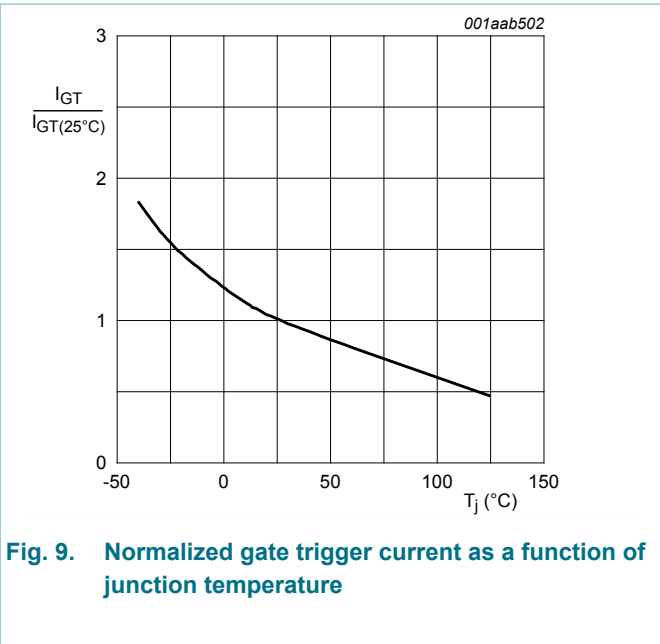
FR4 epoxy glass (1.6 mm thick), copper laminate
(35 µm thick)

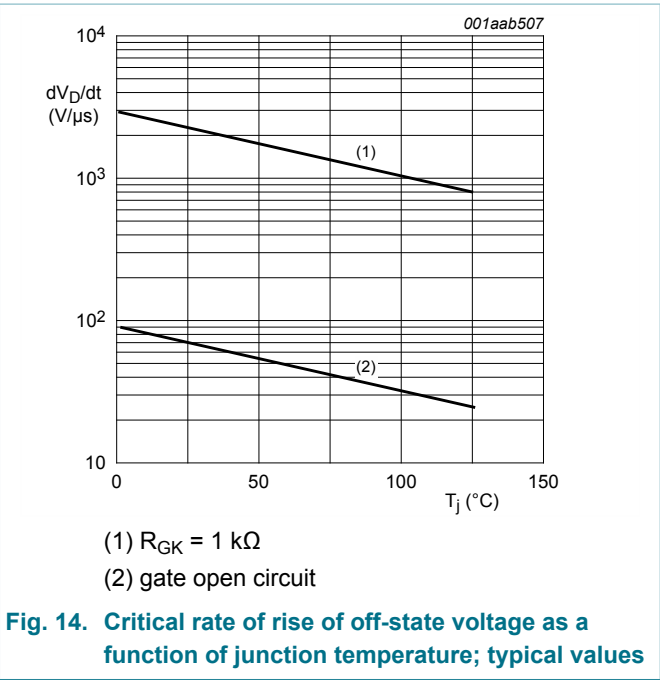
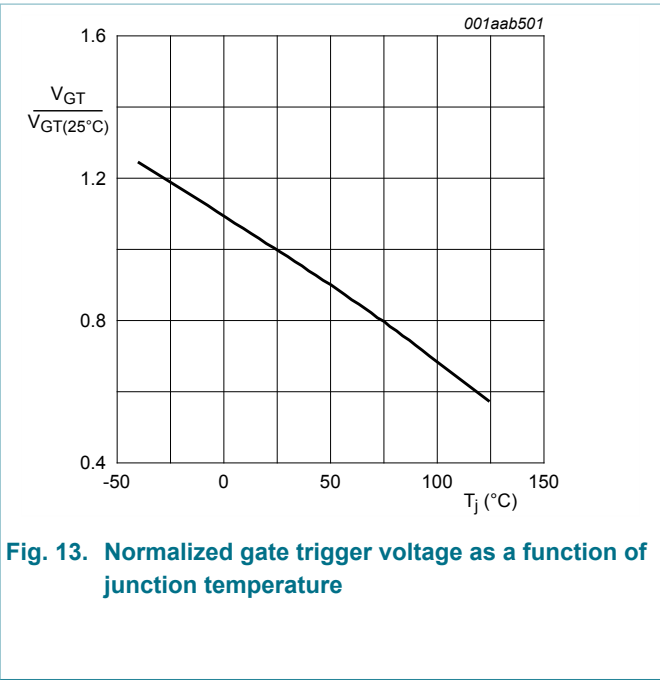
Fig. 8. Printed circuit board pad area: SOT223

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 25\text{ °C}$; Fig. 9	20	50	200	μA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.5\text{ mA}$; $R_{GK} = 1\text{ k}\Omega$; $T_j = 25\text{ °C}$; Fig. 10	-	2	6	mA
I_H	holding current	$V_D = 12\text{ V}$; $R_{GK} = 1\text{ k}\Omega$; $T_j = 25\text{ °C}$; Fig. 11	-	2	5	mA
V_T	on-state voltage	$I_T = 1.2\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12	-	1.25	1.7	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 25\text{ °C}$; Fig. 13	-	0.5	0.8	V
		$V_D = 600\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 125\text{ °C}$	0.2	0.3	-	V
I_D	off-state current	$V_D = 600\text{ V}$; $T_j = 125\text{ °C}$; $R_{GK} = 1\text{ k}\Omega$	-	0.05	0.1	mA
I_R	reverse current	$V_R = 600\text{ V}$; $T_j = 125\text{ °C}$; $R_{GK} = 1\text{ k}\Omega$	-	0.05	0.1	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ °C}$; $R_{GK} = 1\text{ k}\Omega$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; Fig. 14	500	800	-	V/ μs
		$V_{DM} = 402\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit; Fig. 14	-	25	-	V/ μs
t_{gt}	gate-controlled turn-on time	$I_{TM} = 2\text{ A}$; $V_D = 600\text{ V}$; $I_G = 10\text{ mA}$; $dI_G/dt = 0.1\text{ A}/\mu\text{s}$; $T_j = 25\text{ °C}$	-	2	-	μs
t_q	commutated turn-off time	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ °C}$; $I_{TM} = 1.6\text{ A}$; $V_R = 35\text{ V}$; $(dI_T/dt)_M = 30\text{ A}/\mu\text{s}$; $dV_D/dt = 2\text{ V}/\mu\text{s}$; $R_{GK} = 1\text{ k}\Omega$; ($V_{DM} = 67\%$ of V_{DRM})	-	100	-	μs





10. Package outline

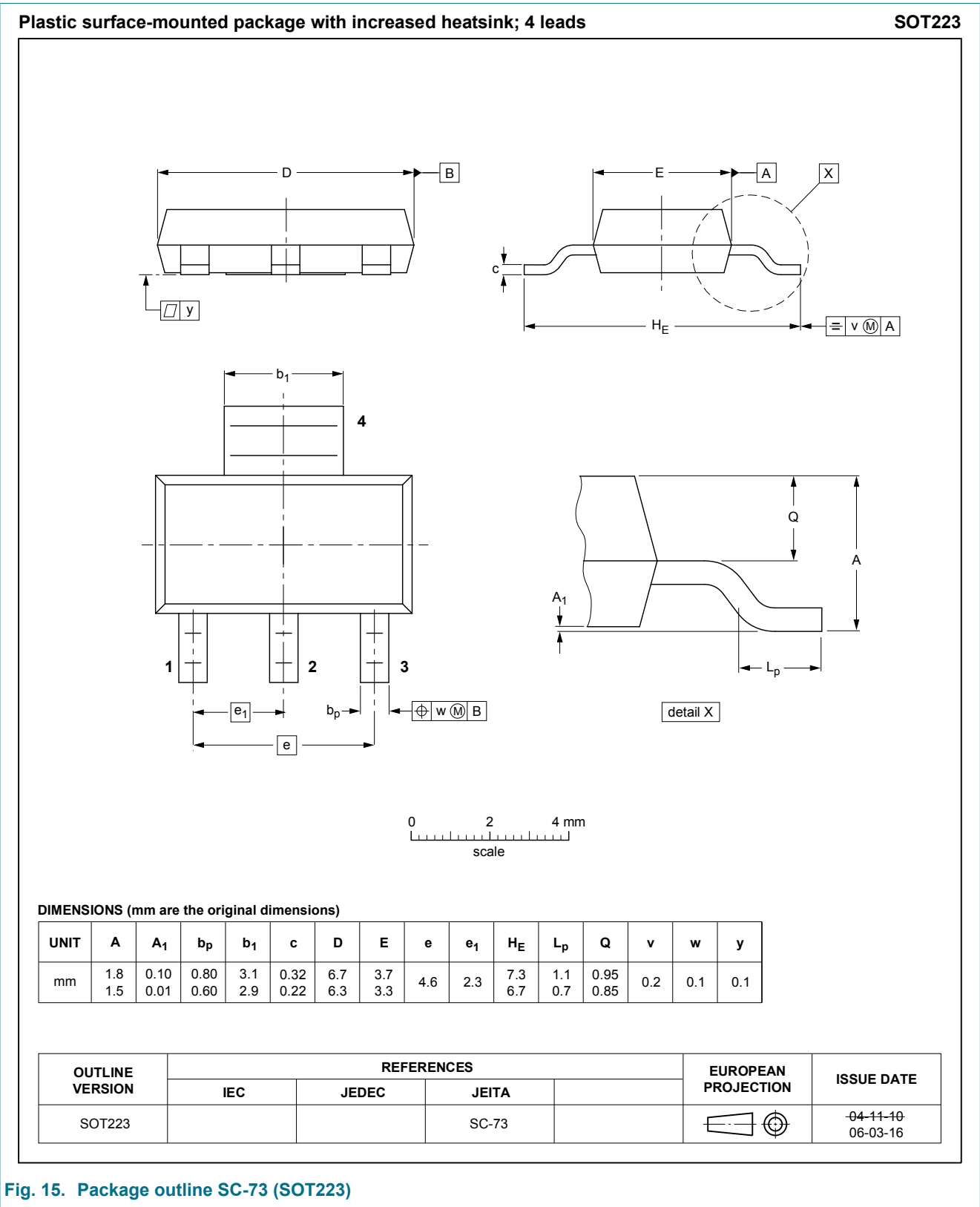


Fig. 15. Package outline SC-73 (SOT223)

11. Soldering

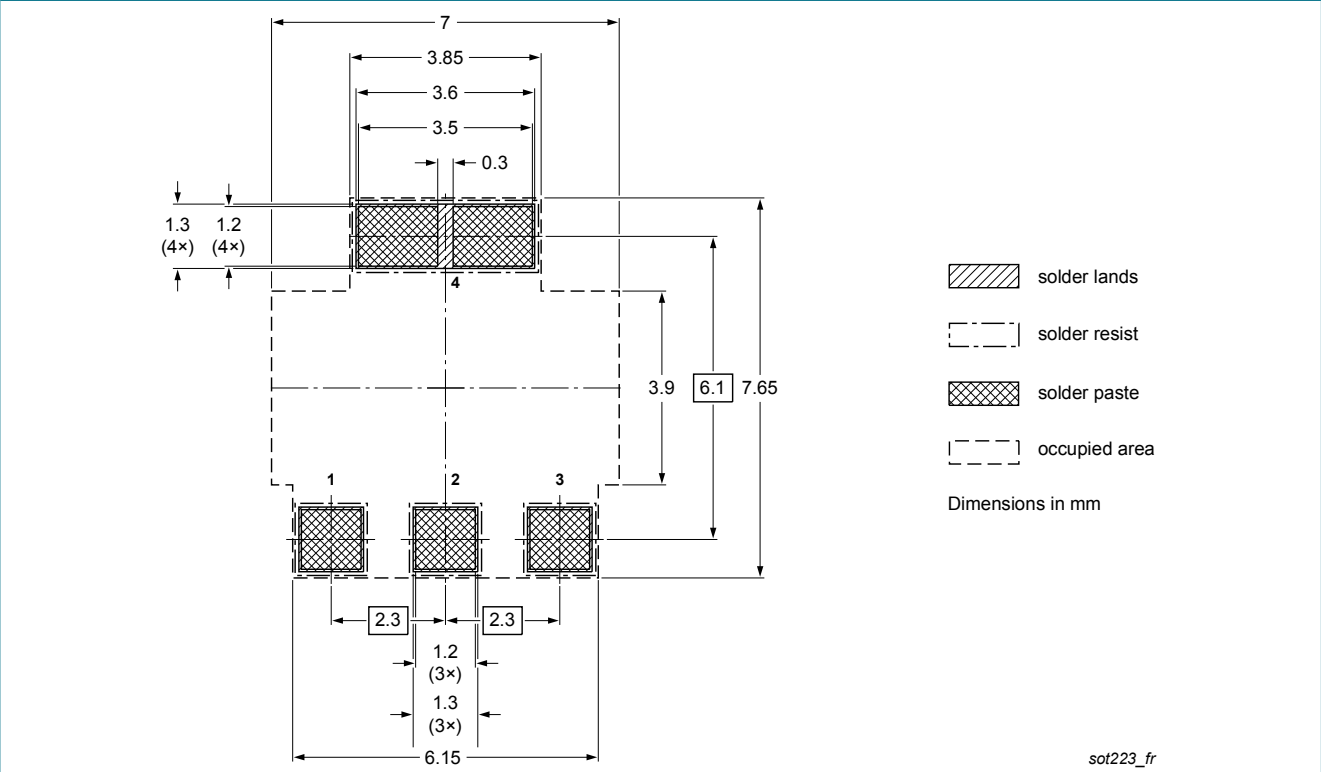


Fig. 16. Reflow soldering footprint for SC-73 (SOT223)

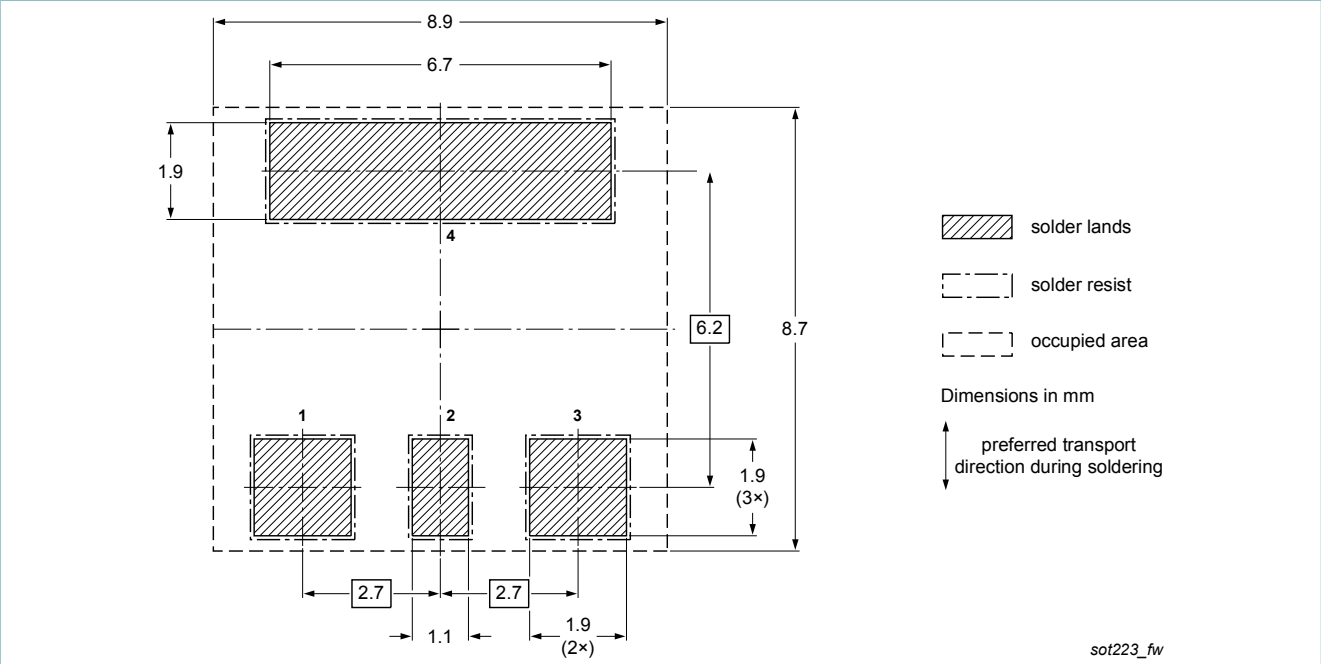


Fig. 17. Wave soldering footprint for SC-73 (SOT223)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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13. Contents

1 General description 1

2 Features and benefits 1

3 Applications 1

4 Quick reference data 1

5 Pinning information 2

6 Ordering information 2

7 Limiting values 3

8 Thermal characteristics 6

9 Characteristics 8

10 Package outline 11

11 Soldering 12

12 Legal information 13

12.1 Data sheet status 13

12.2 Definitions 13

12.3 Disclaimers 13

12.4 Trademarks 14

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Date of release: 17 March 2014