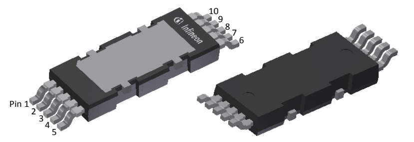
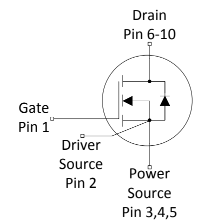
MOSFET

600V CoolMOS™ G7 Power Transistor

The C7 GOLD series (G7) for the first time brings together the benefits of the C7 GOLD CoolMOS™ technology, 4 pin Kelvin Source capability and the improved thermal properties of the DDPAK package to enable a possible SMD solution for high current topologies such as PFC up to 3kW.

PG-HDSOP-10-1





Features

- C7 Gold gives best in class FOM $R_{DS(on)}$*E_{oss} and $R_{DS(on)}$*Q_g.
- Suitable for hard and soft switching (PFC and high performance LLC)
- C7 Gold technology enables best in class $R_{DS(on)}$ in smallest footprint.
- DDPAK package has inbuilt 4th pin Kelvin Source configuration and low parasitic source inductance (~3nH).
- DDPAK package is MSL1 compliant, total Pb-free, has easy visual inspection leads and is qualified for industrial applications according to JEDEC 47/20/22.
- DDPAK SMD package combined with lead free die attach process enables improved thermal performance (R_{th}).

Benefits

- C7 Gold FOM $R_{DS(on)}$*Q_g is 15% better than previous C7 600V enabling faster switching leading to higher efficiency.
- Possibility to increasse economies of scales by usage in PFC and PWM topologies in the application.
- C7 Gold can reach 50mΩ in DDPAK 115mm^2 footprint, whereas previous BIC C7 600V was 40mΩ in 150mm^2 D^{2}PAK footprint.
- Reducing parasitic source inductance by Kelvin Source improves efficiency by faster switching and ease of use due to less ringing.
- DDPAK package is easy to use and has the highest quality standards.
- Improved thermals enable SMD DDPAK package to be used in higher current designs than has been previously possible.

Potential applications

PFC stages and PWM stages (TTF, LLC) for high power/performance SMPS e.g. Computing, Server, Telecom, UPS and Solar.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}@$T_{j,max}$	650	V
$R_{DS(on),max}$	190	mΩ
$Q_{g,typ}$	18	nC
$I_{D,pulse}$	36	A
$I_{D,continuous}$ @ T_j<150°C	19	A
E_{oss}@400V	2.17	µJ
Body diode di/dt	680	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPDD60R190G7	PG-HDSOP-10	60R190G7	see Appendix A

Table of Contents

1 Maximum ratings

at T_j=25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1)]	I_D	- -	- -	13 8	A	T_C=25°C T_C=100°C
Pulsed drain current[2)]	$I_{D,pulse}$	-	-	36	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	42	mJ	I_D=2.8A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.21	mJ	I_D=2.8A; V_{DD}=50V; see table 10
Avalanche current, single pulse	I_{AS}	-	-	2.8	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	76	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55	-	150	°C	-
Mounting torque	-	-	-	n.a.	Ncm	-
Continuous diode forward current	I_S	-	-	13	A	T_C=25°C
Diode pulse current[2)]	$I_{S,pulse}$	-	-	36	A	T_C=25°C
Reverse diode dv/dt[3)]	dv/dt	-	-	25	V/ns	V_{DS}=0...400V, I_{SD}<=4.3A, T_j=25°C see table 8
Maximum diode commutation speed	di_f/dt	-	-	680	A/µs	V_{DS}=0...400V, I_{SD}<=4.3A, T_j=25°C see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C=25°C, t=1min

1) Limited by $T_{j,max}$
2) Pulse width t_p limited by $T_{j,max}$
3) Identical low side and high side switch

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.65	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Reflow soldering temperature	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	V_{DS}=V_{GS}, I_D=0.21mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=600V, V_{GS}=0V, T_j=25°C V_{DS}=600V, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.164 0.409	0.190 -	Ω	V_{GS}=10V, I_D=4.2A, T_j=25°C V_{GS}=10V, I_D=4.2A, T_j=150°C
Gate resistance	R_G	-	0.9	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	718	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}	-	15	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Effective output capacitance, energy related[1]	$C_{o(er)}$	-	27	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[2]	$C_{o(tr)}$	-	277	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	16	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=4.2A, R_G=10Ω; see table 9
Rise time	t_r	-	5	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=4.2A, R_G=10Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	52	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=4.2A, R_G=10Ω; see table 9
Fall time	t_f	-	6.5	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=4.2A, R_G=10Ω; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	4	-	nC	V_{DD}=400V, I_D=4.2A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	7	-	nC	V_{DD}=400V, I_D=4.2A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	18	-	nC	V_{DD}=400V, I_D=4.2A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.0	-	V	V_{DD}=400V, I_D=4.2A, V_{GS}=0 to 10V

[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.8	-	V	V_{GS}=0V, I_F=4.2A, T_j=25°C
Reverse recovery time	t_{rr}	-	235	-	ns	V_R=400V, I_F=4.2A, di_F/dt=100A/µs; see table 8
Reverse recovery charge	Q_{rr}	-	2	-	µC	V_R=400V, I_F=4.2A, di_F/dt=100A/µs; see table 8
Peak reverse recovery current	I_{rrm}	-	18	-	A	V_R=400V, I_F=4.2A, di_F/dt=100A/µs; see table 8

4 Electrical characteristics diagrams

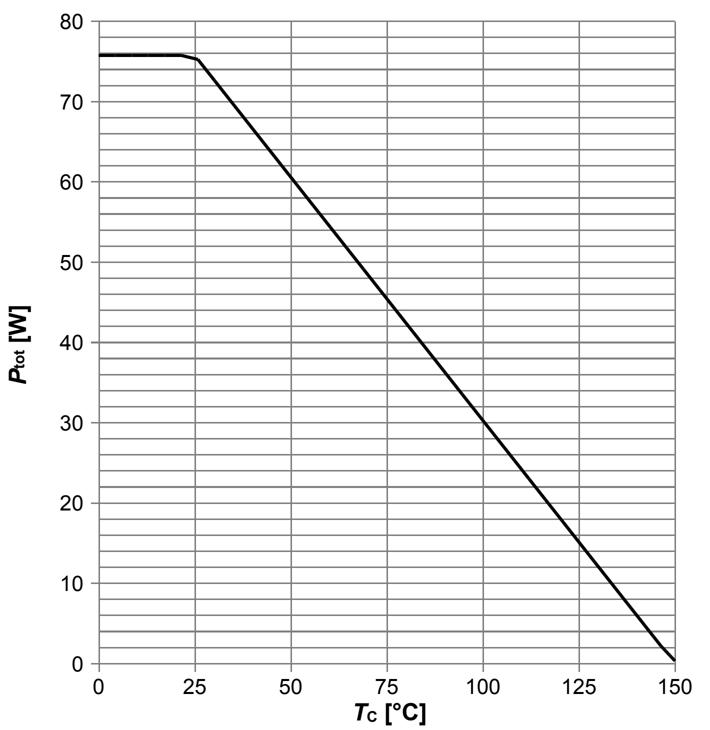
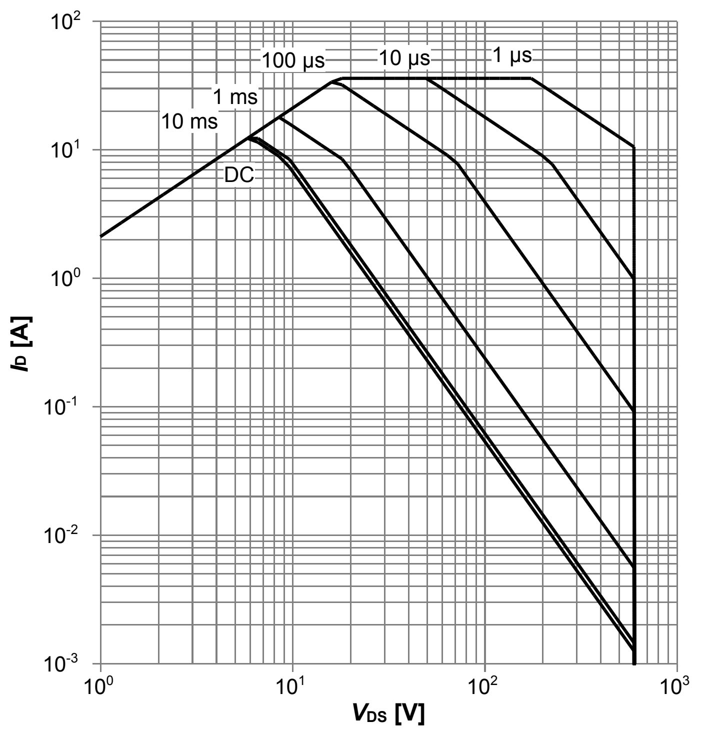
Diagram 1: Power dissipation	Diagram 2: Safe operating area
	
P_{tot}=f(T_C)	I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

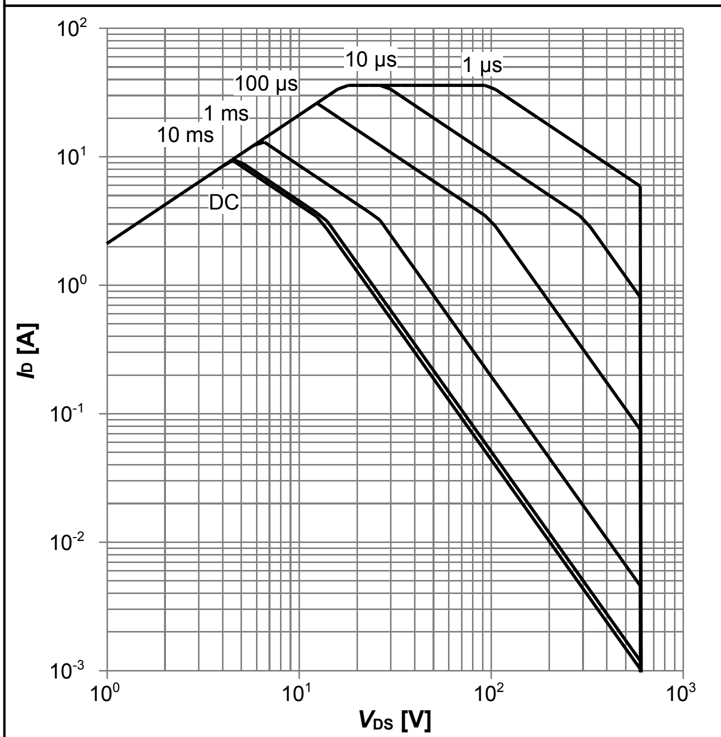
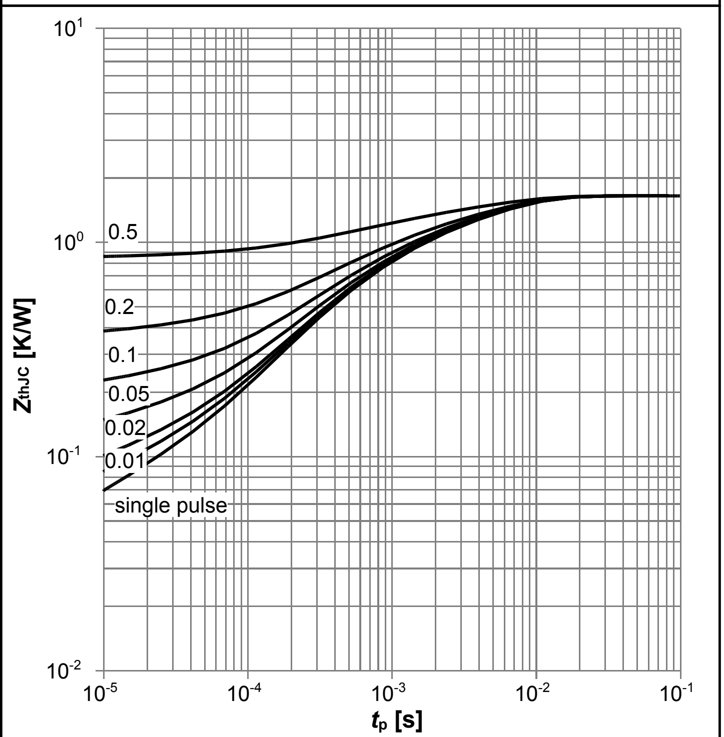
Diagram 3: Safe operating area	Diagram 4: Max. transient thermal impedance
	
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p	Z_{thJC} =f(t_P); parameter: D=t_p/T

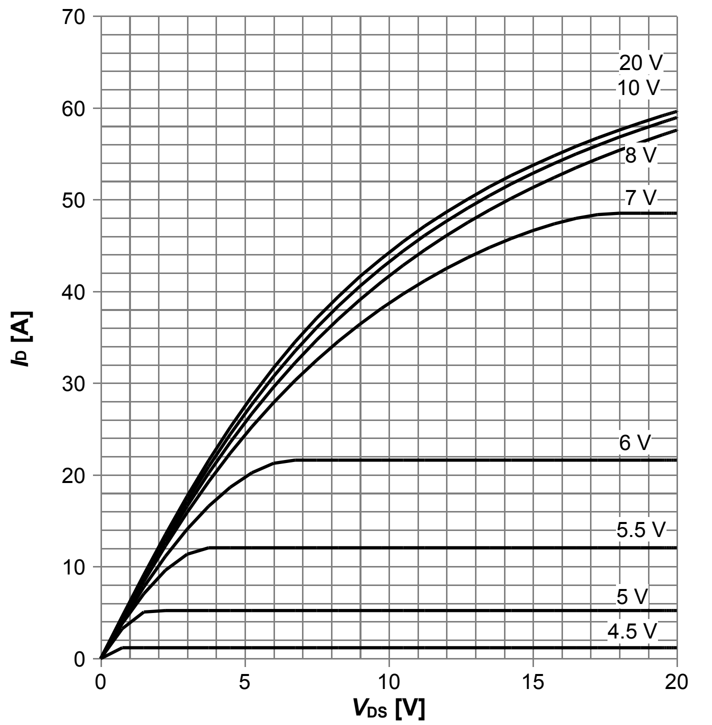
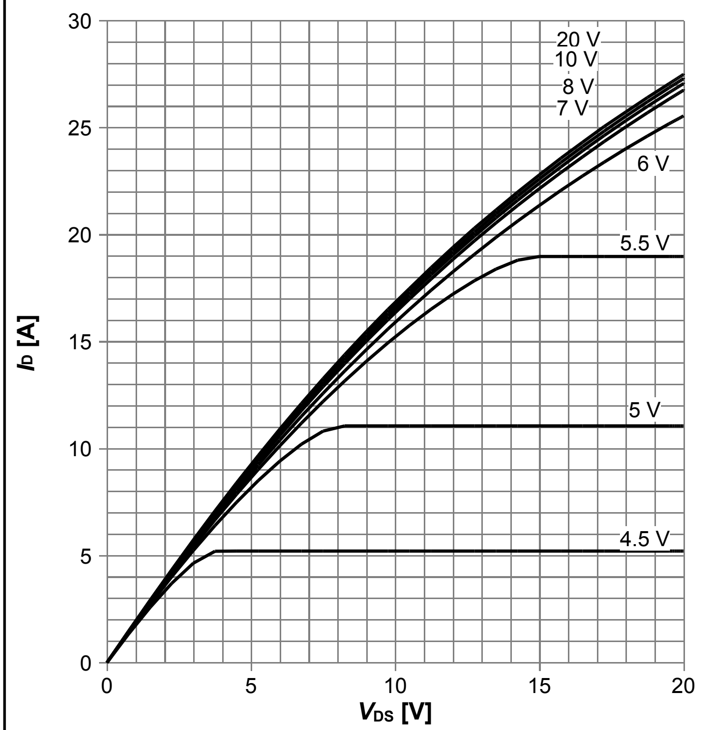
Diagram 5: Typ. output characteristics	Diagram 6: Typ. output characteristics
	
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}	I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

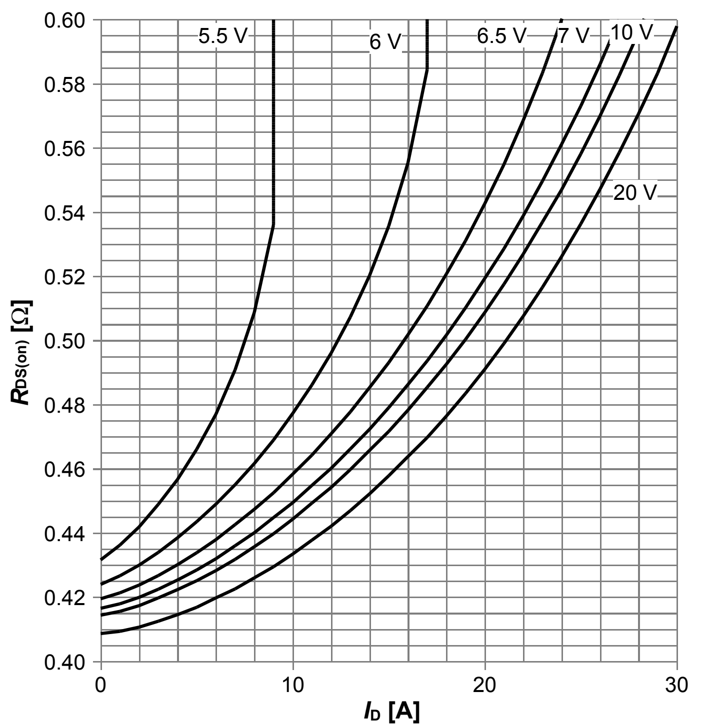
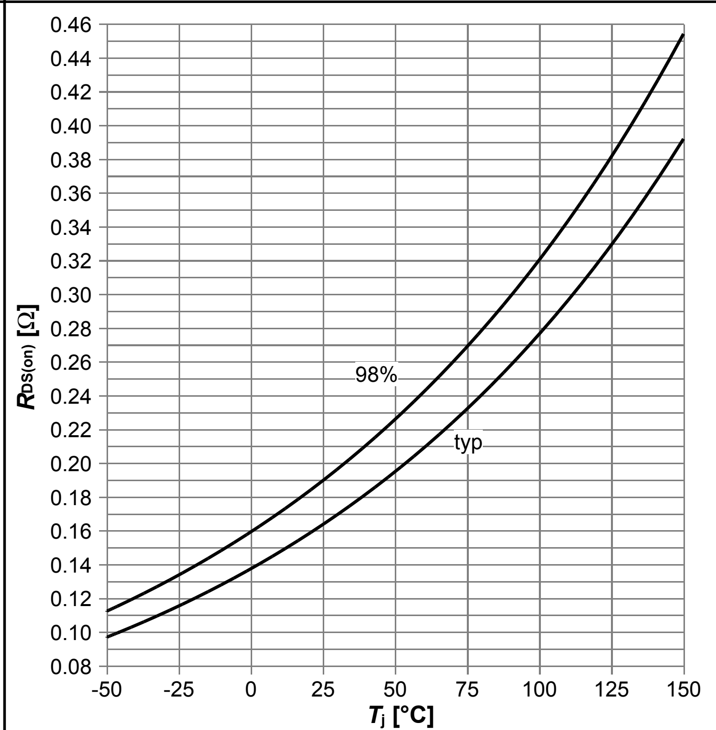
Diagram 7: Typ. drain-source on-state resistance	Diagram 8: Drain-source on-state resistance
	
$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}	$R_{DS(on)}$=f(T_j); I_D=4.2 A; V_{GS}=10 V

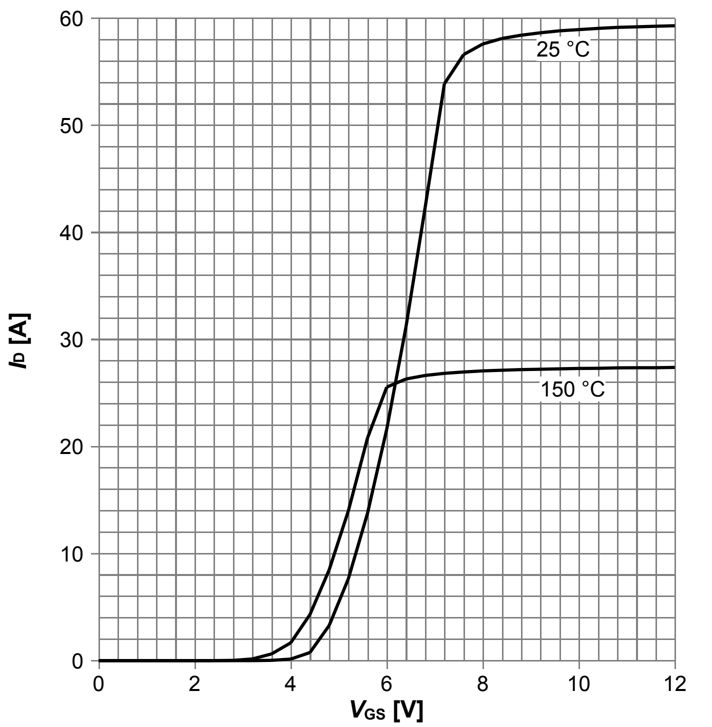
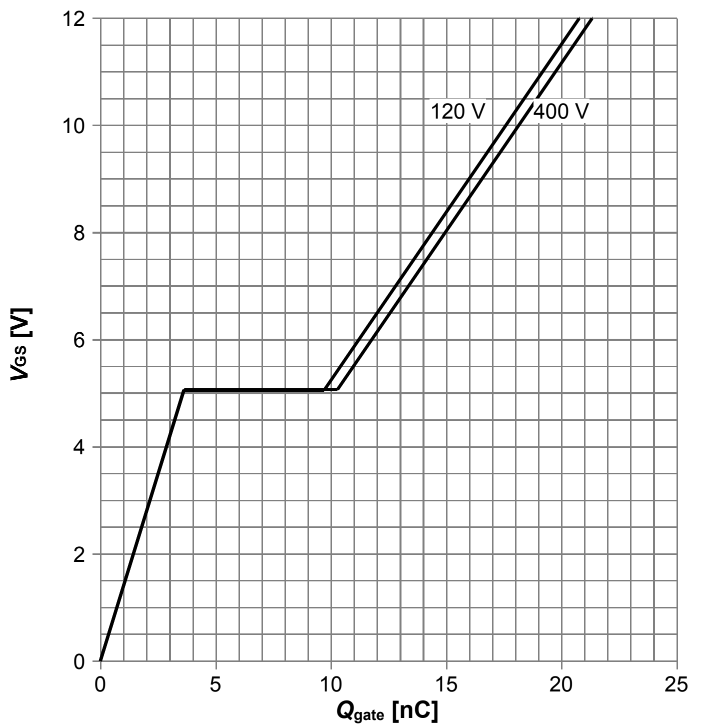
Diagram 9: Typ. transfer characteristics	Diagram 10: Typ. gate charge
	
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j	V_{GS}=f(Q_{gate}); I_D=4.2 A pulsed; parameter: V_{DD}

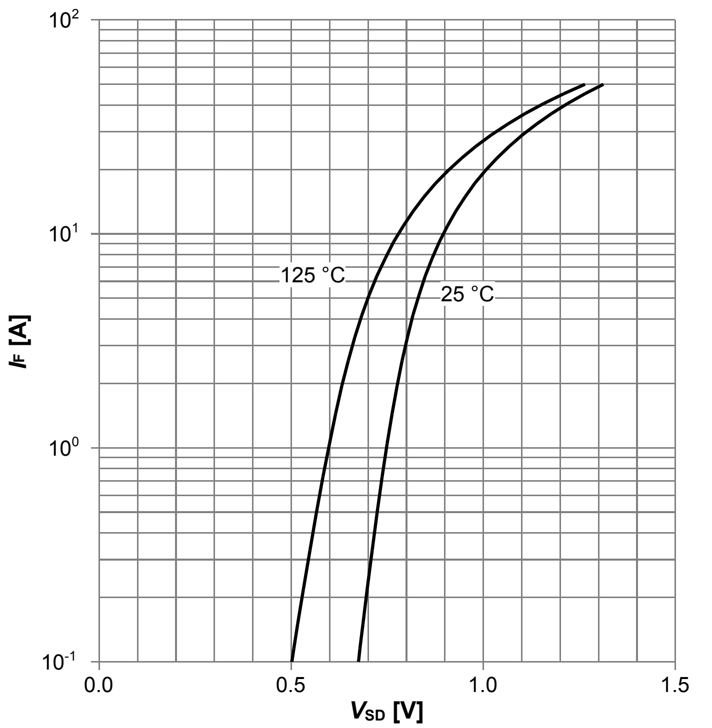
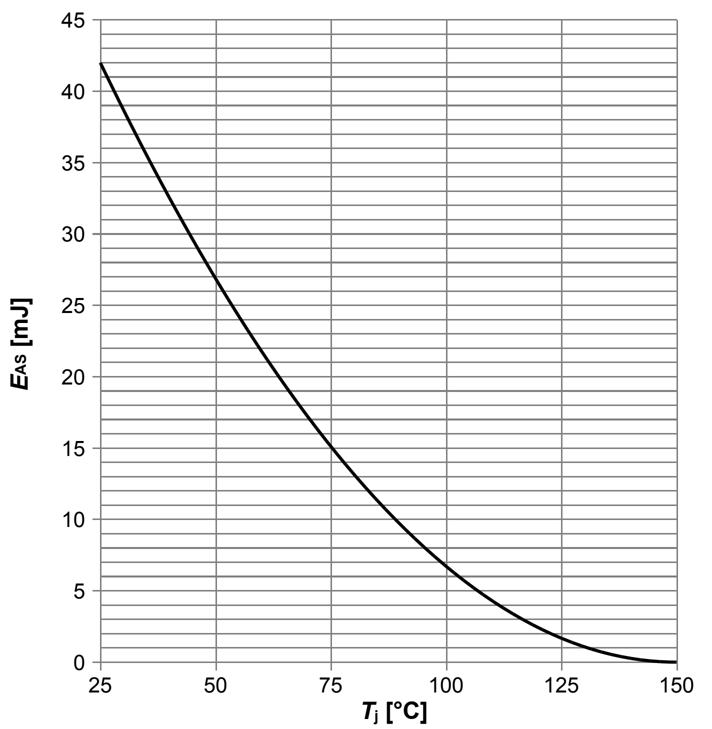
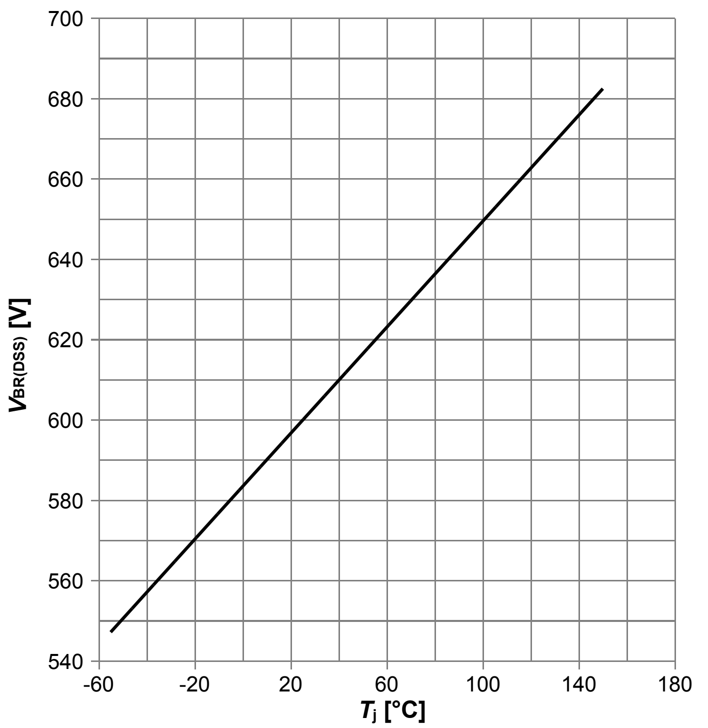
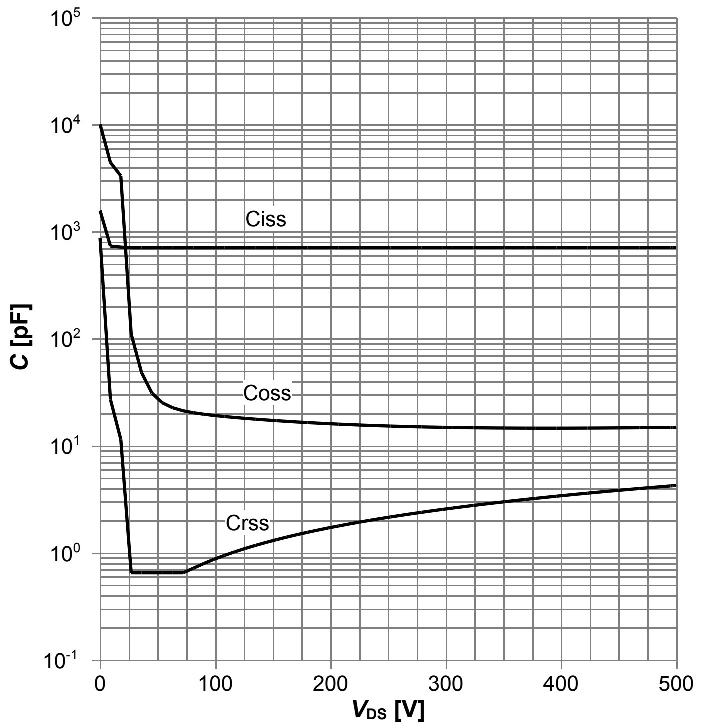
Diagram 11: Forward characteristics of reverse diode	Diagram 12: Avalanche energy
	
I_F=f(V_{SD}); parameter: T_j	E_{AS}=f(T_j); I_D=2.8 A; V_{DD}=50 V

Diagram 13: Drain-source breakdown voltage



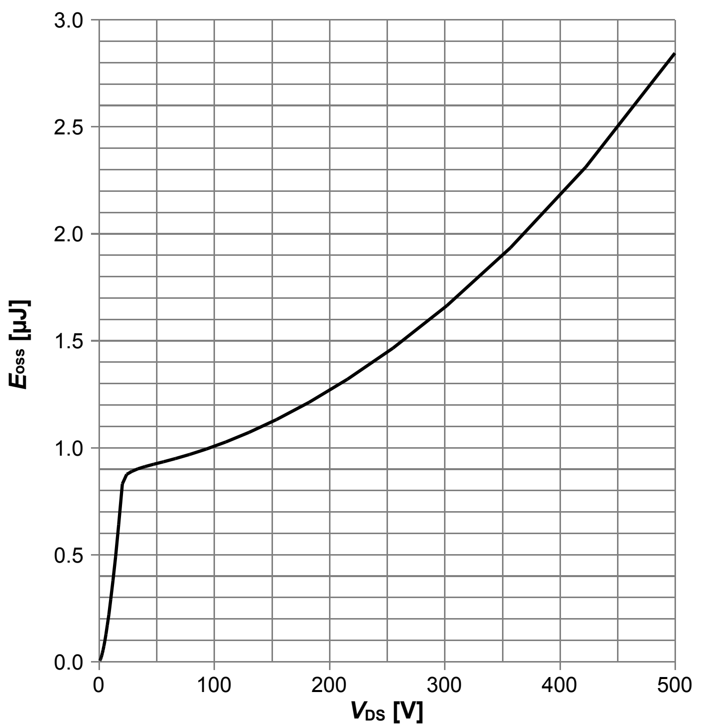
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy

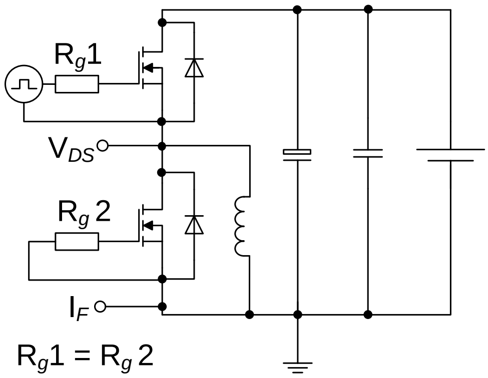


E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

Test circuit for diode characteristics	Diode recovery waveform



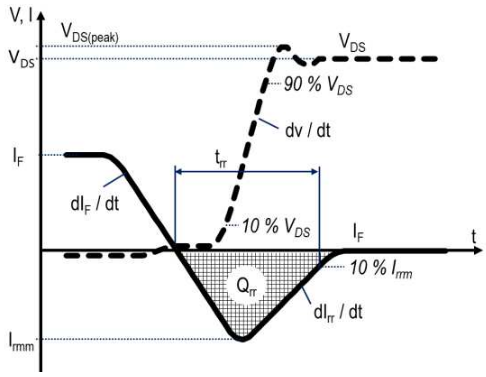
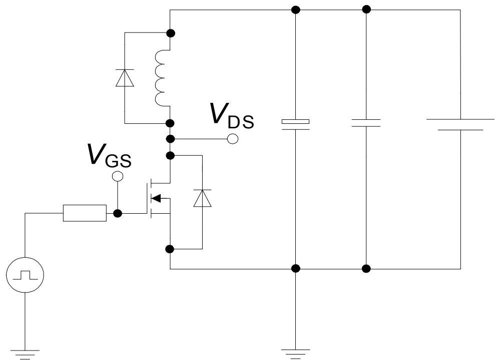


Table 9 Switching times

Switching times test circuit for inductive load	Switching times waveform



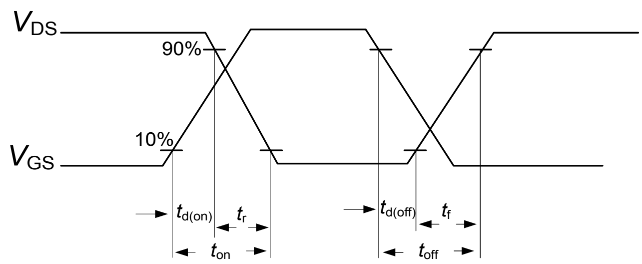
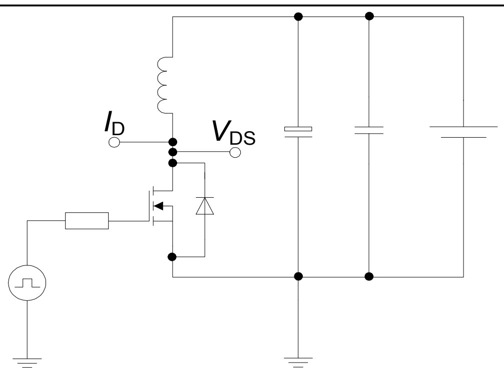
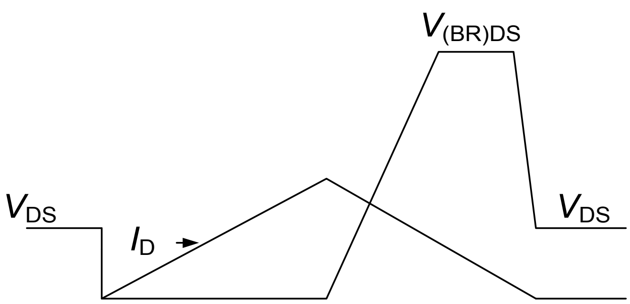


Table 10 Unclamped inductive load

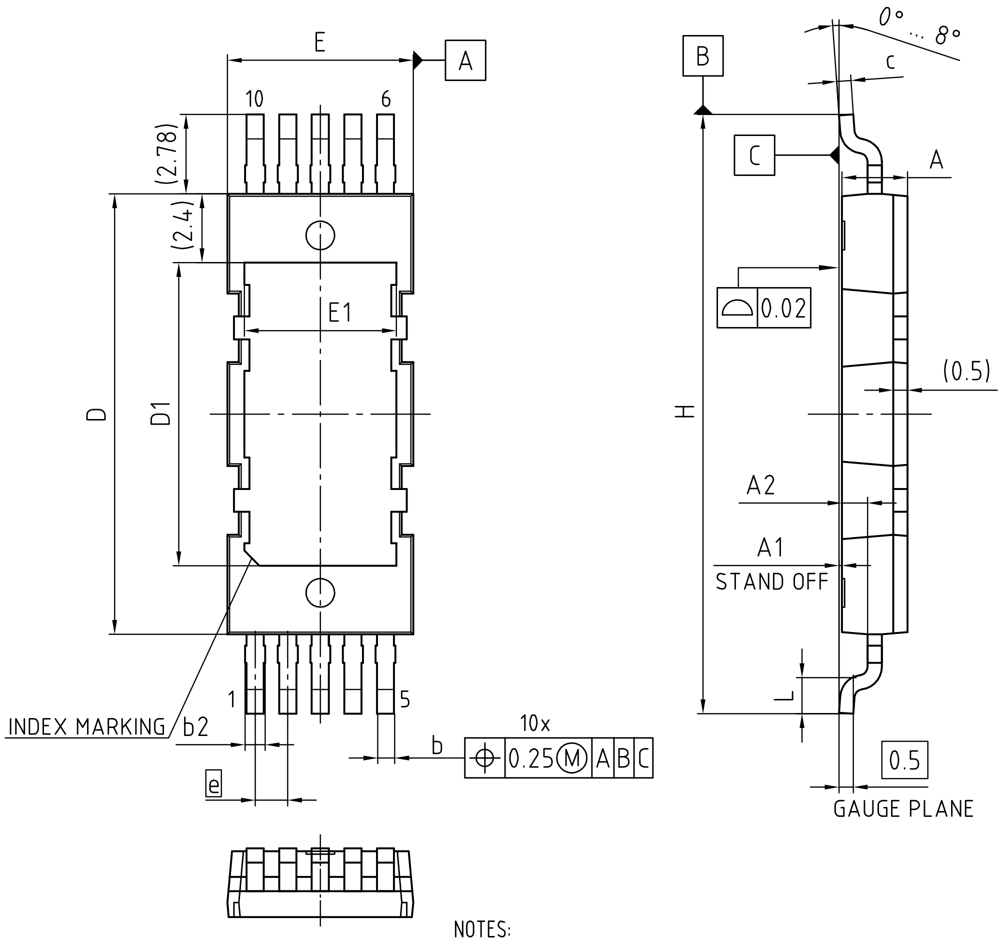
Unclamped inductive load test circuit	Unclamped inductive waveform





6 Package Outlines

PG-HDSOP-10-1



NOTES:
1. INDUSTRIAL QUALITY GRADE
2. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252
AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
3. ALL METAL SUFACES ARE TIN PLATED, EXCEPT AREA OF CUT.

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.35
A1	0.00	0.15
A2	0.89	1.10
b	0.57	0.63
b2	0.57	0.93
c	0.46	0.58
D	15.20	15.60
D1	10.50	10.70
E	6.40	6.60
E1	5.20	5.50
e	1.14	
N	10	
H	20.81	21.11
L	1.20	1.40

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Figure 1 Outline PG-HDSOP-10, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- IFX CoolMOS™ G7 Webpage: www.infineon.com
- IFX CoolMOS™ G7 application note: www.infineon.com
- IFX CoolMOS™ G7 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPDD60R190G7

Revision: 2018-01-05, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2018-01-05	Release of final version

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