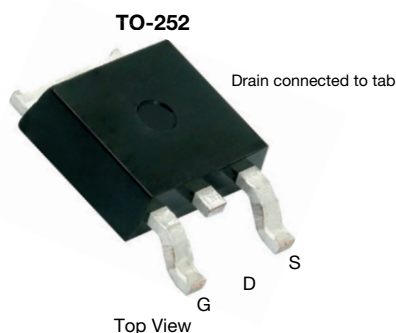


P-Channel 40 V (D-S) 175 °C MOSFET



FEATURES

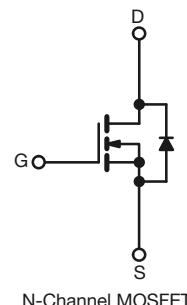
- TrenchFET® Gen IV p-channel power MOSFET
- Maximum 175 °C junction temperature
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Motor drive control
- LED backlighting
- Load switch
- Industrial



PRODUCT SUMMARY

V _{DS} (V)	-40
R _{DS(on)} max. (Ω) at V _{GS} = 10 V	0.0120
R _{DS(on)} max. (Ω) at V _{GS} = 4.5 V	0.0175
Q _g typ. (nC)	74.3
I _D (A)	42 ^d
Configuration	Single

ORDERING INFORMATION

Package	TO-252
Lead (Pb)-free and halogen-free	SUD40151EL-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	40	V
Gate-source voltage	V _{GS}	± 20	
Continuous drain current	I _D	42 ^d	A
		28.6	
Pulsed drain current (t = 100 μs)	I _{DM}	100	
Continuous source-drain diode current	I _S	41.7	
Single pulse avalanche current ^a	I _{AS}	25	mJ
Single pulse avalanche energy ^a	E _{AS}	31.25	
Maximum power dissipation	P _D	50 ^b	W
		16.7 ^b	
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	MAXIMUM	UNIT
Maximum junction-to-ambient (PCB mount) ^c	R _{thJA}	60	°C/W
Maximum junction-to-case (drain)	R _{thJC}	3	

Notes

- Duty cycle ≤ 1 %
- See SOA curve for voltage derating
- When mounted on 1" square PCB (FR4 material)
- Package limited



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	40	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.5	-	2.5	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	250	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 125 °C	-	-	150	
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 175 °C	-	-	5	mA
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} = 10 V	30	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 17.5 A	-	0.0100	0.0120	Ω
		V _{GS} = 4.5 V, I _D = 14.5 A	-	0.0135	0.0175	
Forward transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 17.5 A	-	70	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	-	5340	-	pF
Output capacitance	C _{oss}		-	335	-	
Reverse transfer capacitance	C _{rss}		-	303	-	
Total gate charge	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 17.5 A	-	74.3	112	nC
Gate-source charge	Q _{gs}		-	12.7	-	
Gate-drain charge	Q _{gd}		-	11.1	-	
Gate resistance	R _g	f = 1 MHz	0.86	4.3	8.6	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 20 V, R _L = 1.4 Ω, I _D ≅ 14 A, V _{GEN} = 10 V, R _g = 1 Ω	-	15	30	ns
Rise time	t _r		-	10	20	
Turn-off delay time	t _{d(off)}		-	75	113	
Fall time	t _f		-	75	113	
Drain-Source Body Diode Characteristics						
Pulse diode forward current (t = 100 μs)	I _{SM}		-	-	42	A
Body diode voltage	V _{SD}	I _F = 14 A, V _{GS} = 0 V	-	0.85	1.5	V
Body diode reverse recovery time	t _{rr}	I _F = 14 A, di/dt = 100 A/μs	-	30	45	ns
Body diode reverse recovery charge	Q _{rr}		-	0.02	0.04	μC
Reverse recovery fall time	t _a		-	15.3	-	ns
Reverse recovery rise time	t _b		-	14.7	-	
Body diode peak reverse recovery charge	I _{RM(REC)}		-	-	2.8	A

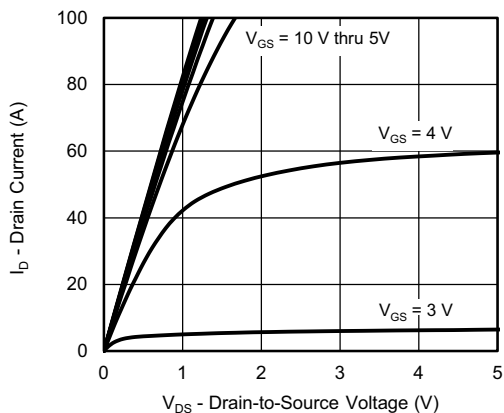
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

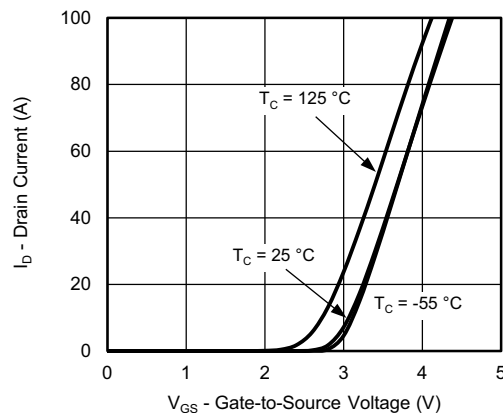
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



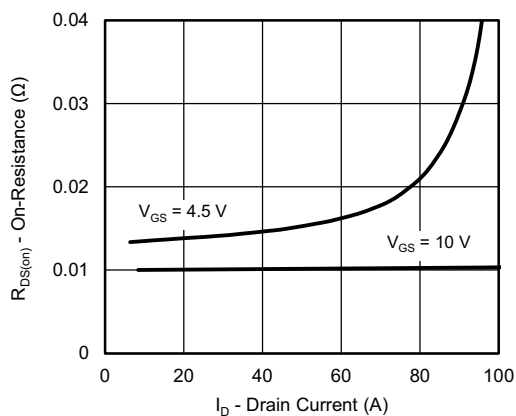
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



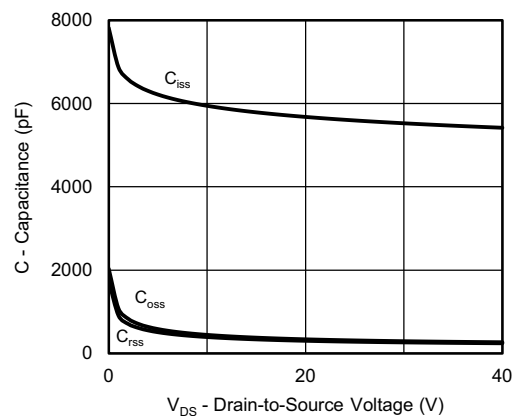
Output Characteristics



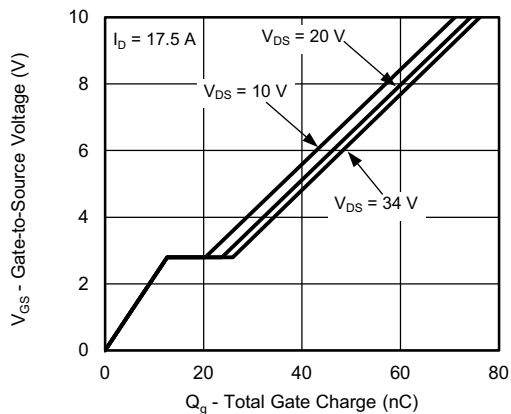
Transfer Characteristics



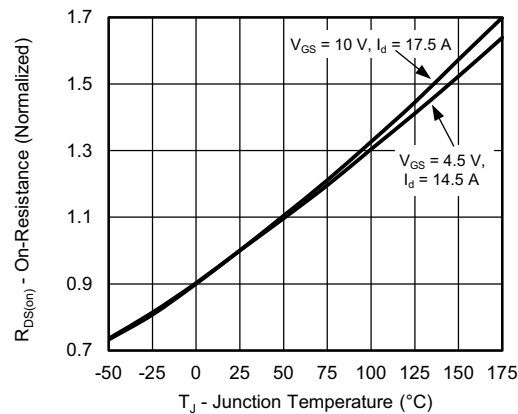
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



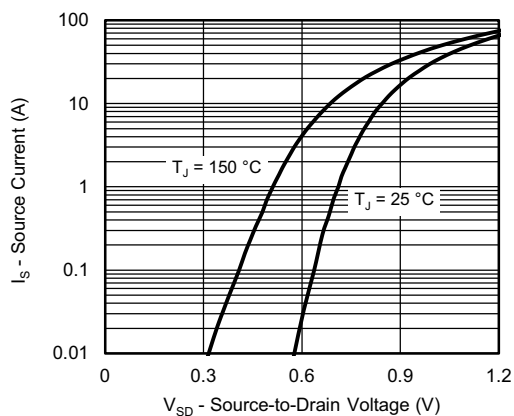
Gate Charge



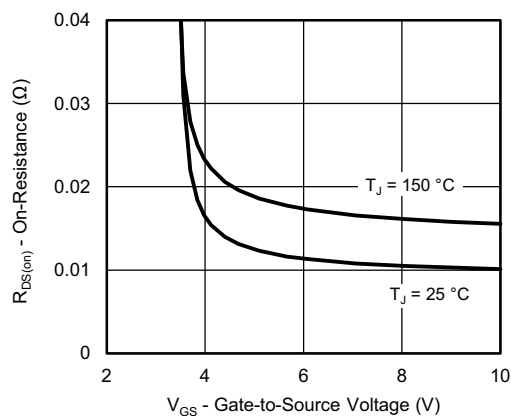
On-Resistance vs. Junction Temperature



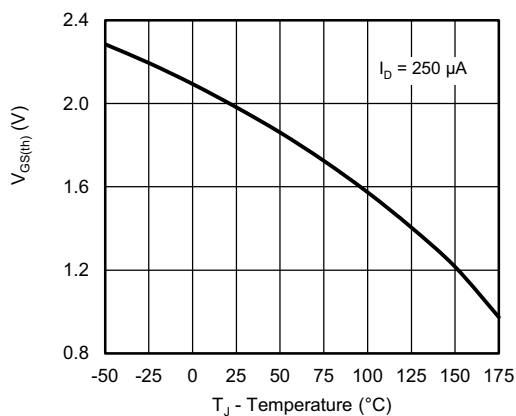
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



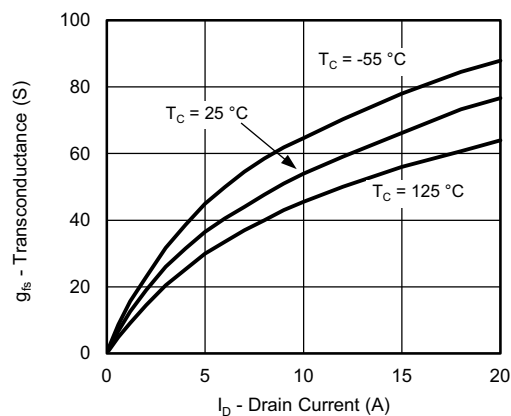
Source-Drain Diode Forward Voltage



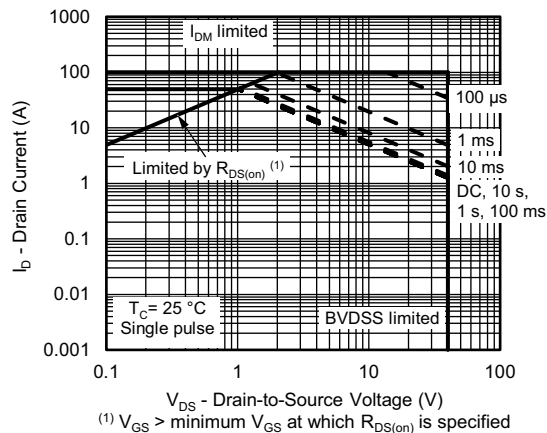
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



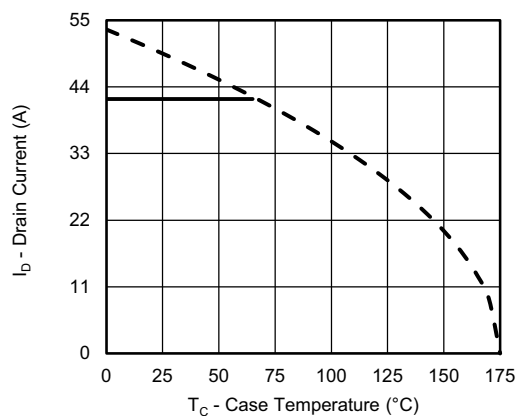
Transconductance



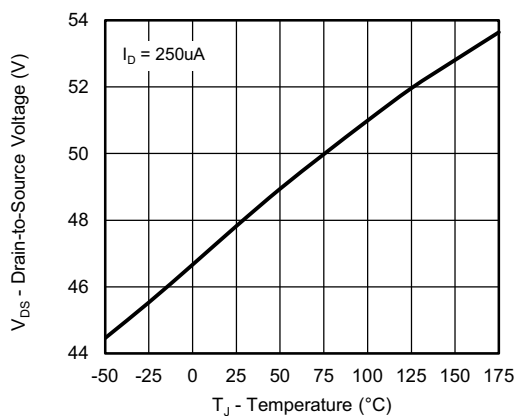
Safe Operating Area, Junction-to-Ambient



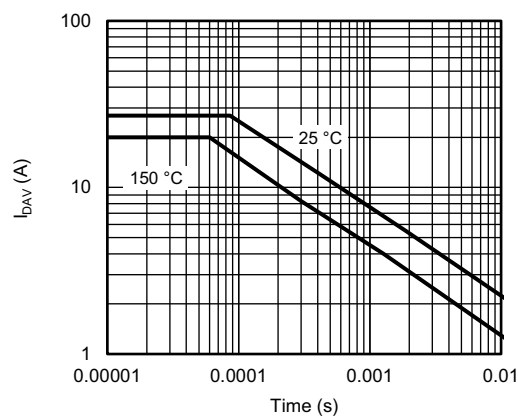
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Drain Source Breakdown vs. Junction Temperature



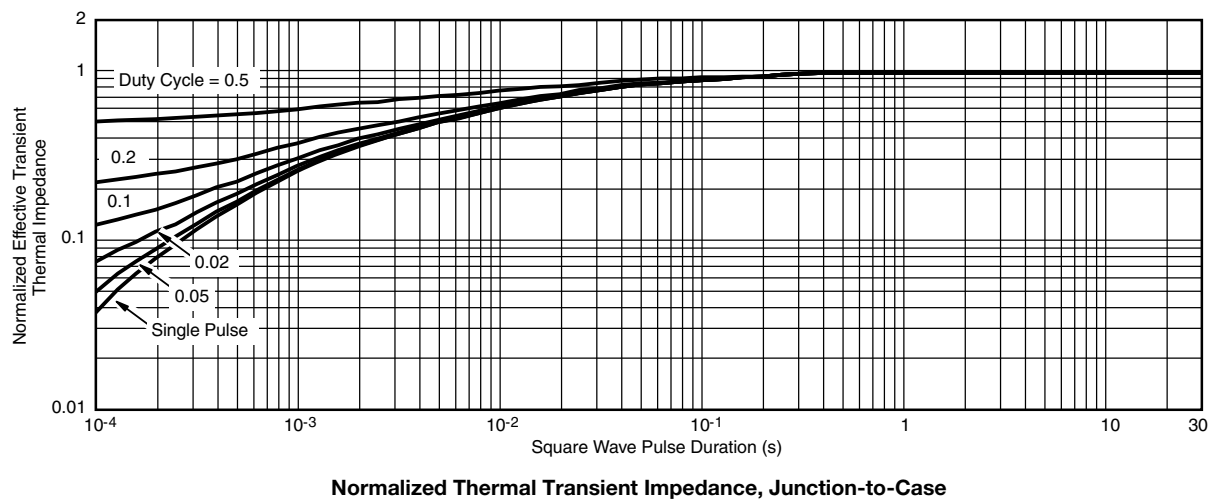
I_{DAV} vs. Time

Note

- a. The power dissipation P_D is based on T_J max. = 25 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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