

N-channel 950 V, 0.110 Ω typ., 38 A MDmesh™ K5 Power MOSFET in a TO-247 package

Datasheet - production data

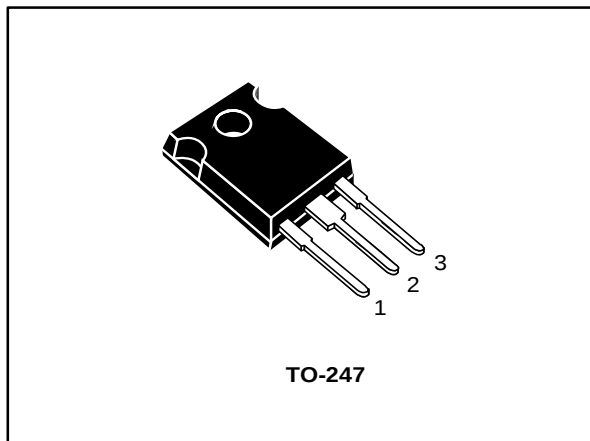
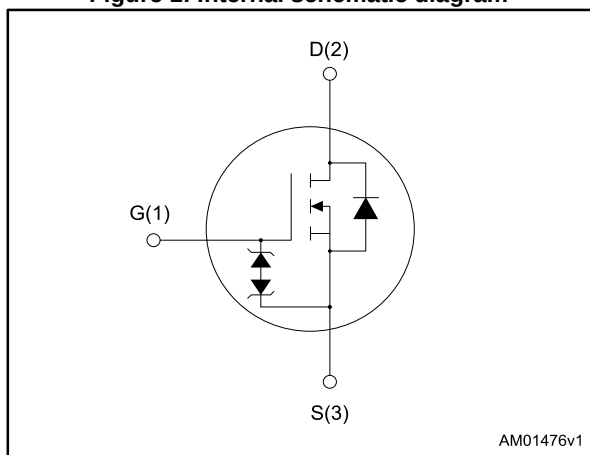


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D	P _{TOT}
STW40N95K5	950 V	0.130 Ω	38 A	450 W

- Industry's lowest R_{DS(on)} x area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STW40N95K5	40N95K5	TO-247	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	38	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	24	A
$I_{DM}^{(1)}$	Drain current (pulsed)	152	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	450	W
I_{AR}	Max current during repetitive or single pulse avalanche	13	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = 13\text{ A}$, $V_{DD} = 50\text{ V}$)	700	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^{\circ}\text{C}$

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾ $I_{SD} \leq 19\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DS(\text{peak})} \leq V_{(BR)DSS}$.

⁽³⁾ $V_{DS} \leq 760\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.28	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb max	50	$^{\circ}\text{C}/\text{W}$

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0, I _D = 1 mA	950			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0, V _{DS} = 950 V			1	μA
		V _{GS} = 0, V _{DS} = 950 V, T _C = 125 °C			50	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0, V _{GS} = ± 20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 19 A		0.110	0.130	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{GS} = 0, V _{DS} = 100 V, f = 1 MHz	-	3300	-	pF
C _{oss}	Output capacitance		-	250	-	pF
C _{rss}	Reverse transfer capacitance		-	2	-	pF
C _{o(tr)} ⁽¹⁾	Equivalent capacitance time related	V _{GS} = 0, V _{DS} = 0 to 760 V	-	398	-	pF
C _{o(er)} ⁽²⁾	Equivalent capacitance energy related		-	142	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz, I _D = 0	-	5	-	Ω
Q _g	Total gate charge	V _{DD} = 760 V, I _D = 38 A	-	93	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 10 V	-	18.7	-	nC
Q _{gd}	Gate-drain charge	(see Figure 16: "Gate charge test circuit")	-	63.4	-	nC

Notes:

⁽¹⁾Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

⁽²⁾energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 475 V, I _D = 19 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 15: "Switching times test circuit for resistive load")	-	33.5	-	ns
t _r	Rise time		-	51	-	ns
t _{d(off)}	Turn-off-delay time		-	91.5	-	ns
t _f	Fall time		-	10	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		38	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		152	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 38\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 38\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 18: "Unclamped inductive load test circuit")	-	706		ns
Q_{rr}	Reverse recovery charge		-	22		μC
I_{RRM}	Reverse recovery current		-	62		A
t_{rr}	Reverse recovery time	$I_{SD} = 38\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 18: "Unclamped inductive load test circuit")	-	886		ns
Q_{rr}	Reverse recovery charge		-	28.2		μC
I_{RRM}	Reverse recovery current		-	64		A

Notes:⁽¹⁾Pulse width limited by safe operating area.⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

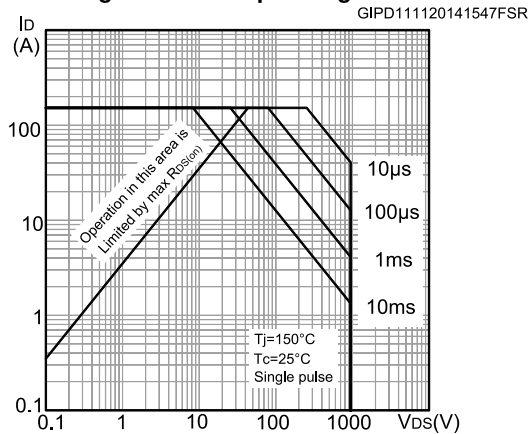


Figure 3: Thermal impedance

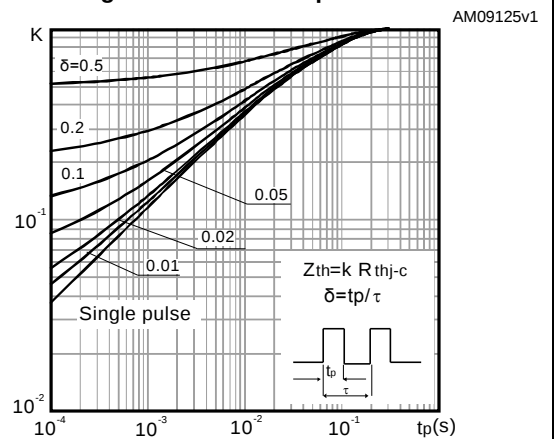


Figure 4: Output characteristics

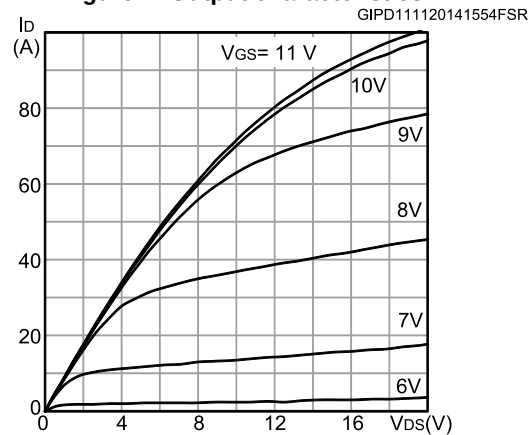


Figure 5: Transfer characteristics

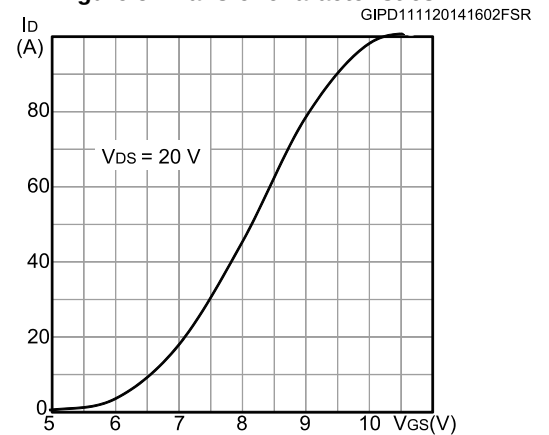


Figure 6: Gate charge vs gate-source voltage

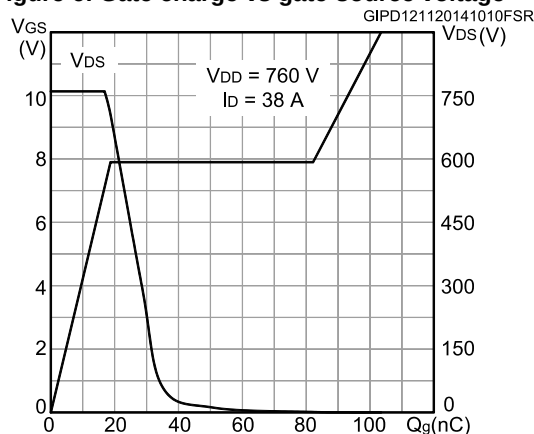


Figure 7: Static drain-source on-resistance

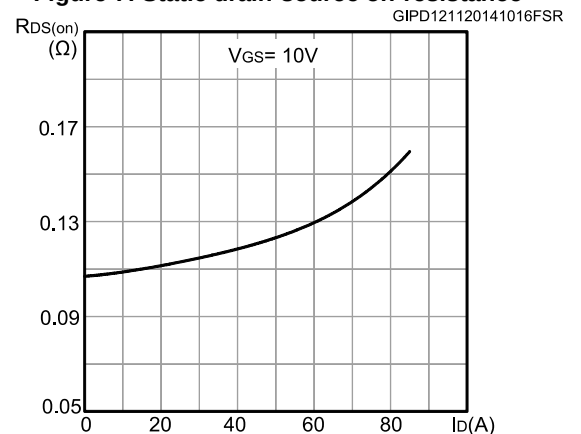


Figure 8: Capacitance variations

GIPD121120141027FSR

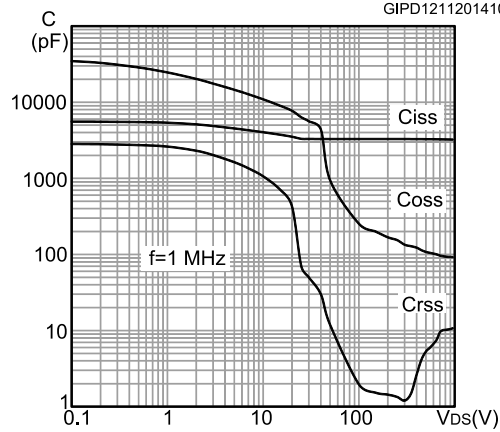


Figure 9: Normalized gate threshold voltage vs temperature

GIPD121120141035FSR

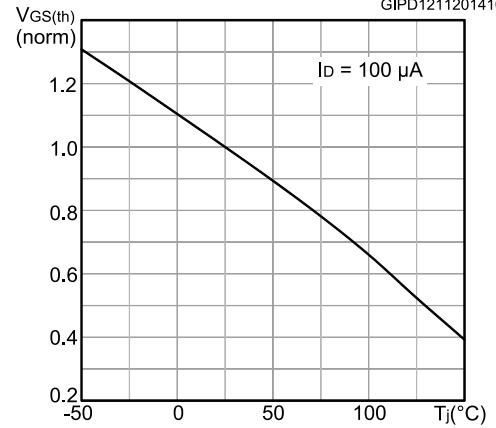


Figure 10: Normalized on-resistance

GIPD121120141039FSR

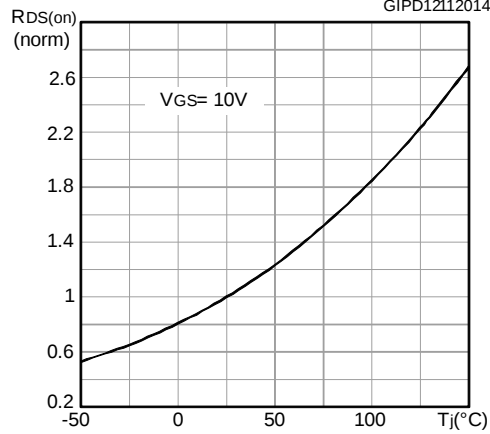


Figure 11: Normalized V(BR)DSS vs temperature

GIPD121120141041FSR

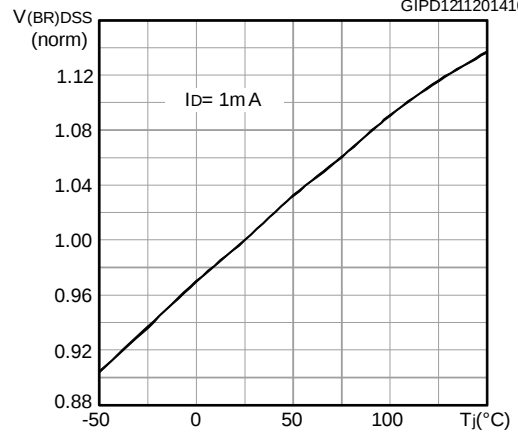


Figure 12: Output capacitance stored energy

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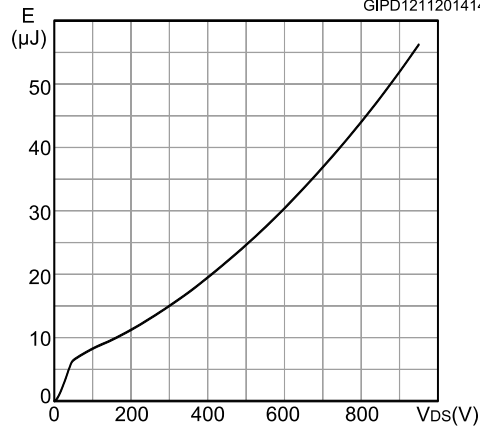


Figure 13: Source-drain diode forward characteristics

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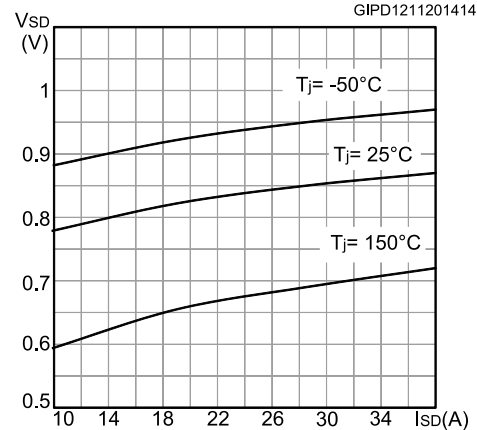
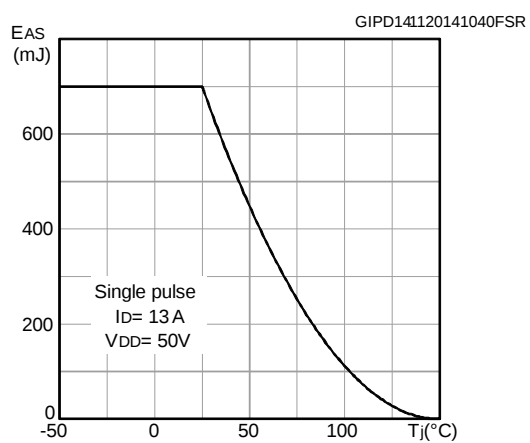


Figure 14: Maximum avalanche energy vs T J



3 Test circuits

Figure 15: Switching times test circuit for resistive load

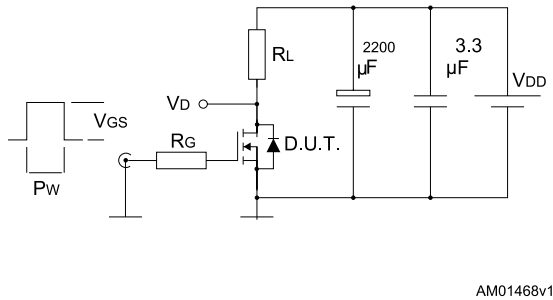


Figure 16: Gate charge test circuit

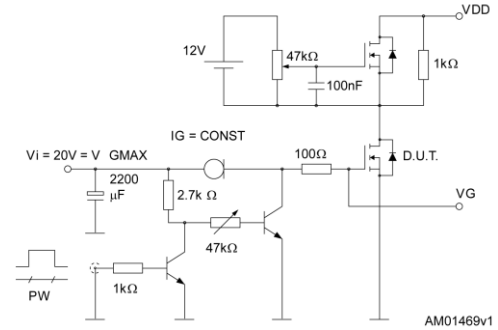


Figure 17: Test circuit for inductive load switching and diode recovery times

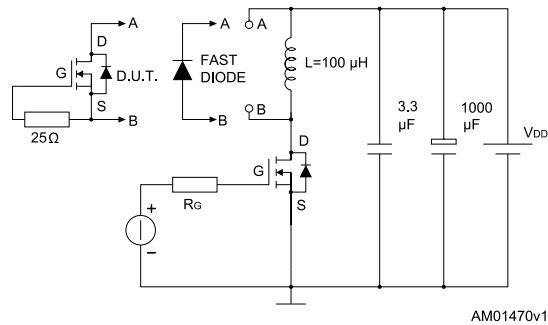


Figure 18: Unclamped inductive load test circuit

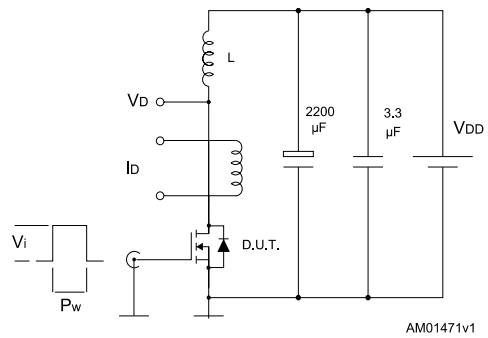


Figure 19: Unclamped inductive waveform

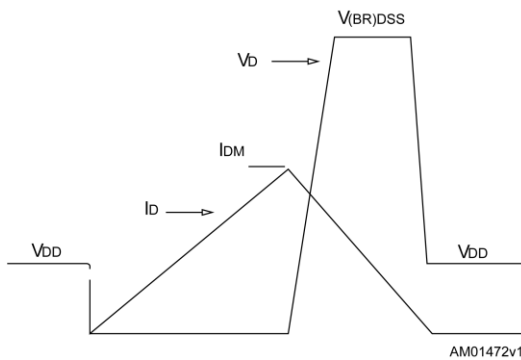
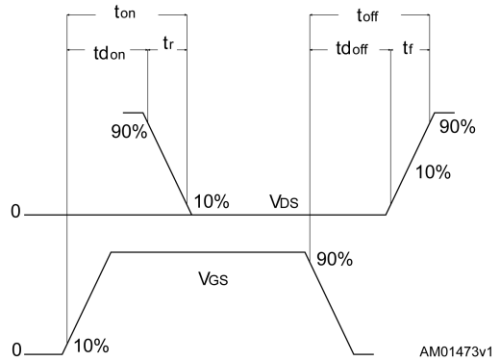


Figure 20: Switching time waveform

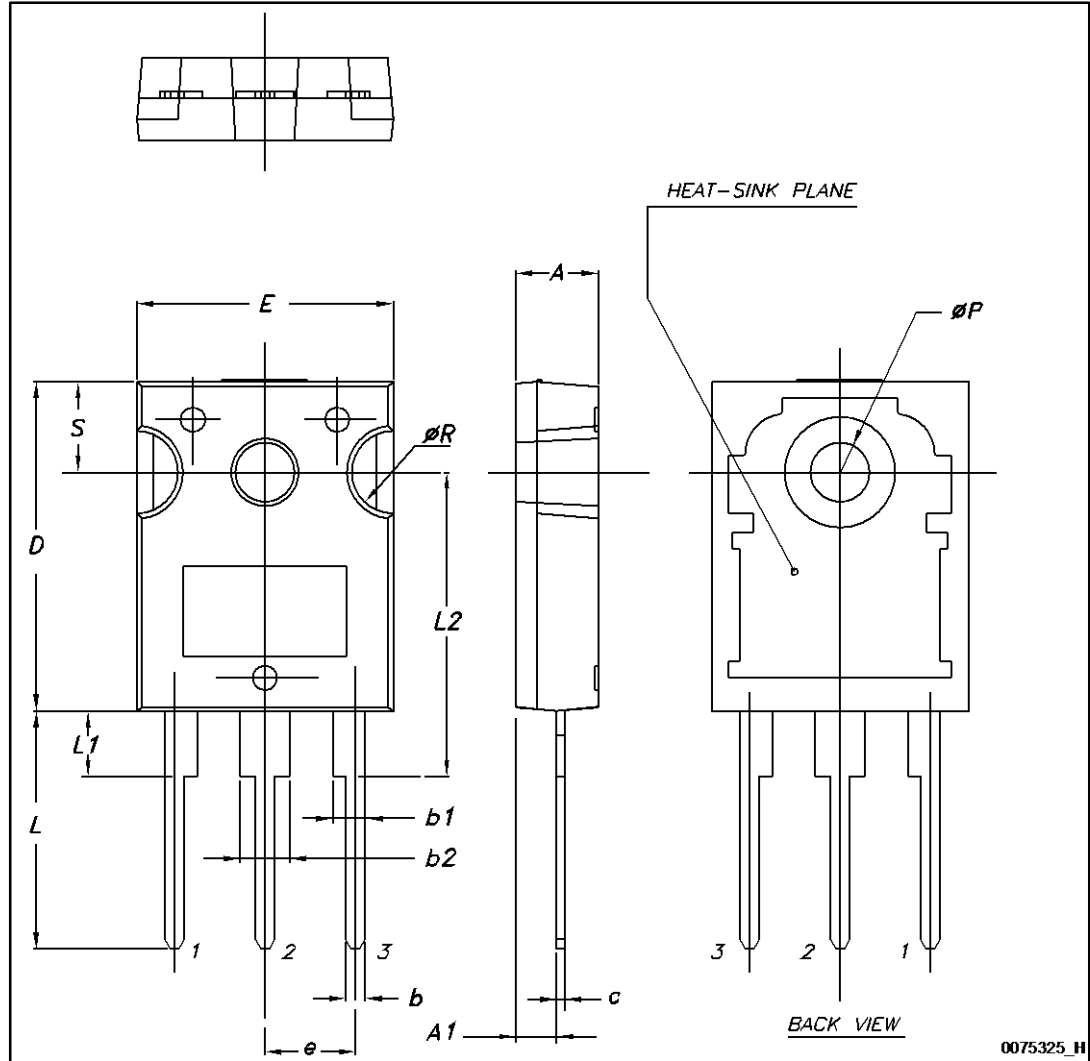


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-247 package information

Figure 21: TO-247 drawing



0075325_H

Table 9: TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
03-Jun-2014	1	First release.
14-Nov-2014	2	Document status promoted from preliminary to production data. Added Section 2.1: "Electrical characteristics (curves)" .

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