



ATP114

P-Channel Power MOSFET -60V, -55A, 16mΩ, Single ATPAK

ON Semiconductor®

<http://onsemi.com>

Features

- ON-resistance $R_{DS(on)1}=12m\Omega$ (typ.)
- 4V drive
- Protection diode in
- Input Capacitance $C_{iss}=4000pF$ (typ.)
- Halogen free compliance

Specifications

Absolute Maximum Ratings at $T_a=25^\circ C$

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		-60	V
Gate-to-Source Voltage	V_{GSS}		± 20	V
Drain Current (DC)	I_D		-55	A
Drain Current ($PW \leq 10\mu s$)	I_{DP}	$PW \leq 10\mu s$, duty cycle $\leq 1\%$	-165	A
Allowable Power Dissipation	P_D	$T_c=25^\circ C$	60	W
Channel Temperature	T_{ch}		150	$^\circ C$
Storage Temperature	T_{stg}		-55 to +150	$^\circ C$
Avalanche Energy (Single Pulse) *1	E_{AS}		100	mJ
Avalanche Current *2	I_{AV}		-28	A

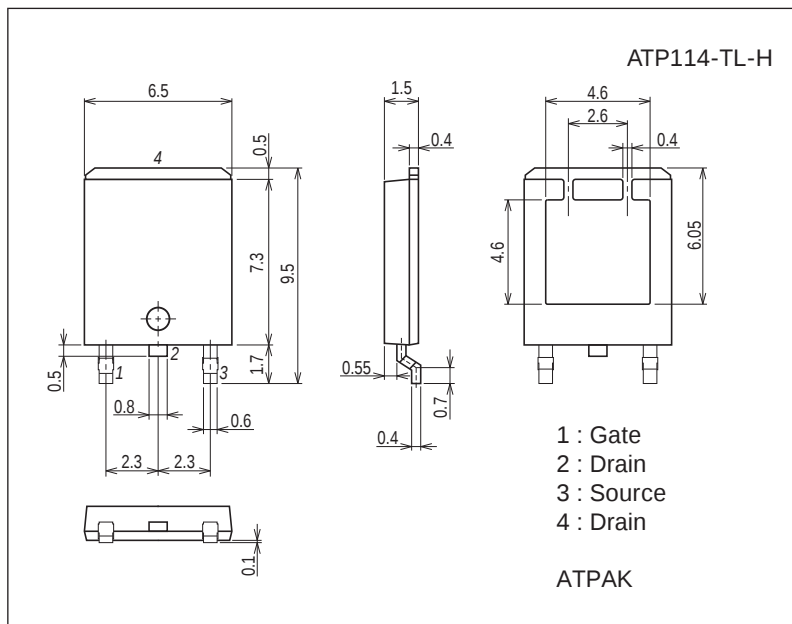
Note : *1 $V_{DD}=-15V$, $L=200\mu H$, $I_{AV}=-28A$ *2 $L \leq 100\mu H$, Single pulse

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

unit : mm (typ)

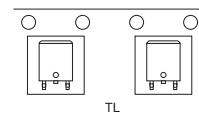
7057-001



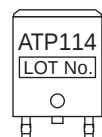
Product & Package Information

- Package : ATPAK
- JEITA, JEDEC : -
- Minimum Packing Quantity : 3,000 pcs./reel

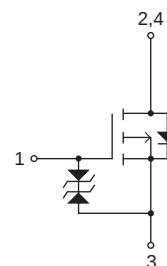
Packing Type: TL



Marking



Electrical Connection

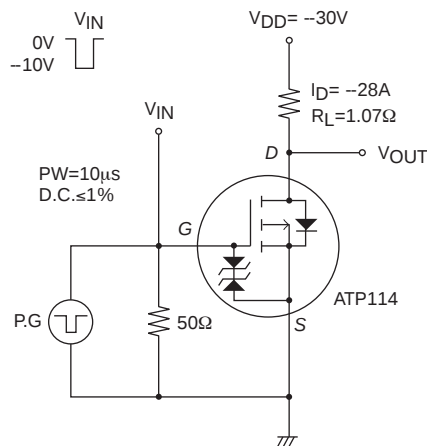


ATP114

Electrical Characteristics at Ta=25°C

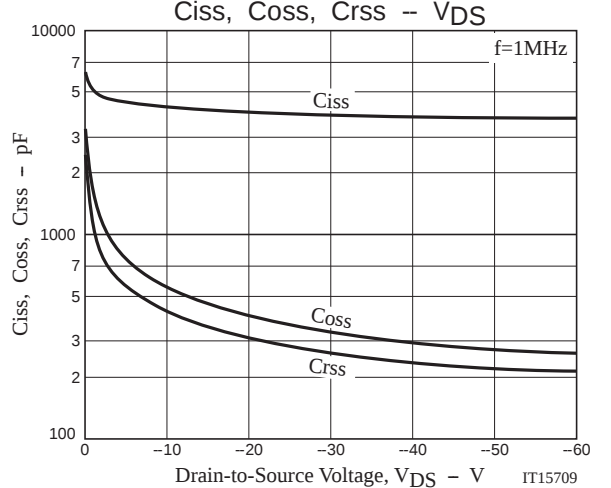
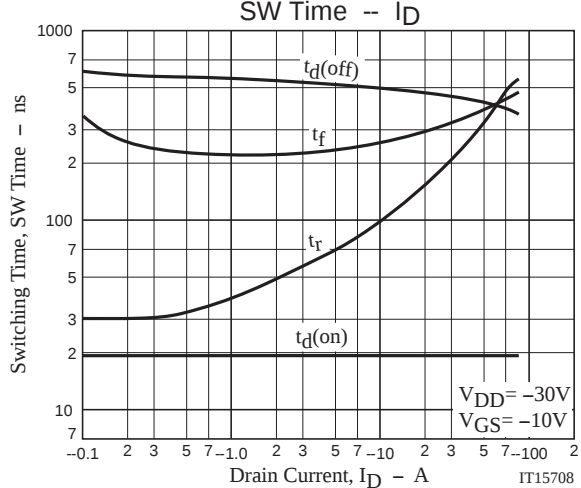
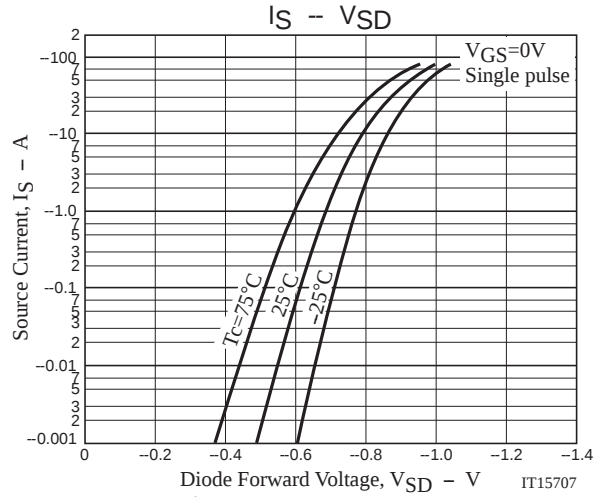
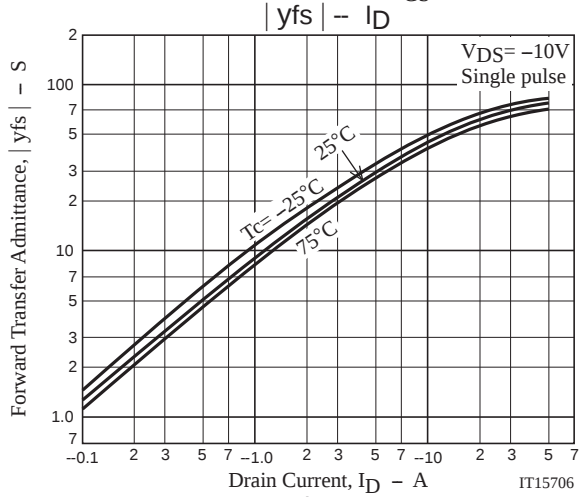
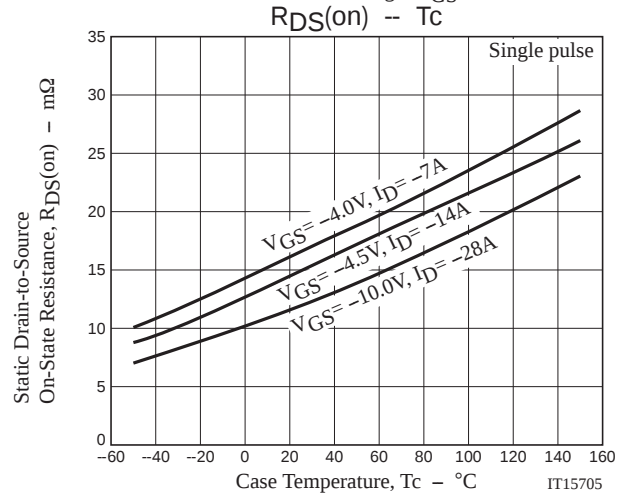
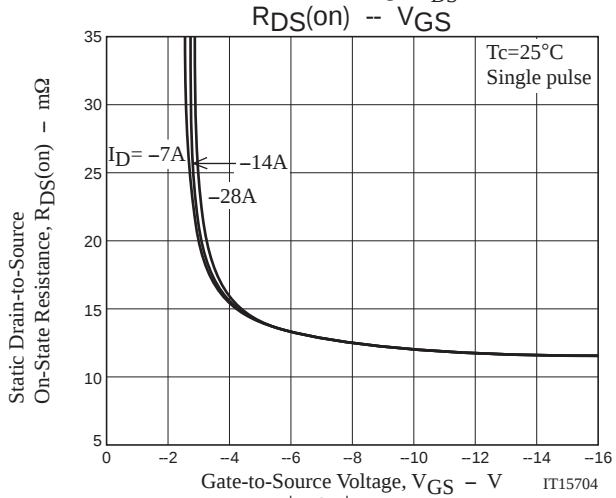
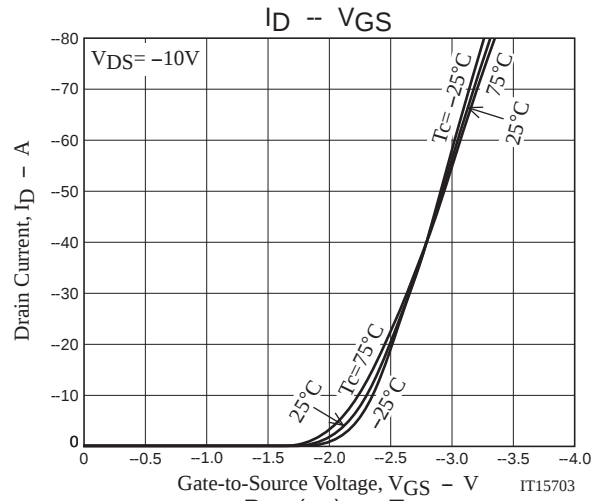
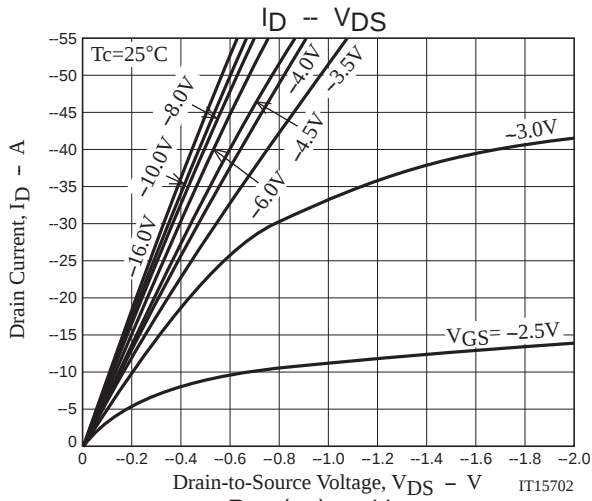
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = -1mA, V_{GS} = 0V$	-60			V
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60V, V_{GS} = 0V$			-1	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 16V, V_{DS} = 0V$			± 10	μA
Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = -10V, I_D = -1mA$	-1.2		-2.6	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS} = -10V, I_D = -28A$		65		S
Static Drain-to-Source On-State Resistance	$R_{DS(on)1}$	$I_D = -28A, V_{GS} = -10V$		12	16	m Ω
	$R_{DS(on)2}$	$I_D = -14A, V_{GS} = -4.5V$		15	21	m Ω
	$R_{DS(on)3}$	$I_D = -7A, V_{GS} = -4V$		16.5	24	m Ω
Input Capacitance	C_{iss}	$V_{DS} = -20V, f = 1MHz$		4000		pF
Output Capacitance	C_{oss}			400		pF
Reverse Transfer Capacitance	C_{rss}			315		pF
Turn-ON Delay Time	$t_d(on)$	See specified Test Circuit.		19		ns
Rise Time	t_r			200		ns
Turn-OFF Delay Time	$t_d(off)$			450		ns
Fall Time	t_f			300		ns
Total Gate Charge	Q_g	$V_{DS} = -30V, V_{GS} = -10V, I_D = -55Ap$		92		nC
Gate-to-Source Charge	Q_{gs}			15		nC
Gate-to-Drain "Miller" Charge	Q_{gd}			15.5		nC
Diode Forward Voltage	V_{SD}	$I_S = -55A, V_{GS} = 0V$		-0.95	-1.5	V

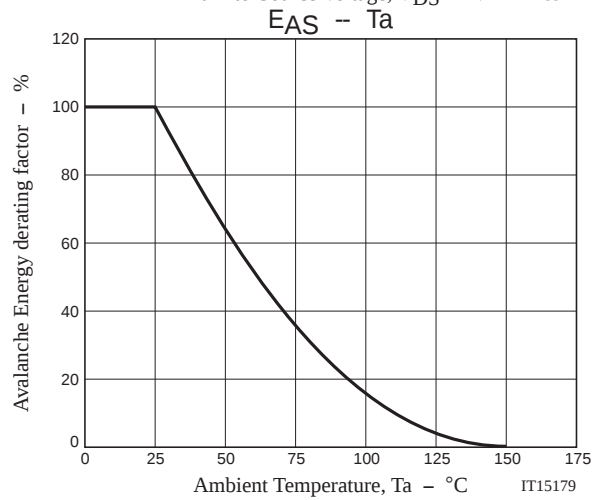
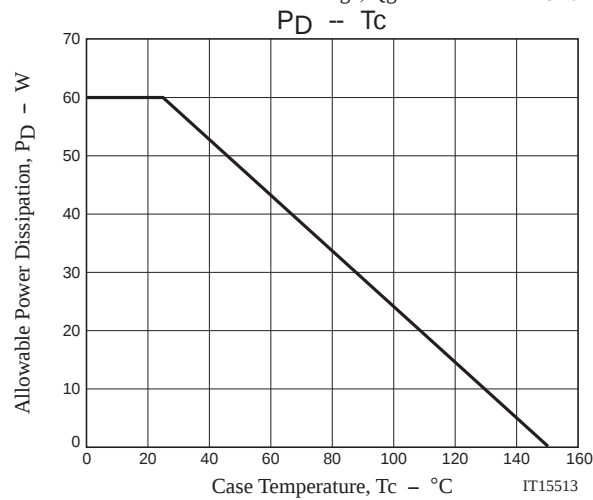
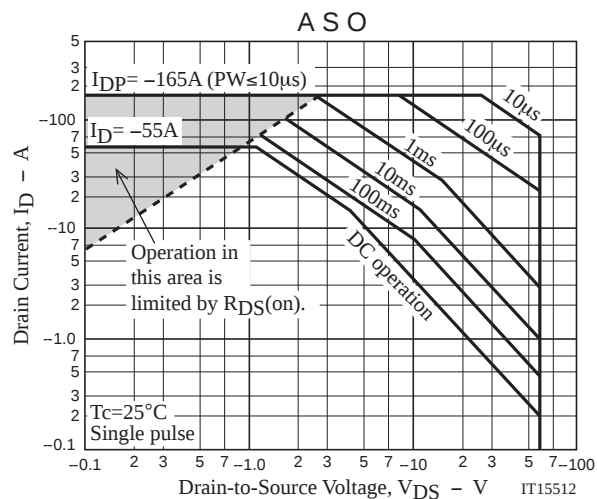
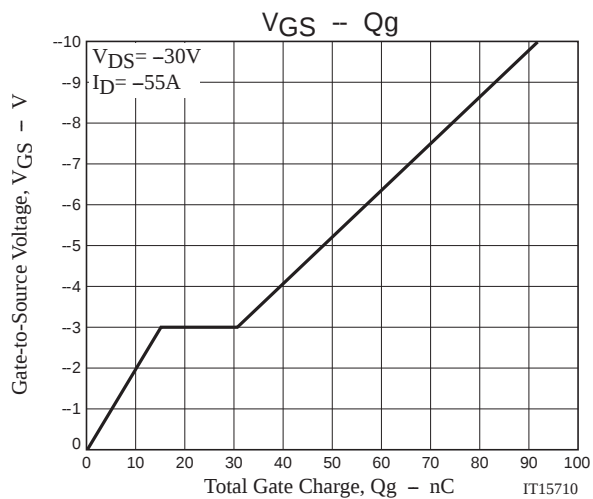
Switching Time Test Circuit



Ordering Information

Device	Package	Shipping	memo
ATP114-TL-H	ATPAK	3,000pcs./reel	Pb Free and Halogen Free



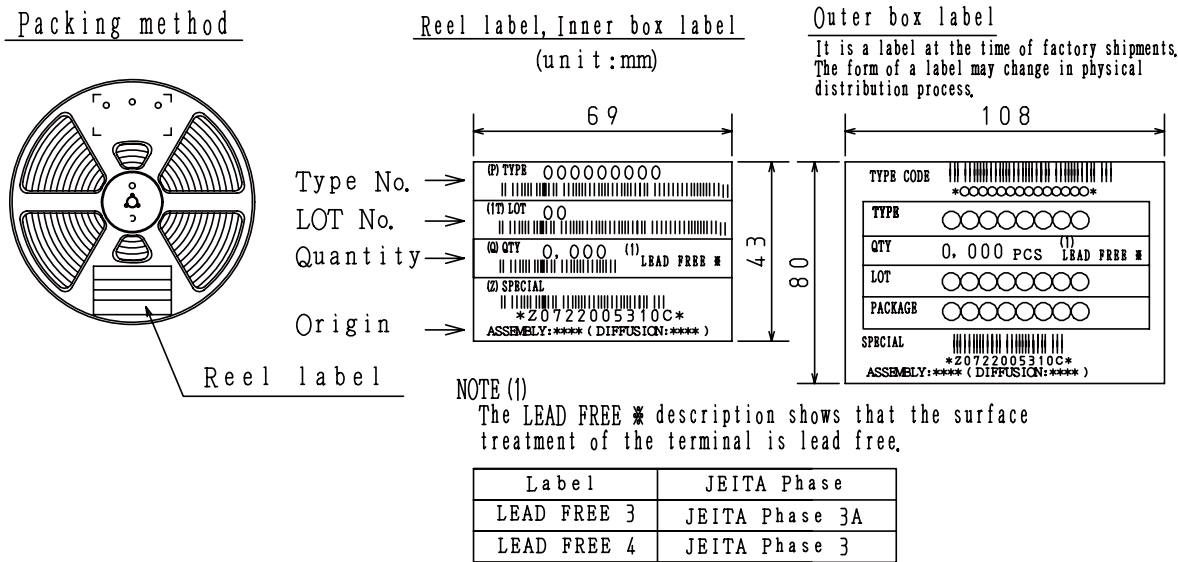


Taping Specification

ATP114-TL-H

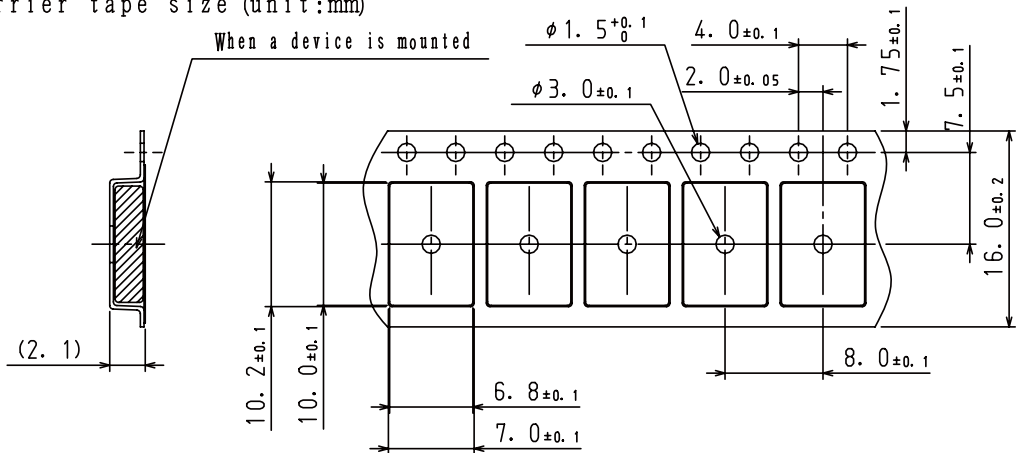
1. Packing Format (TL)

Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	INNER BOX SD-C-18	OUTER BOX SD-A-18
ATPAK	ATP	3, 000	3, 000	15, 000	1 reels contained Dimensions:mm (external) 3 4 0×3 4 0×2 8	5 inner boxes contained Dimensions:mm (external) 3 5 5×3 5 5×1 6 5

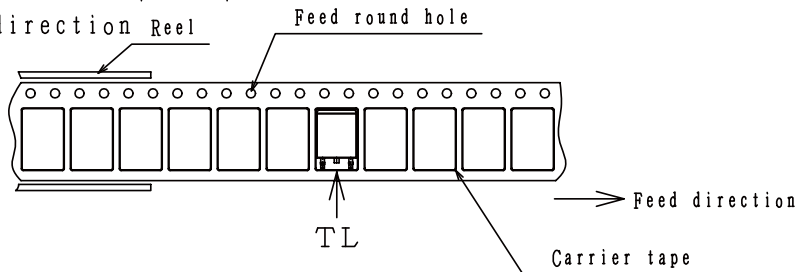


2. Taping configuration

2-1. Carrier tape size (unit:mm)



2-2. Device placement direction Reel



The one electode terminals on feed hole side...TL

Outline Drawing
ATP114-TL-H



Land Pattern Example



Note on usage : Since the ATP114 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.