

Dual N-Channel OptiMOS™ MOSFET

Features

- Dual N-channel OptiMOS™ MOSFET
- Optimized for high performance Buck converter
- Logic level (4.5V rated)
- 100% avalanche tested
- Qualified according to JEDEC¹⁾ for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Integrated monolithic Schottky-like diode



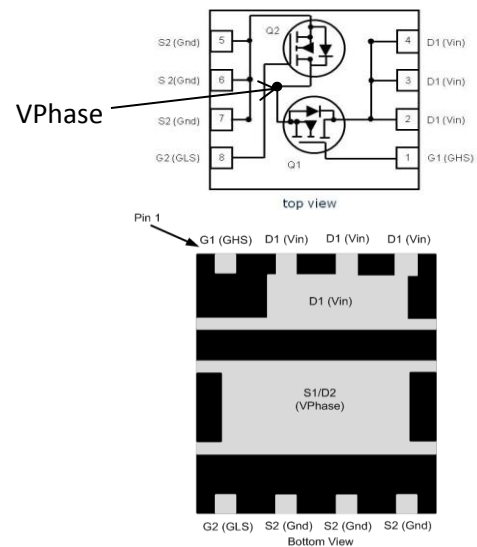
Type	Package	Marking
BSC0910NDI	PG-TISON-8	0910NDI

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified ²⁾

Parameter	Symbol	Conditions	Value		Unit
			Q1	Q2	
Continuous drain current	I_D	$T_C=70\text{ °C}$, $V_{GS}=10\text{ V}$	40	40	A
		$T_A=25\text{ °C}$, $V_{GS}=4.5\text{ V}^{3)}$	16	31	
		$T_A=70\text{ °C}$, $V_{GS}=4.5\text{ V}^{3)}$	13	25	
		$T_A=25\text{ °C}$, $V_{GS}=10\text{ V}^{4)}$	11	22	
Pulsed drain current ⁵⁾	$I_{D,pulse}$	$T_C=70\text{ °C}$	160	160	
Avalanche energy, single pulse	E_{AS}	Q1: $I_D=20\text{ A}$, Q2: $I_D=20\text{ A}$, $R_{GS}=25\text{ }\Omega$	12	80	mJ
Gate source voltage	V_{GS}		± 20		V
Power dissipation	P_{tot}	$T_A=25\text{ °C}^{2)}$	2.5	2.5	W
		$T_A=25\text{ °C}$, minimum footprint ⁴⁾	1.0	1.0	
Operating and storage temperature	T_j, T_{stg}		-55 ... 150		°C
IEC climatic category; DIN IEC 68-1			55/150/56		

Product Summary

		Q1	Q2	
V_{DS}		25	25	V
$R_{DS(on),max}$	$V_{GS}=10\text{ V}$	4.6	1.2	mΩ
	$V_{GS}=4.5\text{ V}$	5.9	1.6	
I_D		40	40	A



Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	Q1	R_{thJC}		-	-	4.5	K/W
	Q2			-	-	1.5	
Thermal resistance, junction - ambient ¹⁾	Q1	R_{thJA}	6 cm ² cooling area ³⁾	-	-	50	
	Q2			-	-		
	Q1		minimal footprint, steady state ⁴⁾	-	-	125	
	Q2			-	-		

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	Q1	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=10\text{ mA}$	25	-	-	V
	Q2						
Breakdown voltage temperature coefficient	Q1	$dV_{(BR)DSS}/dT_j$	$I_D=10\text{ mA}$, referenced to 25 °C	-	15	-	mV/K
	Q2						
Gate threshold voltage	Q1	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\text{ }\mu\text{A}$	1	-	2	V
	Q2						
Zero gate voltage drain current	Q1	I_{DSS}	$V_{DS}=20\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	-	1	μA
	Q2			-	-	500	
	Q1		$V_{DS}=20\text{ V}, V_{GS}=0\text{ V}, T_j=150\text{ °C}$	-	-	0.1	mA
	Q2			-	3	-	
Gate-source leakage current	Q1	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	-	100	nA
	Q2						
Drain-source on-state resistance	Q1	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=25\text{ A}$	-	4.7	5.9	m Ω
	Q2			-	1.25	1.6	
	Q1		$V_{GS}=10\text{ V}, I_D=25\text{ A}$	-	3.5	4.6	
	Q2			-	0.9	1.2	
Gate resistance	Q1	R_G		0.4	0.8	1.6	Ω
	Q2			0.4	0.7	1.4	
Transconductance	Q1	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=30\text{ A}$	42	84	-	S
	Q2			85	170	-	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	Q1	C_{iss}	$V_{GS}=0\text{ V},$ $V_{DS}=12\text{ V}, f=1\text{ MHz}$	-	760	1000	pF
	Q2			-	3400	4500	
Output capacitance	Q1	C_{oss}		-	370	500	
	Q2			-	1700	2300	
Reverse transfer capacitance	Q1	C_{rss}		-	35	-	
	Q2			-	150	-	
Turn-on delay time	Q1	$t_{d(on)}$	$V_{DD}=12\text{ V},$ $V_{GS}=10\text{ V}, R_G=1.6\text{ }\Omega,$ $I_D=30\text{ A}$	-	2.4	-	ns
	Q2			-	5.6	-	
Rise time	Q1	t_r		-	3.6	-	
	Q2			-	5.6	-	
Turn-off delay time	Q1	$t_{d(off)}$		-	13	-	
	Q2			-	28	-	
Fall time	Q1	t_f		-	2.4	-	
	Q2			-	4.1	-	

Gate Charge Characteristics

Gate to source charge	Q1	Q_{gs}	$V_{DD}=12\text{ V},$ $I_D=30\text{ A},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	1.9	2.5	nC
Gate to drain charge		Q_{gd}		-	1.2	1.8	
Switching charge		Q_g		-	5.0	6.6	
Gate plateau voltage		$V_{plateau}$		-	2.5	-	V
Gate to source charge	Q2	Q_{gs}		-	8.1	10.8	
Gate to drain charge		Q_{gd}		-	5.6	8.4	
Switching charge		Q_g		-	23	30.6	
Gate plateau voltage		$V_{plateau}$		-	2.4	-	
Output charge	Q1	Q_{oss}	$V_{DD}=12\text{ V}, V_{GS}=0\text{ V}$	-	8	10.6	nC
	Q2			-	36	48	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Reverse Diode

Diode continuous forward current	Q1	I_S	$T_C=25\text{ °C}$	-	-	28	A
	Q2			-	-	40	
Diode pulse current	Q1	$I_{S,pulse}$		-	-	160	
	Q2			-	-	160	
Diode forward voltage	Q1	V_{SD}	$V_{GS}=0\text{ V}, I_F=20\text{ A}, T_j=25\text{ °C}$	-	0.87	1	V
	Q2		$V_{GS}=0\text{ V}, I_F=10\text{ A}, T_j=25\text{ °C}$	-	0.56	0.7	
Reverse recovery charge	Q1	Q_{rr}	$V_R=12\text{ V}, I_F=10\text{ A}, di_F/dt=400\text{ A/}\mu\text{s}$	-	5	-	nC
	Q2			-	5	-	nC

¹⁾ J-STD20 and JESD22

²⁾ One transistor active

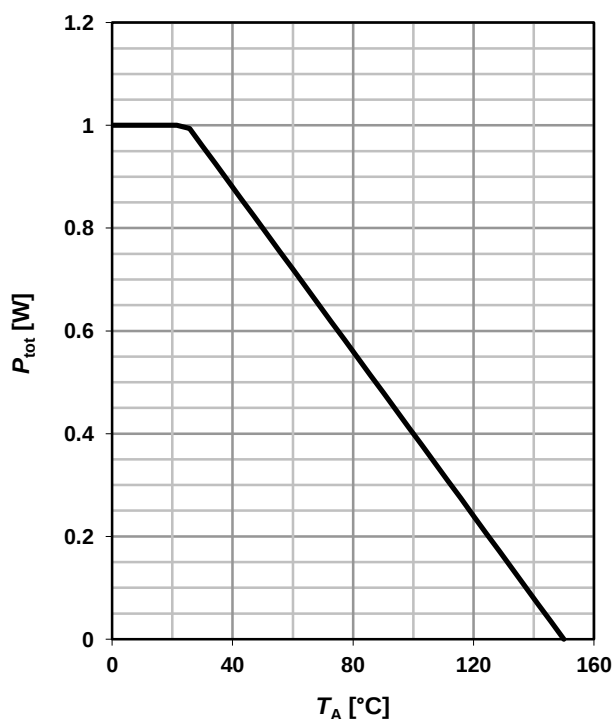
³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is

⁴⁾ Device mounted on a minimum pad (one layer, 70 μm thick). One transistor active.

⁵⁾ See figure 3 for more detailed information.

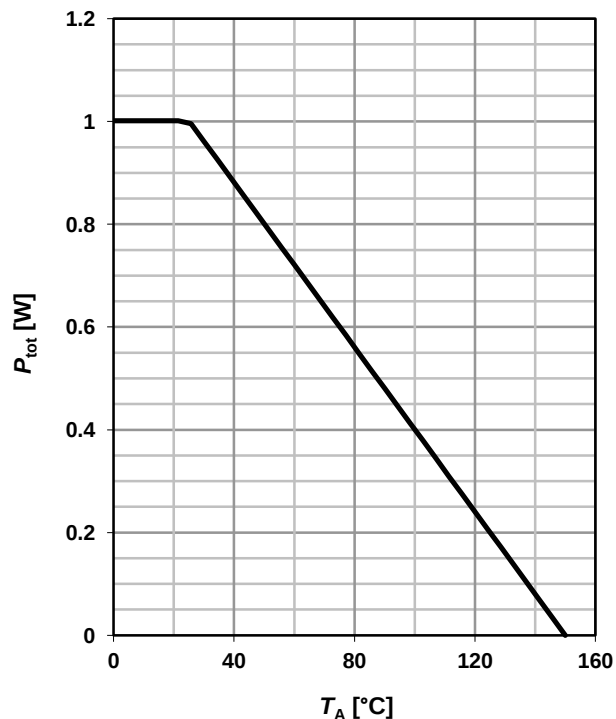
1 Power dissipation (Q1)

$$P_{\text{tot}} = f(T_A)^{(3)}$$



2 Power dissipation (Q2)

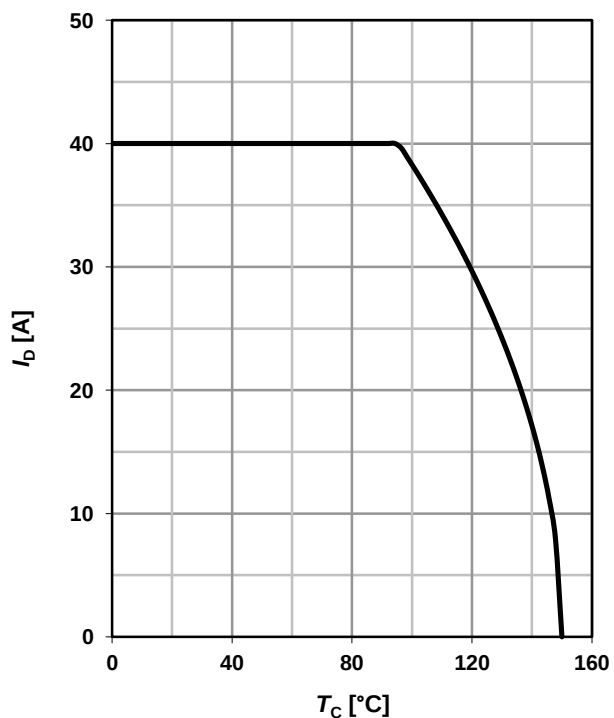
$$P_{\text{tot}} = f(T_A)^{(3)}$$



3 Drain current (Q1)

$$I_D = f(T_C)$$

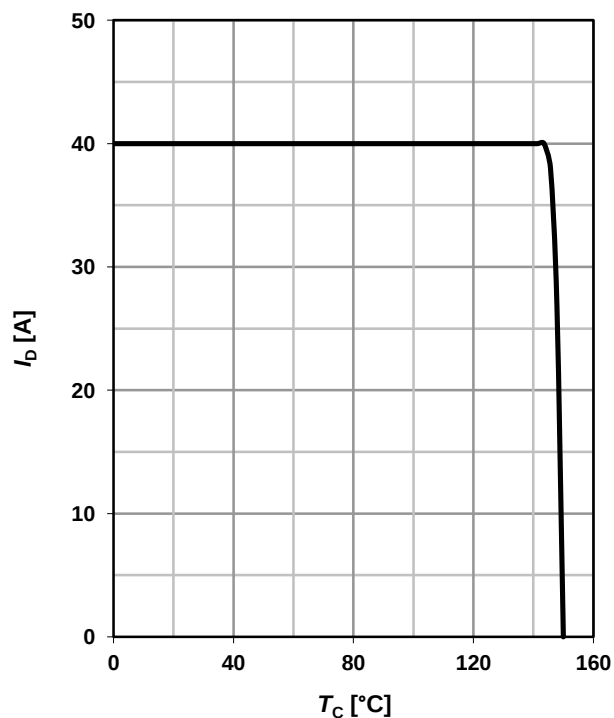
parameter: $V_{GS} \geq 10$ V



4 Drain current (Q2)

$$I_D = f(T_C)$$

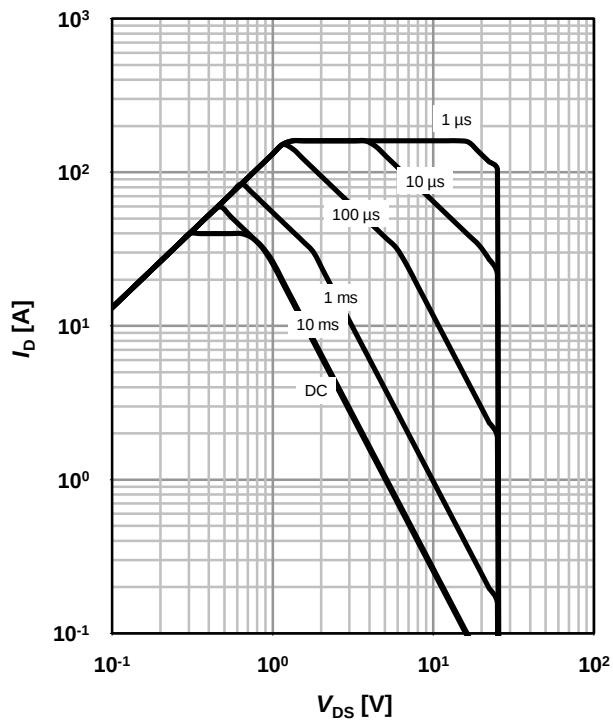
parameter: $V_{GS} \geq 10$ V



5 Safe operating area (Q1)

$$I_D = f(V_{DS}); T_C = 25^\circ\text{C}; D = 0$$

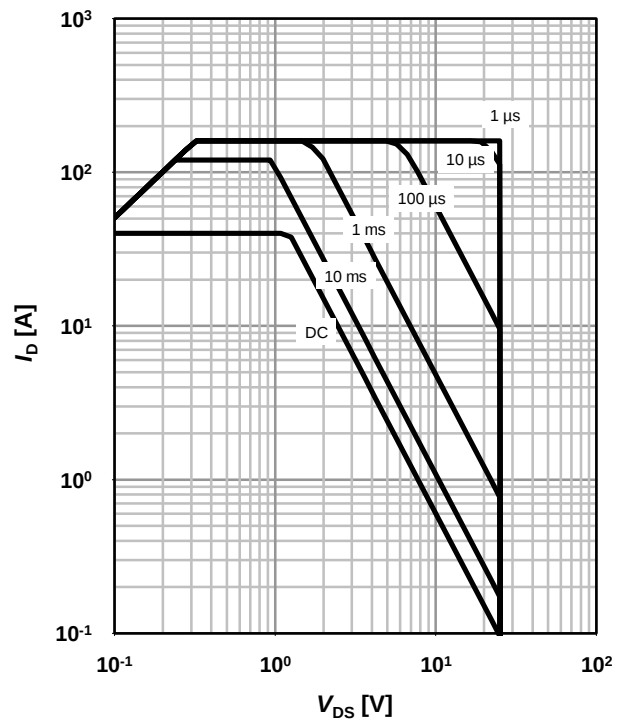
parameter: t_p



6 Safe operating area (Q2)

$$I_D = f(V_{DS}); T_C = 25^\circ\text{C}; D = 0$$

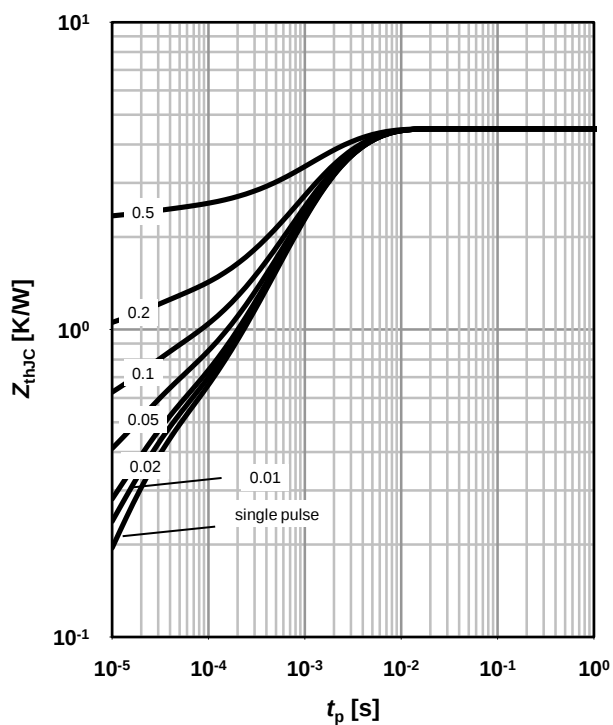
parameter: t_p



7 Max. transient thermal impedance (Q1)

$$Z_{thJC} = f(t_p)$$

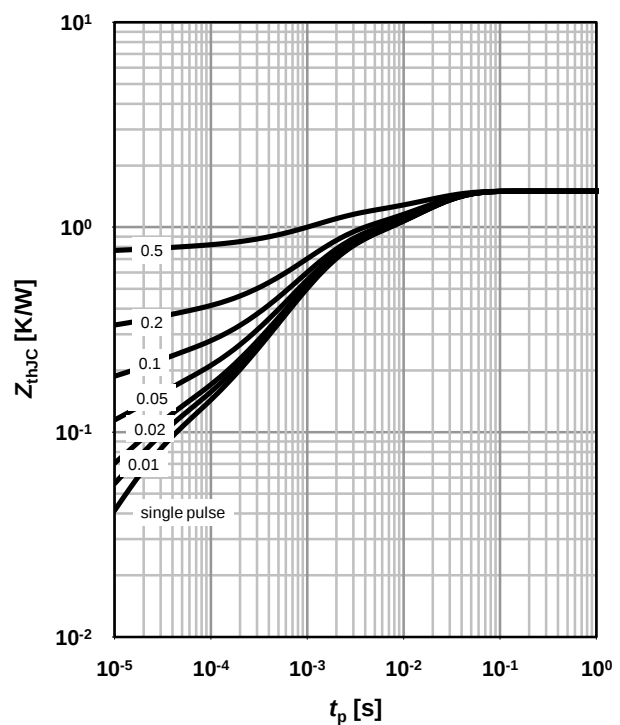
parameter: $D = t_p/T$



8 Max. transient thermal impedance (Q2)

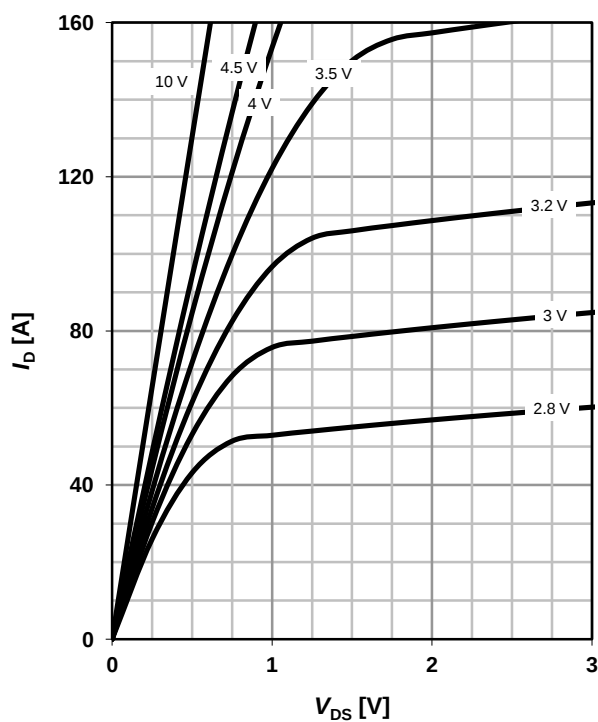
$$Z_{thJC} = f(t_p)$$

parameter: $D = t_p/T$



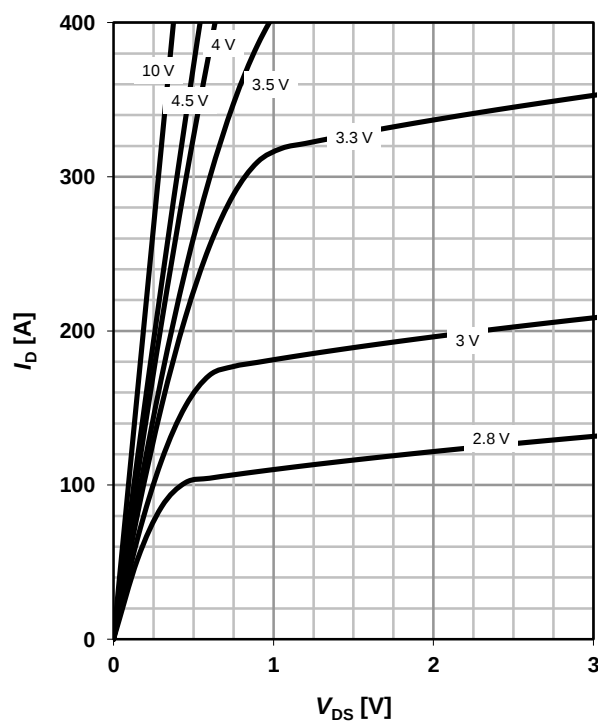
9 Typ. output characteristics (Q1)

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


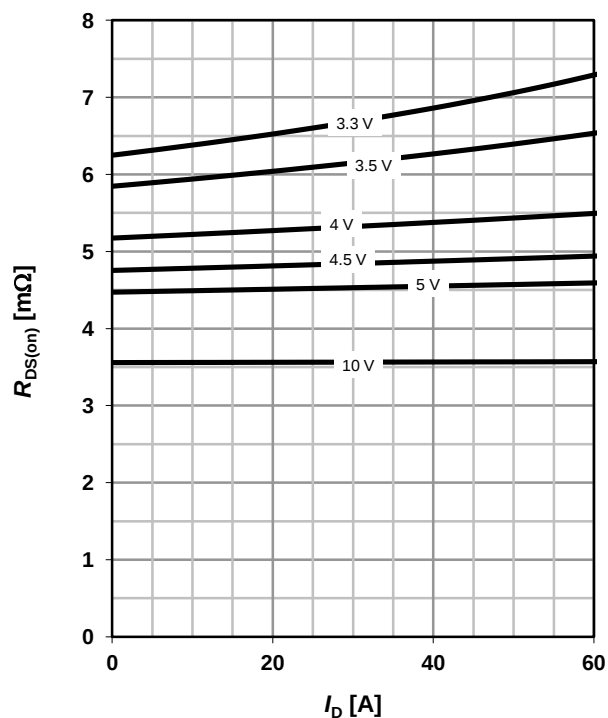
10 Typ. output characteristics (Q2)

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


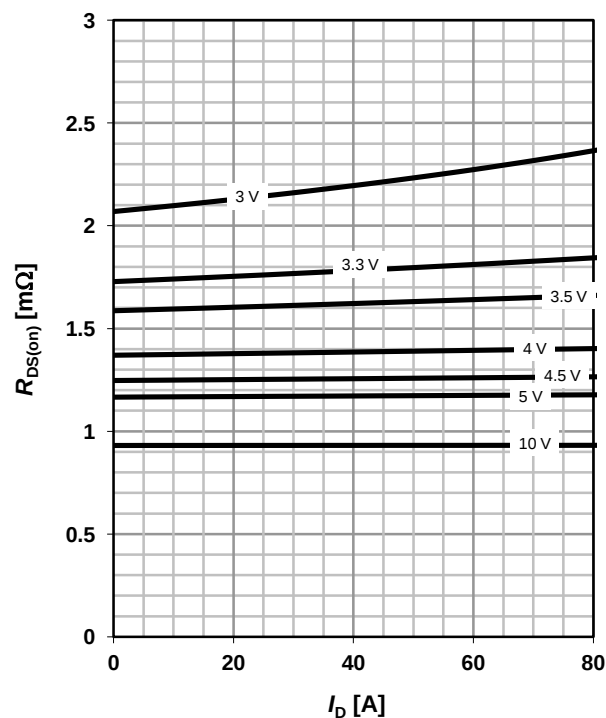
11 Typ. drain-source on resistance (Q1)

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

parameter: V_{GS}


12 Typ. drain-source on resistance (Q2)

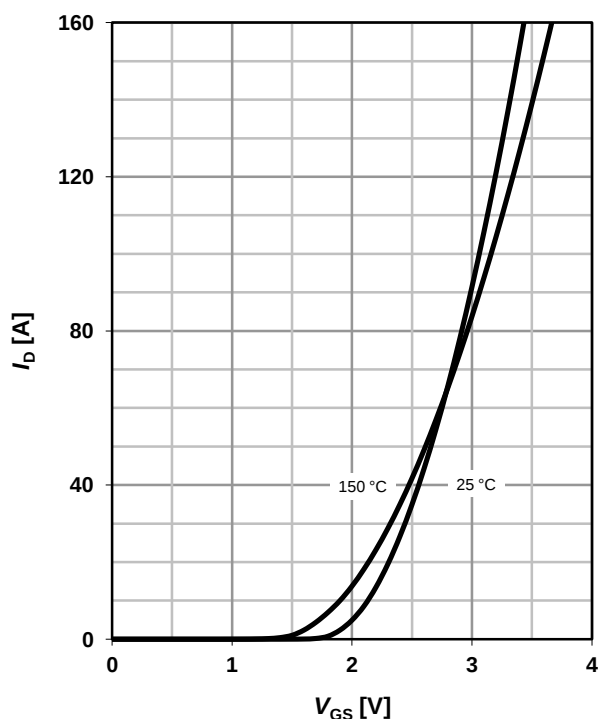
 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

parameter: V_{GS}


13 Typ. transfer characteristics (Q1)

$$I_D = f(V_{GS}); |V_{DS}| > 2 |I_D| R_{DS(on)max}$$

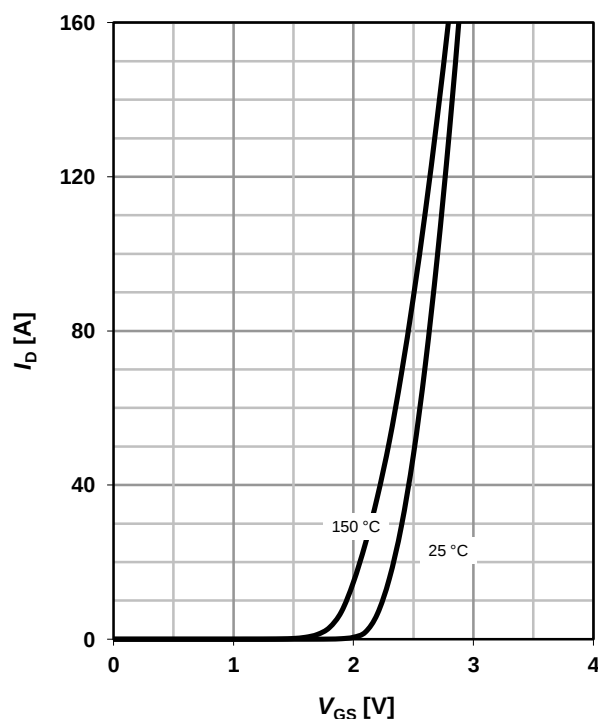
parameter: T_j



14 Typ. transfer characteristics (Q2)

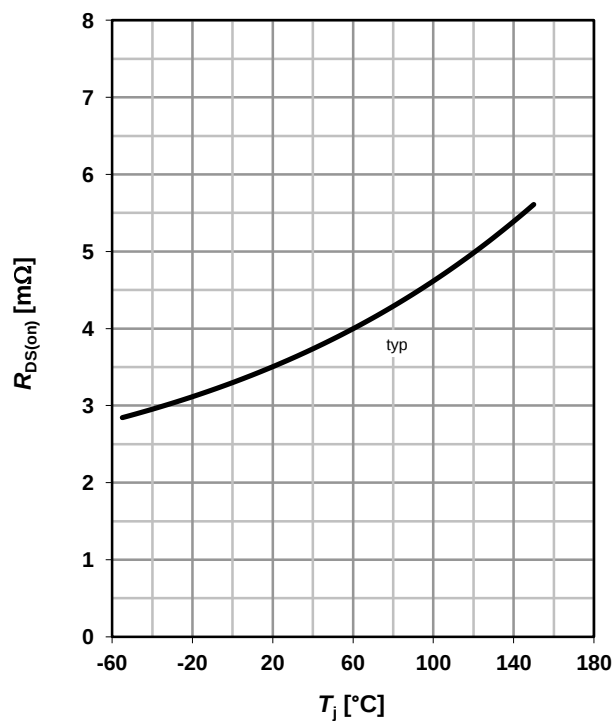
$$I_D = f(V_{GS}); |V_{DS}| > 2 |I_D| R_{DS(on)max}$$

parameter: T_j



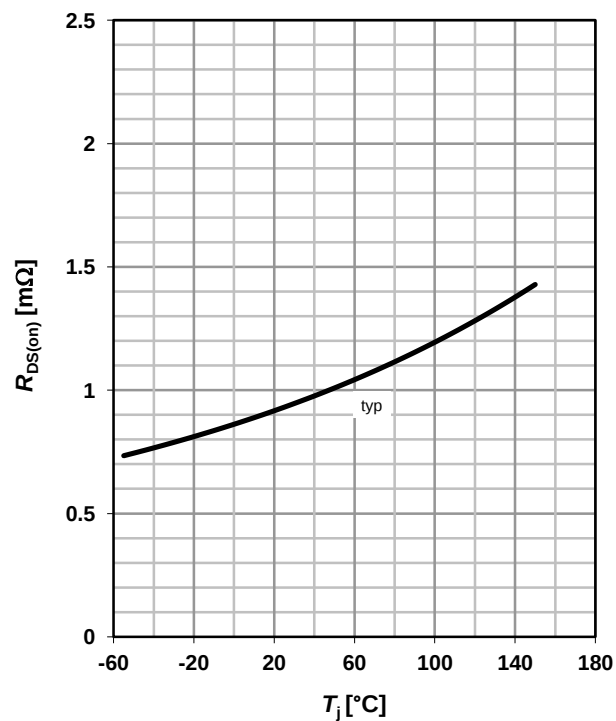
15 Drain-source on-state resistance (Q1)

$$R_{DS(on)} = f(T_j); I_D = 25 \text{ A}; V_{GS} = 10 \text{ V}$$

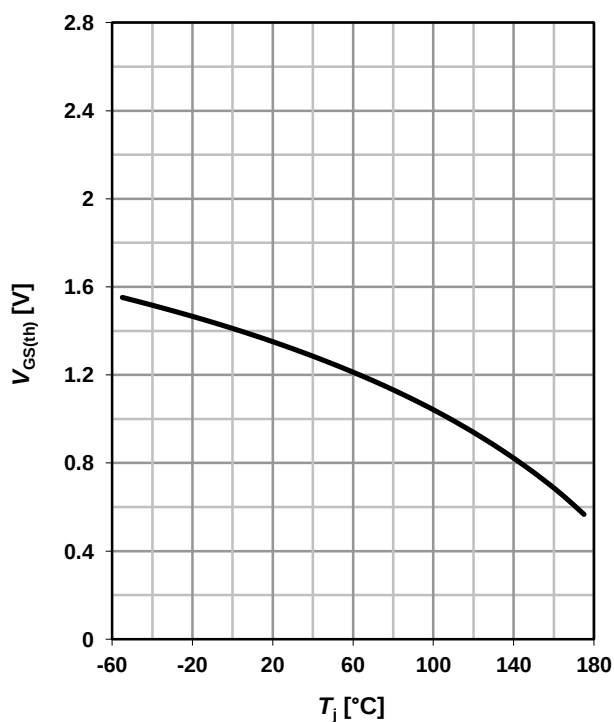


16 Drain-source on-state resistance (Q2)

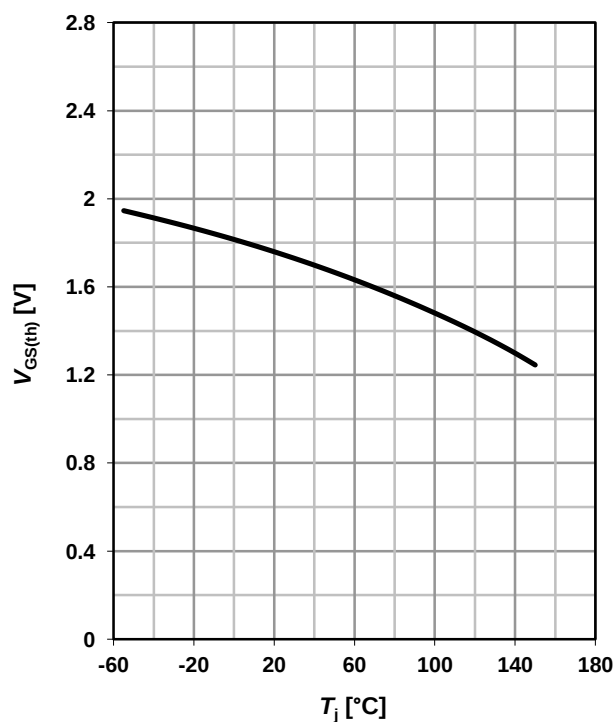
$$R_{DS(on)} = f(T_j); I_D = 25 \text{ A}; V_{GS} = 10 \text{ V}$$



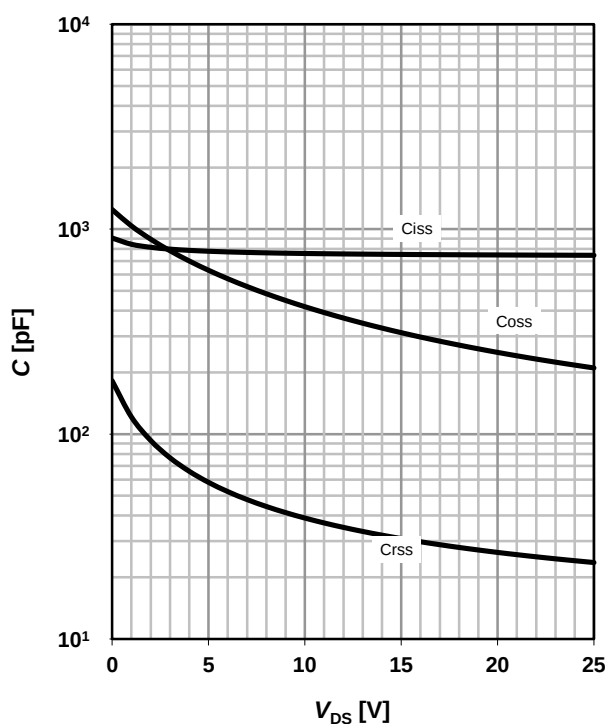
17 Typ. gate threshold voltage (Q1)

 $V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = 250 \mu A$


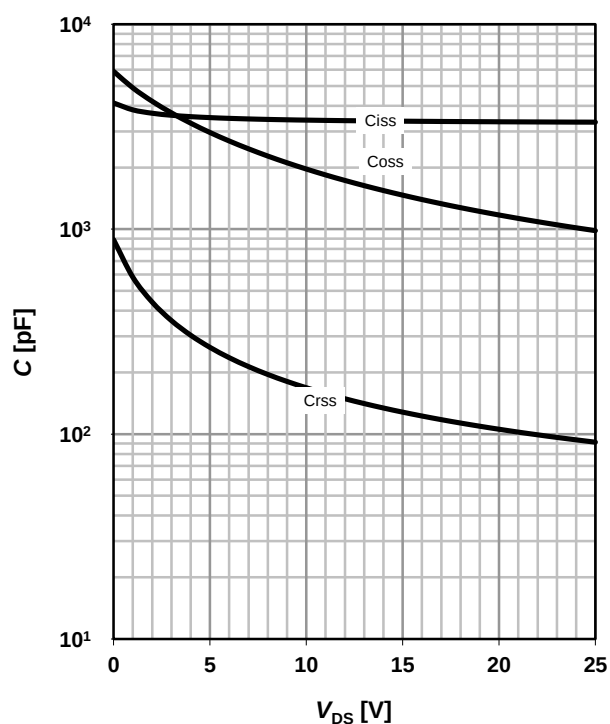
18 Typ. gate threshold voltage (Q2)

 $V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = 10 \text{ mA}$


19 Typ. capacitances (Q1)

 $C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$


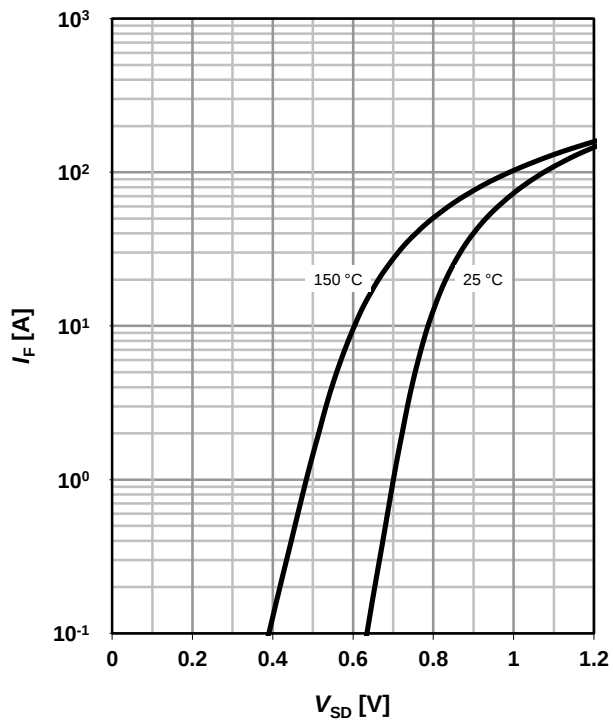
20 Typ. capacitances (Q2)

 $C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$


21 Forward characteristics of reverse diode (Q1)

$$I_F = f(V_{SD})$$

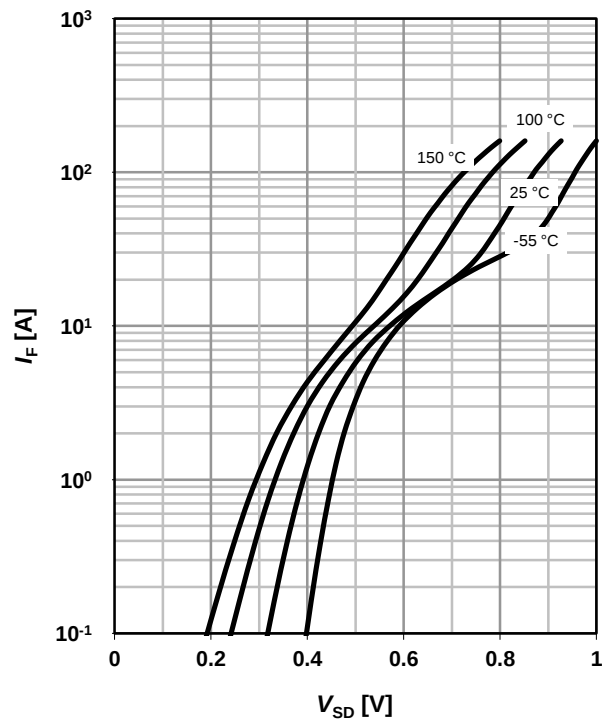
parameter: T_j



22 Forward characteristics of reverse diode (Q2)

$$I_F = f(V_{SD})$$

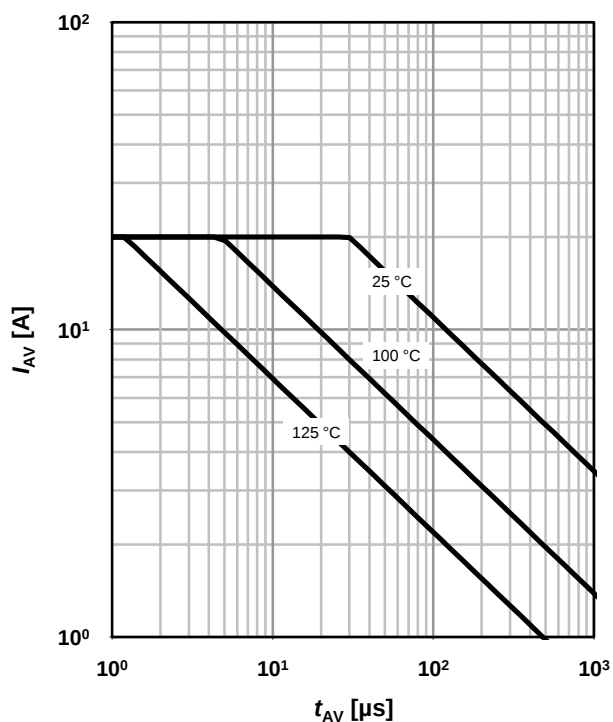
parameter: T_j



23 Avalanche characteristics (Q1)

$$I_{AS} = f(t_{AV}); R_{GS} = 25 \Omega$$

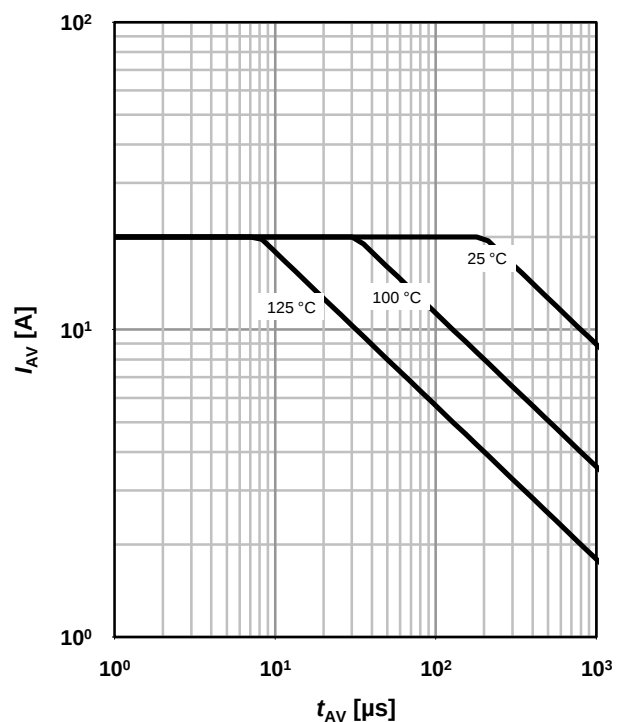
parameter: $T_{j(\text{start})}$



24 Avalanche characteristics (Q2)

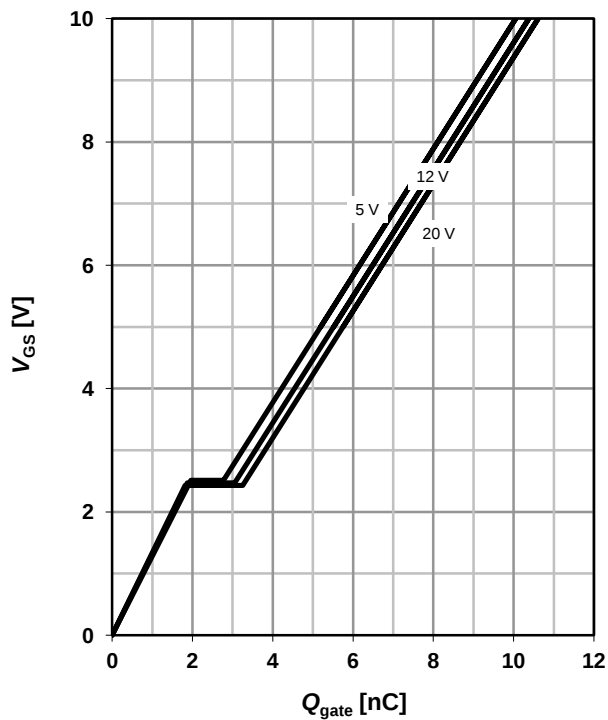
$$I_{AS} = f(t_{AV}); R_{GS} = 25 \Omega$$

parameter: $T_{j(\text{start})}$



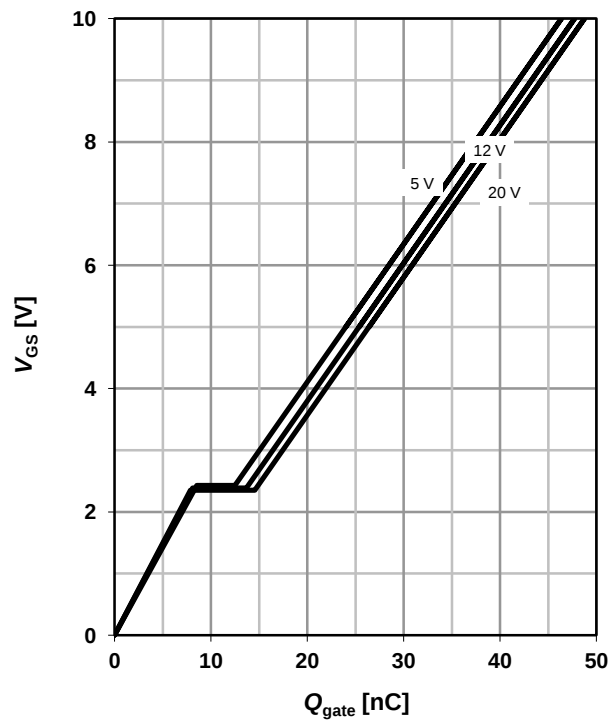
25 Typ. gate charge (Q1)

 $V_{GS}=f(Q_{gate}); I_D=20\text{ A pulsed}$

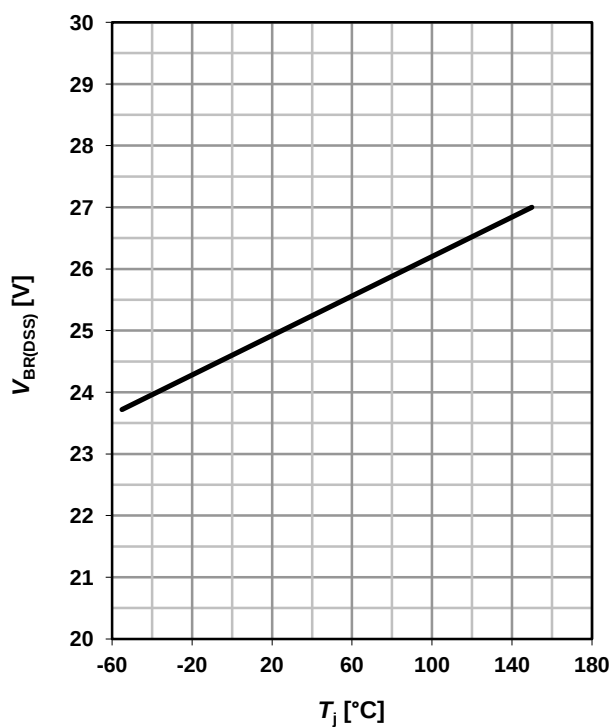
parameter: V_{DD}


26 Typ. gate charge (Q2)

 $V_{GS}=f(Q_{gate}); I_D=20\text{ A pulsed}$

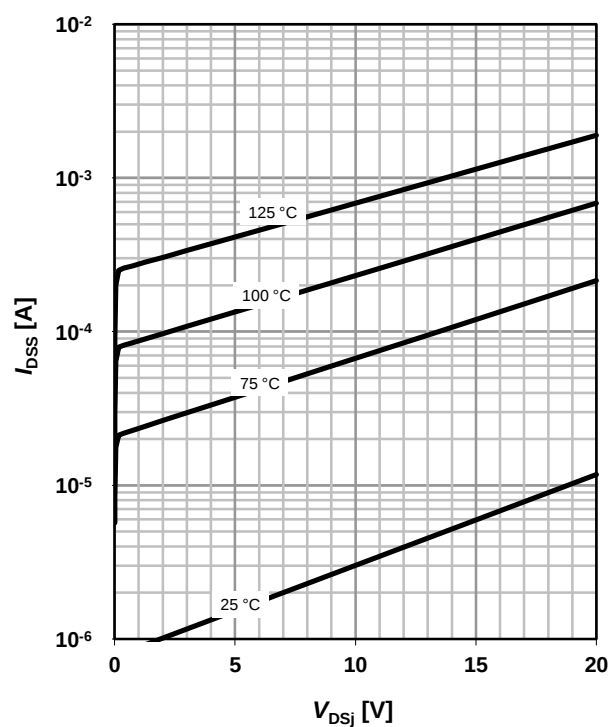
parameter: V_{DD}


27 Drain-source breakdown voltage (Q1)

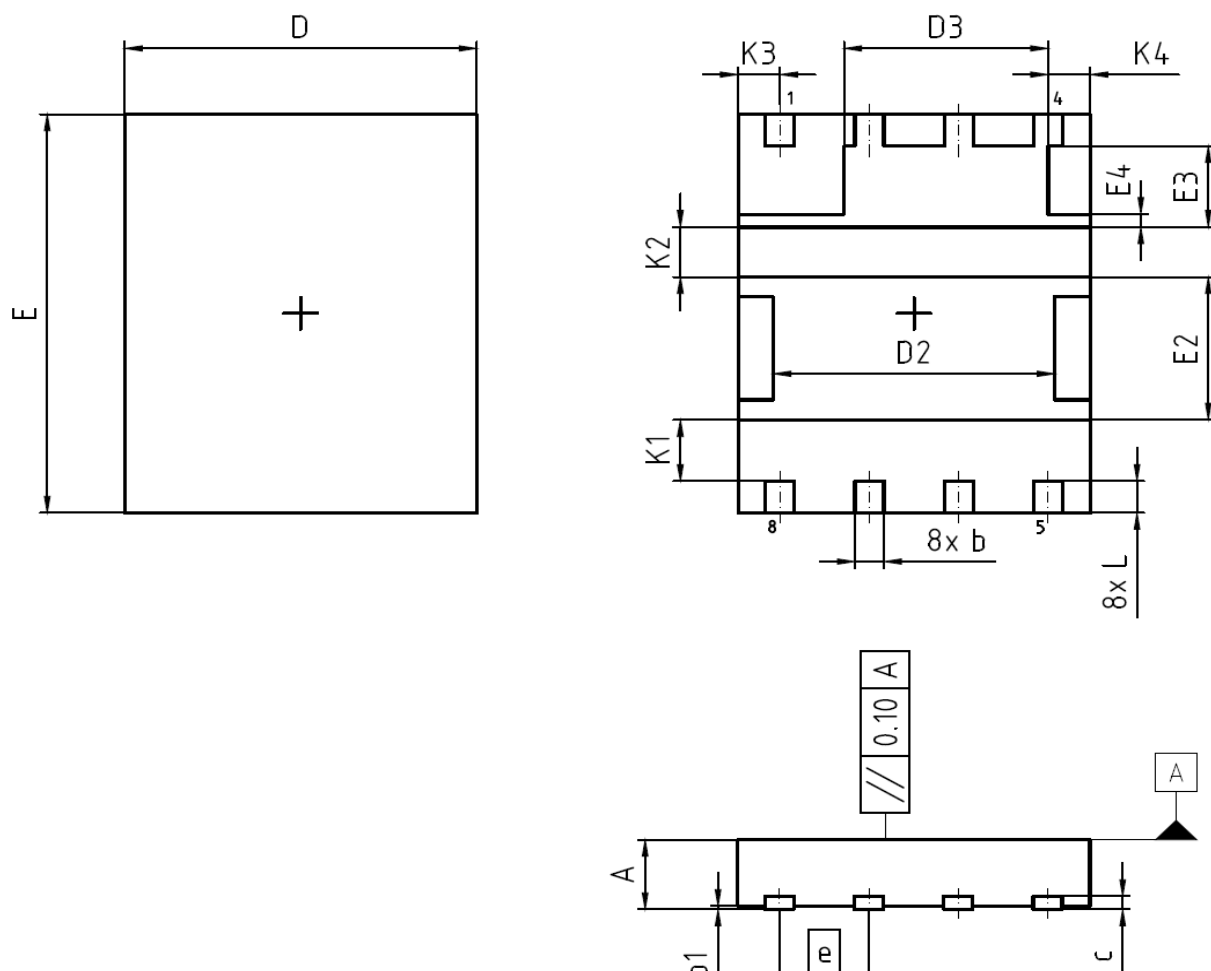
 $V_{BR(DSS)}=f(T_j); I_D=1\text{ mA}$


28 Typ. drain-source leakage current (Q2)

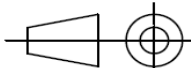
 $I_{DSS}=f(V_{DS}); V_{GS}=0\text{ V}$

parameter: T_j


PG-TISON



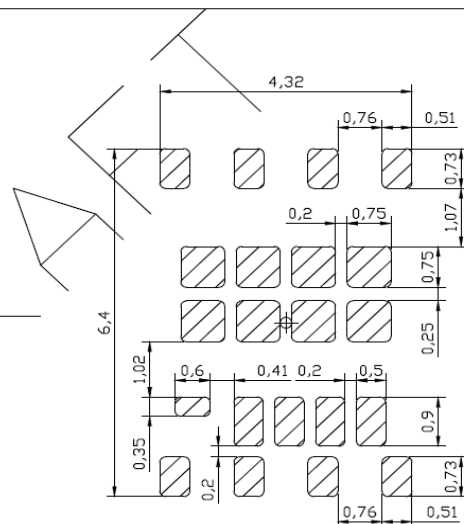
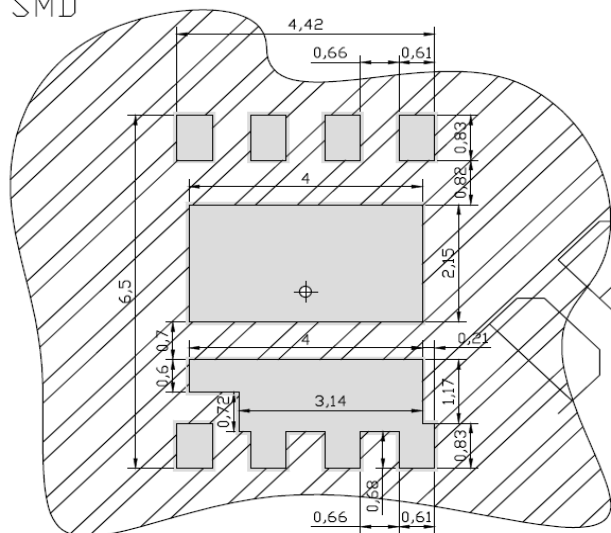
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.15	0.035	0.045
b	0.31	0.51	0.012	0.020
b1	0.00	0.05	0.000	0.002
c	0.10	0.30	0.004	0.012
D	4.90	5.10	0.193	0.201
D2	3.90	4.10	0.154	0.161
D3	2.80	3.00	0.110	0.118
E	5.90	6.10	0.232	0.240
E2	2.05	2.25	0.081	0.089
E3	1.12	1.32	0.044	0.052
E4	0.10	0.30	0.004	0.012
e	1.27 (BSC)		0.05 (BSC)	
N	8		8	
L	0.38	0.58	0.015	0.023
K1	0.82	1.02	0.032	0.040
K2	0.65	0.85	0.026	0.033
K3 = K4	0.50	0.70	0.019	0.027

DOCUMENT NO. Z8B00162738	
SCALE 0 2.5 5mm	
EUROPEAN PROJECTION 	
ISSUE DATE 21-09-2011	
REVISION 01	

PG-TISON-8

Powerstage: Boardpads & Apertures

SMD


(stencil thickness 120 μm)

■ copper

□ solder mask

▨ stencil apertures

Published by
Infineon Technologies AG
81726 Munich, Germany
© 2013 Infineon Technologies AG
All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.