Densitron

TFT DISPLAY MODULE

Product Specification

Customer	Standard	
Product Number	DMT035QVNXNT0-1A	
Customer Part Number		
Customer Approval		**Date:**

Internal Approvals		
Product Mgr	Doc. Control	Electr. Eng
Luo Luo	Luo Luo	Eric Wan
Date: 30/06/17	**Date: 30/06/17**	**Date: 30/06/17**

Revision Record

Rev.	Date	Page	Chapt.	Comment	ECR no.
1.0	26-May-17	All	All	Initial Release	
2.0	30-June-17	9	3.3.1	Improve brightness: Modified Backlight pinout arrangement	
		16	4.1	Modified Colour Chromaticity values	

Table of Contents

1.0 Main Features

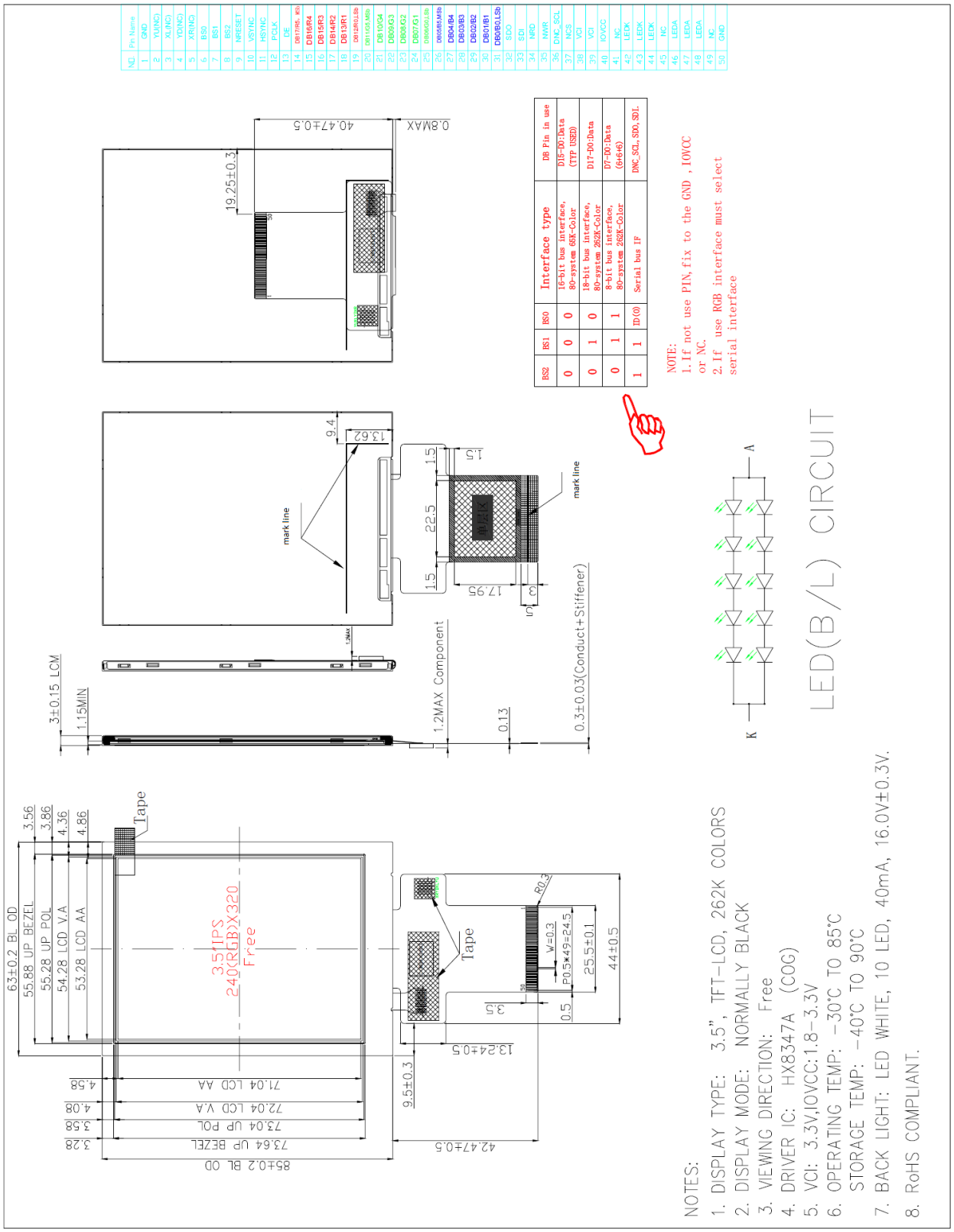
Item	Contents
Screen Size	3.5” Diagonal
Display Format	240 x RGB x 320 Dots
N° of Colour	65K/262K
Active Area	53.28 mm (H) x 71.04 mm (V)
LCD Type	TFT
Mode	IPS Transmissive / Normally Black
Viewing Direction	Full view
Interface	8/16/18-bit DBI Type B (CPU) interface 3-lines SPI +16/18-bit RGB interface; 3-lines SPI
Driver IC	HX8347A or equivalent
Backlight Type	LED
Operating Temperature	-30°C ~ +85°C
Storage Temperature	-40°C ~ +90°C
RoHS compliant	Yes

2.0 Mechanical Specification

2.1 Mechanical Characteristics

Item	Characteristic	Unit
Display Format	240 x RGB x 320 Dots	Dots
Overall Dimensions	63.00 mm (H) x 85.00 mm (V) x 3.0 mm (D)	mm
Active Area	53.28 mm (H) x 71.04 mm (V)	mm
pixel Pitch	222 (H) x 222 (V)	µm
Weight	20	g

2.2 Mechanical Drawing



3.0 Electrical Specification

3.1 Absolute Maximum Ratings

Item	Symbol	Condition	Min	Max	Unit	Note
Power Supply Voltage	VCI		-0.3	4.0	V	
Digital Interface Supply Voltage	IOVCC		-0.3	4.0	V	
Operating Temperature	TOP		-30	85	°C	1
Storage Temperature	TST		-40	90	°C	1,2,3

Note 1. 90 % RH Max for Ta<50 °C, and 60% RH for Ta≥50°C.
Note 2. In case of below 0°C, the response time of liquid crystal (LC) becomes slower and the colour of panel becomes darker than normal one. Level of retardation depends on temperature, because of LC's characteristic.
Note 3. Only operation is guaranteed at operating temperature. Contrast, response time, another display quality are evaluated at +25°C.

3.2 Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Voltage	VCI	Ta=25˚C	2.5	2.8	3.3	V	
Digital Interface Supply Voltage	IOVCC	Ta=25˚C	1.65	1.8	3.3	V	
Input Voltage for Logic	VIH		0.7 IOVCC	-	IOVCC	V	
	VIL		GND	-	0.3 IOVCC	V	
Output Voltage for Logic	VOH		0.8 IOVCC	-	IOVCC	V	
	VOL		GND	-	0.2 IOVCC	V	
Current Consumption	IDD		-	9		mA	1

Note 1: The specified power consumption is under the conditions of VCI=2.8V, FV=60Hz.

3.3 Interface Pin Assignment

3.3.1 TFT Pin Assignment

Recommended connector: MOLEX 51296-5093

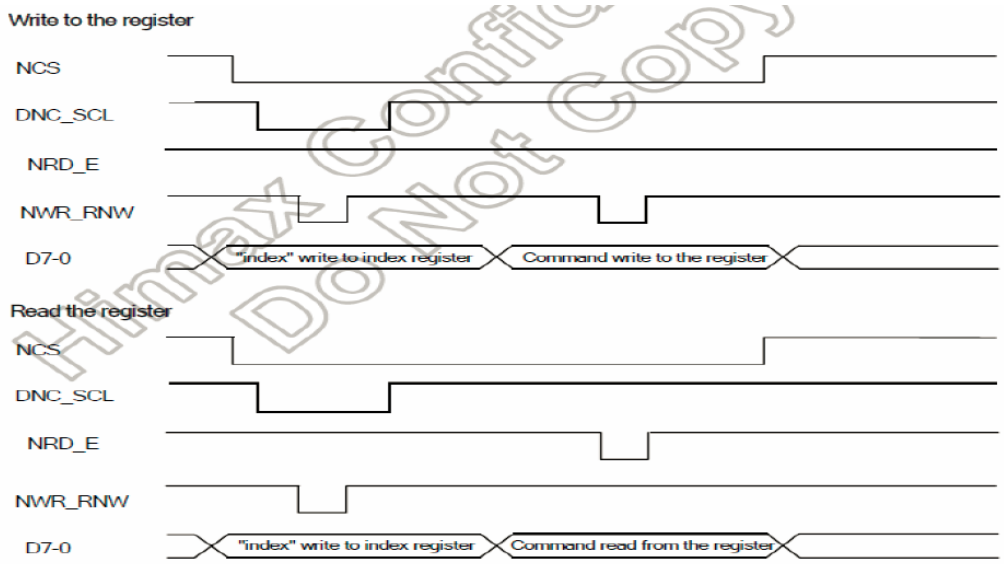
No.	Symbol	Function
1	GND	Ground.
2	XR(NC)	NC.
3	YD(NC)	NC.
4	XL(NC)	NC.
5	YU(NC)	NC.
6	BS0	Interface selecting mode signal. MPU Parallel interface bus and serial interface select if use RGB interface must select serial interface.
7	BS1	
8	BS2	
9	NRESET	This signal will reset the device and must be applied to properly initialize the chip
10	VSYNC	Frame synchronizing signal for RGB Interface mode. If not used, please connect to GND or IOVCC.
11	HSYNC	Line synchronizing signal for RGB Interface mode. If not used, please connect to GND or IOVCC.
12	PCLK	Pixel clock signal for RGB Interface mode. If not used, please connect to GND or IOVCC.
13	DE	A DATA ENABLE signal for RGB Interface mode. If not used, please connect to GND or IOVCC.
14-31	DB17-DB0	Data bus PINS. 18-bit bi-directional data bus for MCU system and RGB interface mode. 8-bit bus: use DB7-DB0 and D17-D8 unused 16-bit bus: use DB15-DB0 and D17-16 unused 18-bit bus: use DB17-DB0 Pins not used must be connected to GND.
32	SDO	Serial data output pin in serial bus system interface. If not used, please open this pin.
33	SDI	Serial input signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at GND or IOVCC.
34	NRD	Serves as a read signal and read data at the rising edge. If not used, please connect to GND or IOVCC.
35	NWR	Serves as a write signal and write data at the rising edge. If not used, please connect to GND or IOVCC.

No.	Symbol	Function
36	DNC_SCL	When under serial interface, it servers as SCL.
37	NCS	Chip select signal. Low: chip can be accessed; High: chip cannot be accessed. If not used, please connect to GND.
38-39	VCI	Supply voltage (VCI=3.3V).
40	IOVCC	Supply voltage for IO (IOVCC=1.8V-3.3V).
41	NC	Not connected
42-44	LEDK1-LEDK3	Power supply for Backlight.
45	NC	Not connected
46-48	LEDA1-LEDA3	Power supply for Backlight.
49	NC	Not connected
50	GND	Ground.

3.4 Timing Characteristics

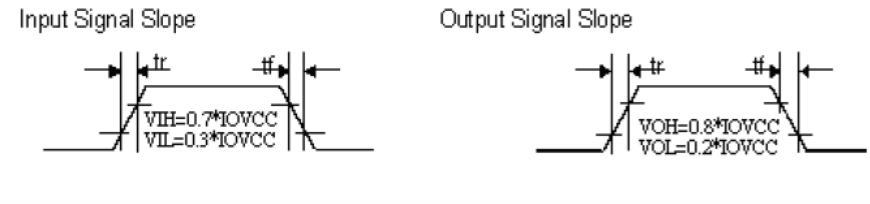
Please refer to Himax IC HX8347A datasheet for more information

3.4.1 Display Parallel Interface Timing Characteristics (8080 system)



Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DNC_SCL	t_{AST}	Address setup time	10	-	ns	-
	t_{AHT}	Address hold time (Write/Read)	10	-		
NCS	t_{CHW}	Chip select "H" pulse width	0	-	ns	-
	t_{CS}	Chip select setup time (Write)	35	-		
	t_{RCSFM}	Chip select setup time	180	-		
	t_{CSF}	Chip select wait time (Write/Read)	10	-		
	t_{CSH}	Chip select hold time	10	-		
NWR_RNW	t_{WC}	Write cycle	100	-	ns	-
	t_{WRH}	Control pulse "H" duration	15	-		
	t_{WRL}	Control pulse "L" duration	20	-		
NRD_E	t_{RCFM}	Read cycle	250	-	ns	When read from GRAM
	t_{RDHFM}	Control pulse "H" duration	15	-		
	t_{RDLFM}	Control pulse "L" duration	180	-		
D17 to D0	t_{DST}	Data setup time	10	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	t_{DHT}	Data hold time	10	-		
	t_{RAT}	Read access time (ID)	-	180		
	t_{RATFM}	Read access time (FM)	-	340		
	t_{ODH}	Output disable time	20	80		

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.



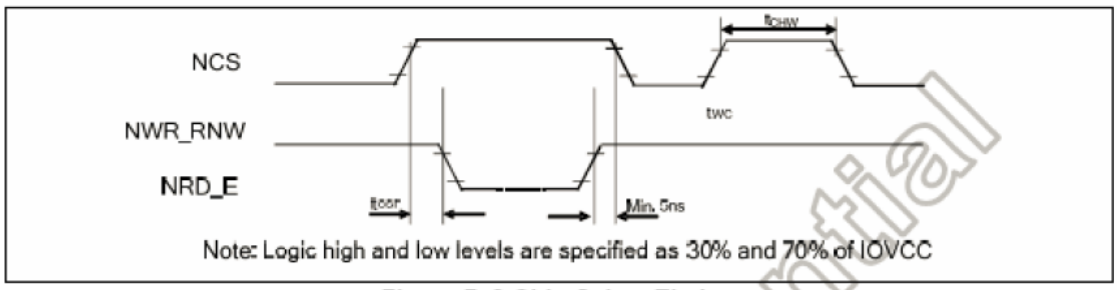
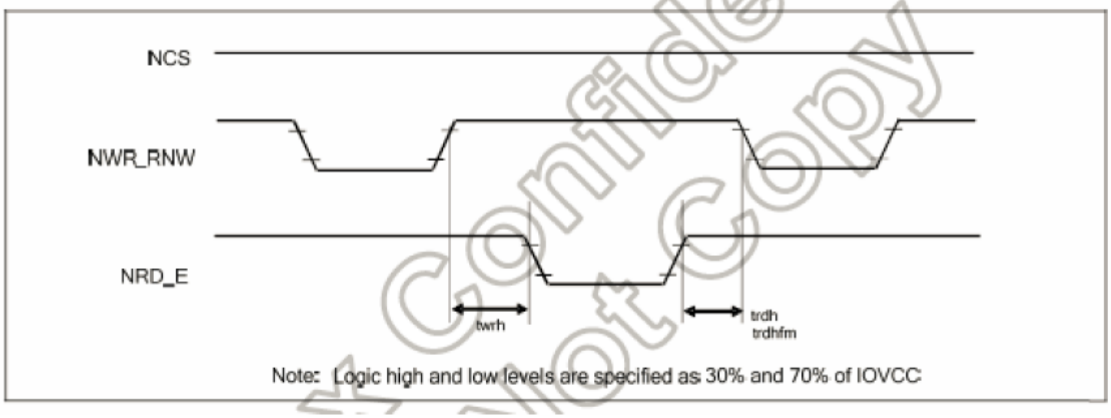
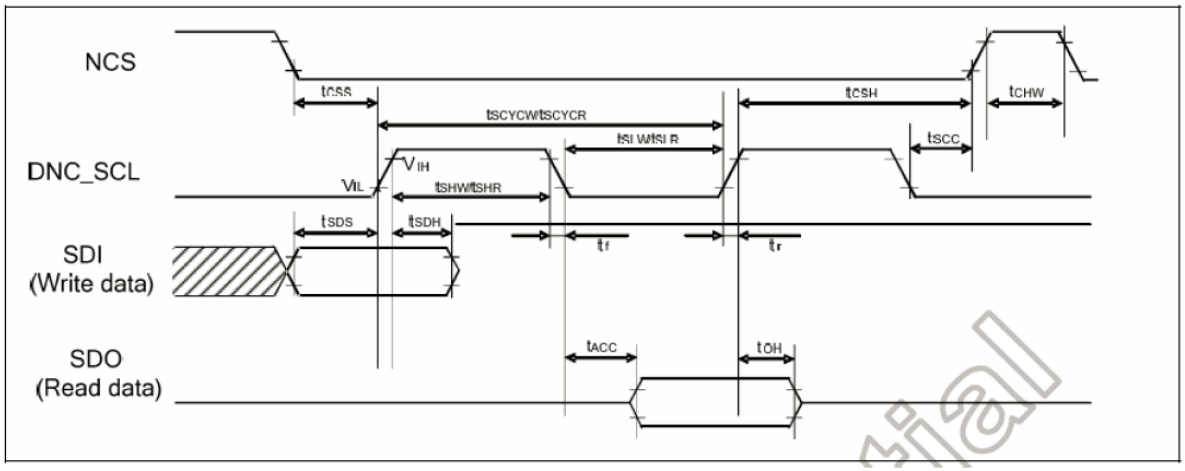


Figure 7. 2 Chip Select Timing



3.4.2 Display Serial Interface Timing Characteristics (3-line SPI system)

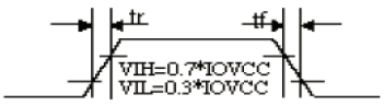


(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V,Ta = -40 to 85° C)

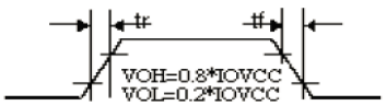
Parameter	Symbol	Conditions	Min.	Typ.	Maz.	Unit
Serial clock cycle (Write)	t_{SCYCW}	DNC_SCL	100	-	-	ns
DNC_SCL "H" pulse width (Write)	t_{SHW}		35	-	-	
DNC_SCL "L" pulse width (Write)	t_{SLW}		35	-	-	
Data setup time (Write)	t_{SDS}	SDI	30	-	-	ns
Data hold time (Write)	t_{SDH}		30	-	-	
Serial clock cycle (Read)	t_{SCYCR}	DNC_SCL	150	-	-	ns
DNC_SCL "H" pulse width (Read)	t_{SHR}		60	-	-	
DNC_SCL "L" pulse width (Read)	t_{SLR}		100	-	-	
Access Time	t_{ACC}	SDO for maximum C_L=30pF For minimum C_L=8pF	10	-	100	ns
Output disable time	t_{OH}	SDO For maximum C_L=30pF For minimum C_L=8pF	15	-	100	ns
DNC_SCL to Chip select	t_{SCC}	DNC_SCL, NCS	50	-	-	ns
NCS "H" pulse width	t_{CHW}	NCS	45	-	-	ns
Chip select setup time	t_{CSS}	NCS	60	-	-	ns
Chip select hold time	t_{CSH}		80	-	-	

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

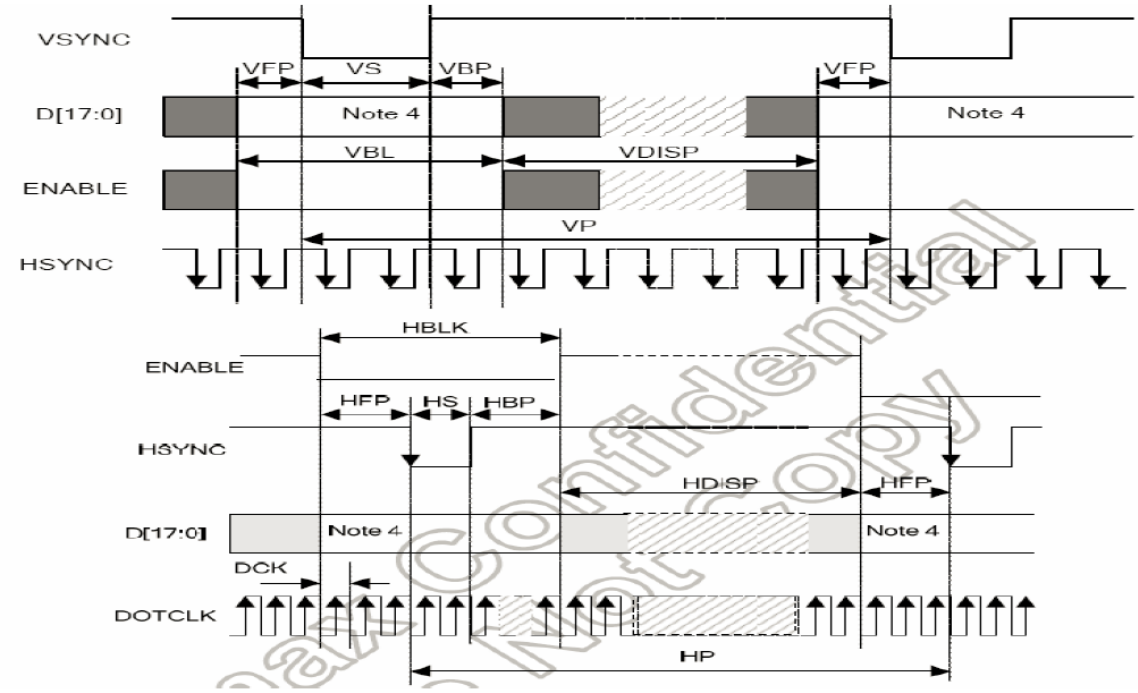
Input Signal Slope

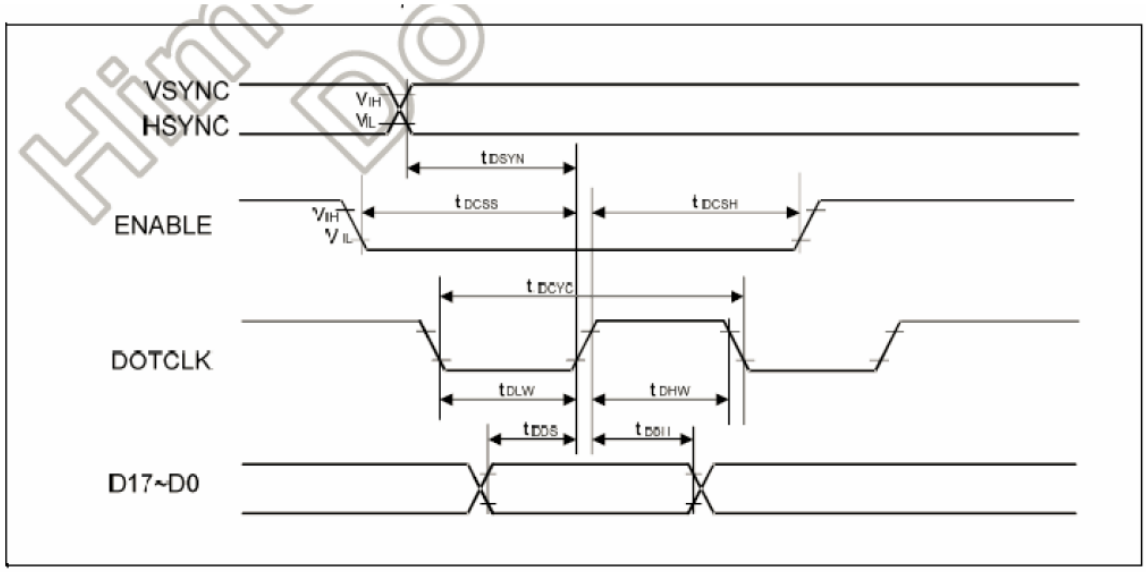


Output Signal Slope



3.4.3 Parallel RGB Interface Timing Characteristics

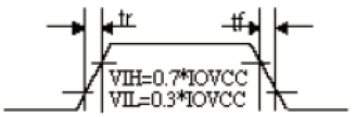




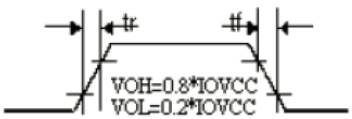
Symbol	Parameter	Conditions	Related Pins	Min.	Typ.	Max.	Unit
VS	VSYNC Low Pulse Width	-	VSYNC	1	-	-	Line
VBP	Vertical Back Porch	-	VSYNC	1	-	-	Line
VFP	Vertical Front Porch	-	VSYNC	1	-	-	Line
VDISP	Vertical Active Area	-	VSYNC, HSYNC	-	320	-	Line
HS	HSYNC Low Pulse Width	-	HSYNC	2	-	-	DOTCLK
HBP	Horizontal Back Porch	-	HSYNC	2	-	-	DOTCLK
HFP	Horizontal Front Porch	-	HSYNC	2	-	-	DOTCLK
HDISP	Horizontal Active Area	-	HSYNC, DOTCLK	-	240	-	DOTCLK
t_{DCYC}	DOTCLK cycle time	VRR = Min . 50 Hz Max. 65 Hz	DOTCLK	100 (note2)		226 (note3)	ns
t_{DLW} t_{CHW}	DOTCLK Low time DOTCLK High time	-		50 15	-	- -	ns
t_{DDS} t_{DDH}	RGB Data setup time RGB Data hold time	-	DOTCLK, D17-D0	15 15	- -	- -	ns
t_{DCSS} t_{DCSH}	ENABLE setup time ENABLE hold Time	-	ENABLE	15 15	-	-	ns
t_{DSYN}	SYNC setup time	-	DOTCLK, HSYNC, VSYNC	15	-	-	ns

Note: (1) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(2) 16.6 MHz
(3) 4.4MHz
(4) Data line can be set to "H" or "L" during blanking time – Don't care.

Input Signal Slope



Output Signal Slope



3.4.4 Reset Timing Characteristics

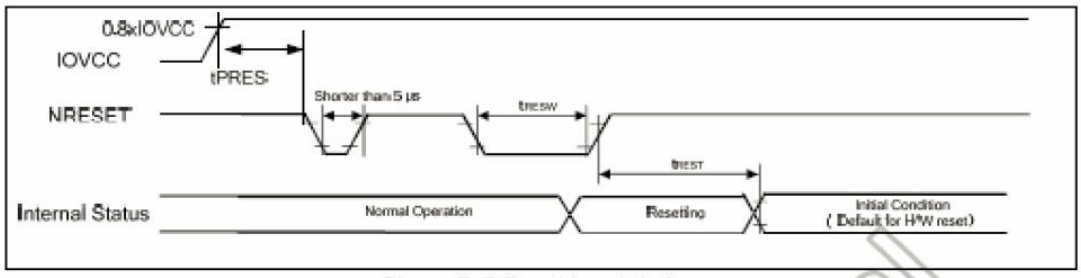


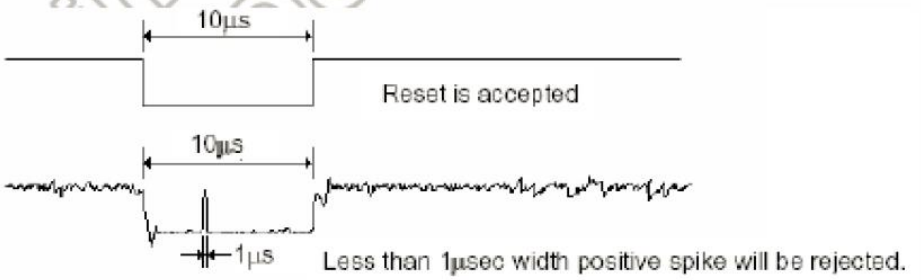
Figure 7. 7 Reset input timing

Symbol	Parameter	Related Pins	Min.	Typ.	Max.	Note	Unit
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	-	-	5	When reset applied during STB mode	ms
		-		-	120	When reset applied during STB mode	ms
tPRES	Reset goes high level after Power on time	NRESET & IOVCC	1	-	-	Reset goes high level after Power on	ms

Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the table below.

NRESET Pulse	Action
Shorter than 5 µ	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in STB Out –mode. The display remains the blank state in STB –mode) and then return to Default condition for H/W reset.
(3) During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.
(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) It is necessary to wait 5msec after releasing !RES before sending commands. Also STB Out command cannot be sent for 120msec.

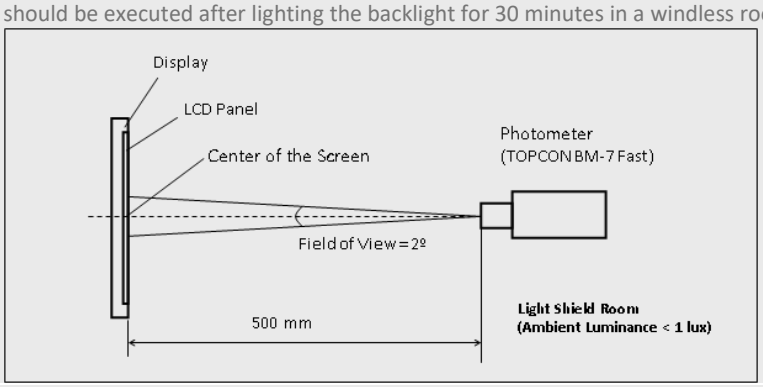
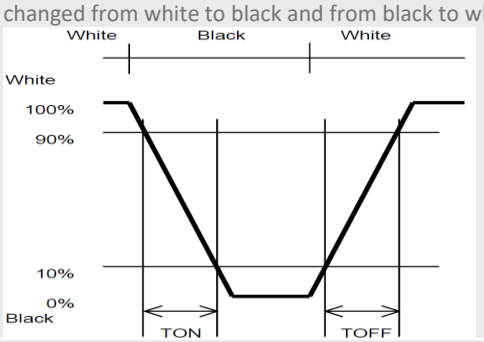
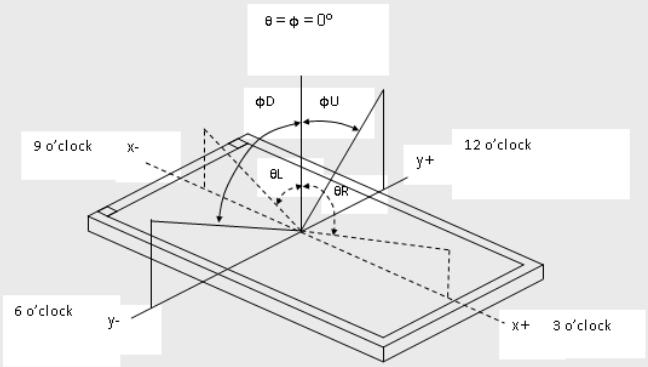
4.0 Optical Specification

4.1 Optical Characteristics

Measuring instruments: LCD-5100, Eldim, Topcon BM-7
Driving condition: VCI = 3.3V, VSS = 0V
Backlight: IF=40mA
Measured temperature: Ta ＝ 25 ˚C

Item		Symbol	Condition	Min	Typ	Max	Unit	Note
Response Time		TR+TF	θ=Φ=0° Normal Viewing Angle	-	35	45	ms	2
Contrast Ratio		CR		600	800	-		3
Viewing Angle	Left	θL	CR ≥ 10	-	80	-	deg	4
	Right	θR		-	80	-	deg	
	Up	ϕU		-	80	-	deg	
	Down	ϕD		-	80	-	deg	
Colour Chromaticity	Red	Rx	CR ≥ 10	0.618	0.620	0.622	-	5
		Ry		0.338	0.340	0.342	-	
	Green	Gx		0.328	0.346	0.366	-	
		Gy		0.604	0.624	0.644	-	
	Blue	Bx		0.129	0.149	0.169	-	
		By		0.033	0.035	0.037	-	
	White	Wx		0.302	0.342	0.382	-	
		Wy		0.319	0.359	0.399	-	
Centre Brightness				450	500	-	cd/m²	6
Brightness Distribution				80	-	-	%	7

4.1.1 Test Method

Note	Item	Test Method
1	Setup	The display should be stabilised at a given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilise the luminance, measurements should be executed after lighting the backlight for 30 minutes in a windless room. 
2	Response time	Measure output signal waveform by the luminance meter when raster of window pattern is changed from white to black and from black to white. 
3	Contrast ratio	Measure maximum brightness and minimum brightness at the centre of the screen by displaying raster or window pattern. Then calculate the ratio between these two values. Contrast Ratio (CR) = Brightness of unselected position (white) / Brightness of selected position (black)
4	Viewing angle Horizontal θ Vertical Ø	Move the luminance meter from right to left and up and down and determinate the angles where contrast ratio is 10 
5	Colour chromaticity	Measure chromaticity coordinates x and y of CIE1931 colorimetric system
6	Centre brightness	Measure the brightness at the centre of the screen
7	Brightness distribution	(Brightness distribution) = 100 x B/A % A: max. brightness of the 9 points B: min. brightness of the 9 points

5.0 Backlight Specification

5.1 LED Driving Conditions

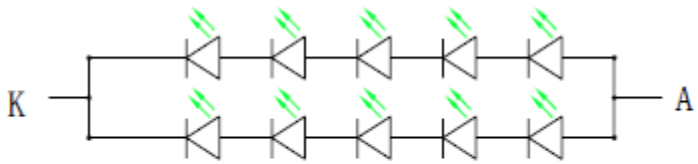
Item	Symbol	Condition	Min	Typ	Max	Unit
Forward Current	IF	Ta=25 °C	30	40	-	mA
Forward Voltage	VF	Ta= 25°C		16		V
LED life time	Hr				50k	hour

Note:

- The lifetime of the LED is defined as a period till the brightness of the LED decreases to the half of its initial value.
- This figure is given as a reference purpose only, and not a guarantee.
- This figure is estimated for an LED operating alone.
  The performance of an LED may differ when assembled as a monitor together with a TFT panel due to different environmental temperature.
- Estimated lifetime could vary on a different temperature and usually higher temperature could reduce the life significantly.

5.2 LED Circuit

LED Circuit Drawing



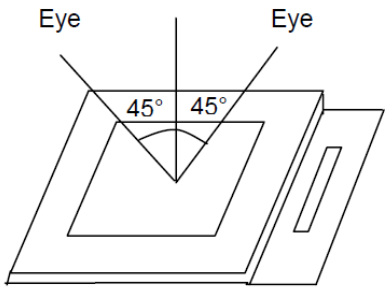
LED(B/L) CIRCUIT

6.0 Quality Assurance Specification

6.1 Delivery Inspection Standards

6.1.1 Inspection Conditions

Inspection distance: 30 cm ± 2 cm
Viewing angle: ±45°



6.1.2 Environmental Conditions

Ambient temperature: 25°C ±5°C
Ambient humidity: 65±10% RH
Ambient illumination: 300~700 lux

6.1.3 Sampling Conditions

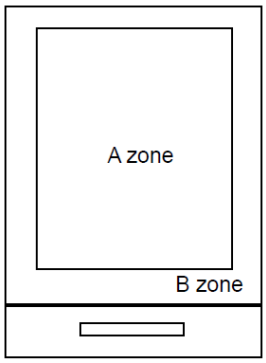
1. Lot size: quantity of shipment lot per model
2. Sampling method:

Sampling Plan		GB/T 2828-2003
		Normal inspection, Class II
AQL	Major Defect	0.65%
	Minor Defect	1.5%

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot Line defect	Light dot , Dim spot,Polarizer Bubble ; Polarizer accidented spot.	
6	Soldering appearance	Good soldering , Peeling off is not allowed.	

6.1.4 Definition of Area

A zone: active area
B zone: viewing area

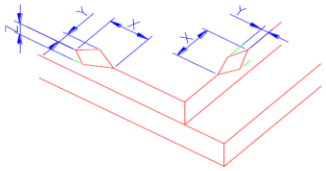
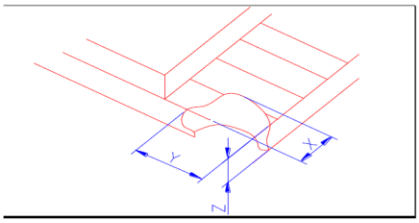
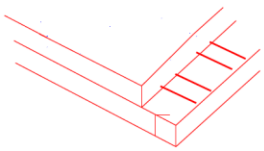


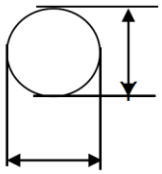
6.1.5 Basic Principle

A set of sample to indicate the limit of acceptable quality level shall be discussed should a dispute occur.

6.1.6 Inspection Criteria

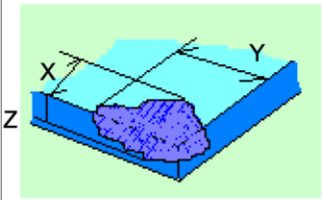
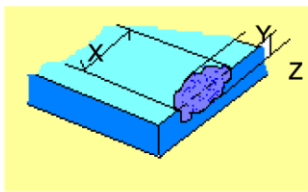
<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken

NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

<table>
<tr><th>Number</th><th>Items</th><th>Criteria (mm)</th></tr>
<tr><td>2.0</td><td>Spot defect
 
X
Φ=(X+Y)/2</td><td>① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain)
<table>
<tr><th rowspan="2">Zone
Size (mm)</th><th colspan="3">Accep able Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.10</td><td colspan="2">Ignore</td><td rowspan="4">Ignor</td></tr>
<tr><td>0.10<Φ≤0.20</td><td colspan="2">3(distance≧10mm)</td></tr>
<tr><td>0.20<Φ≤0.25</td><td colspan="2">2</td></tr>
<tr><td>Φ > 0.25</td><td colspan="2">0</td></tr>
</table>
②Dim spot (LCD/TP/Polarizer dim dot, light leakage、dark spot)
<table>
<tr><th rowspan="2">Zone
Size (mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.10<Φ≤0.20</td><td colspan="2">3(distance≧10mm)</td></tr>
<tr><td>0.20<Φ≤0.30</td><td colspan="2">2</td></tr>
<tr><td>Φ > 0.30</td><td colspan="2">0</td></tr>
</table>
③ Polarizer accidented spot
<table>
<tr><th rowspan="2">Zone
Size (mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.2</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.3<Φ≤0.5</td><td colspan="2">2(distance≧10mm)</td></tr>
<tr><td>Φ>0.5</td><td colspan="2">0</td></tr>
</table></td></tr>
<tr><td></td><td>Line defect (LCD/TP /Polarizer black/white line, scratch, stain)</td><td>
<table>
<tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.03</td><td>Ignoe</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.03<W≤0.05</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.05<W≤0.08</td><td>L≤2.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>3.0</td><td>Polarizer Bubble</td><td>
<table>
<tr><td rowspan="2">Zone
Size (mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.2</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.2<Φ≤0.4</td><td colspan="2">3(distance≧10 m)</td></tr>
<tr><td>0.4<Φ≤0.6</td><td colspan="2">2</td></tr>
<tr><td>0.6<Φ</td><td colspan="2">0</td></tr>
</table>
</td></tr>
<tr><td>4.0</td><td>SMT</td><td>According to IPC-A-610C class Ⅱ standard . Function defect and missing part are major defect ,the others are minor defect.</td></tr>
</table>

<table>
<tr><td rowspan="2"></td><td rowspan="2"></td><td>TP bubble/ accidented spot</td><td>
<table>
<tr><td rowspan="2">Size Φ(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.1<Φ≤0.25</td><td colspan="2"></td></tr>
<tr><td>0.25<Φ≤0.3</td><td colspan="2">2</td></tr>
<tr><td>0.3<Φ</td><td colspan="2">0</td></tr>
</table>
</td></tr>
<tr><td>Assembly deflection</td><td>beyond the edge of backlight ≤0.15mm</td></tr>
</table>

<table>
<tr>
<td>5.0</td>
<td>TP Related</td>
<td>Newton Ring</td>
<td>Newton Ring area>1/3 TP area NG
Newton Ring area≤1/3 TP area OK</td>
<td>  </td>
</tr>
<tr>
<td></td>
<td></td>
<td>TP corner broken
X : length
Y : width
Z : height</td>
<td><table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>X≤3.0mm</td><td>Y≤3.0mm</td><td>Z<LCD thickness</td></tr></table>*
Circuitry broken is not allowed.</td>
<td>  </td>
</tr>
<tr>
<td></td>
<td></td>
<td>TP edge broken
X : length
Y : width
Z : height</td>
<td><table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>X≤6.0mm</td><td>Y≤2.0mm</td><td>Z<LCD thickness</td></tr></table>* Circuitry broken is not allowed.</td>
<td>  </td>
</tr>
</table>

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

6.1.7 Classification of Defects

Visual defects (except no or wrong label) are treated as minor defects, while electrical defects are treated as major defects.
Two minor defects are equal to one major defect in lot sampling inspection.

6.1.8 Identification / marking criteria

Any unit with illegible / wrong / double or no marking / label shall be rejected.

6.2 Dealing with Customer Complaints

6.2.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.
After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

6.2.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

7.0 Reliability Specification

7.1 Reliability Tests

Test Item		Test Condition		Sample Size
Durability Test	High Temperature Operation	Ta= 70˚C	96h	3pcs
	Low Temperature Operation	Ta=-20˚C	96h	3pcs
	Temperature Cycle Operation	-20°C ←→ 70°C ON/OFF, 20 cycles. ON time over 10 seconds, OFF time over 10 seconds		3pcs
	High Temperature Storage	Tp= 80°C	96h	3pcs
	Low Temperature Storage	Tp= -30°C	96h	3pcs
	ESD Test	150pF, 330Ω, ±6KV (Contact)/±8KV (Air), 5 Points/panel, 10 times/point		3pcs
	Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: LTS for 30 minutes -> normal temperature for 5 minutes -> HTS for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours		3pcs
	Box Drop Test	1 Corner 3 Edges 6 faces, 66 cm (Medium Box)		1 box

Note: Ta=ambient temperature Tp= Panel temperature

Notes:
1. No dew condensation to be observed.
2. The function test shall be conducted after 4 hours storage at the normal temperature and humidity after removed from the test chamber.
3. No cosmetic or functional defects should be allowed.
4. Total current consumption should be less than twice the initial value.

8.0 Handling Precautions

Safety

If the LCD panel breaks, be careful not to get the liquid crystal fluid in your mouth or in your eyes.
If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design

Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.
When assembling with a zebra connector, clean the surface of the pads with alcohol and keep the surrounding air very clean.
Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during LCD cleaning

Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotriflorothane.
Do not wipe the display surface with dry or hard materials that will damage the polariser surface.
Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge

As the display uses C-MOS LSI drivers, connect any unused input terminal to VDD or VSS. Do not input any signals before power is turned on. Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging

Displays use LCD elements, and must be treated as such. Avoid strong shock and drop from a height. To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation

It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life. Direct current causes an electrochemical reaction with remarkable deterioration of the display quality. Give careful consideration to prevent direct current during ON/OFF timing and during operation. Response time is extremely delayed at temperatures lower than the operating temperature range while, at high temperatures, displays become dark. However, this phenomenon is reversible and does not mean a malfunction or a display that has been permanently damaged. If the display area is pushed on hard during operation, some graphics will be abnormally displayed but returns to a normal condition after turning off the display once. Even a small amount of condensation on the contact pads (terminals) can cause an electro-chemical reaction which causes missing rows and columns. Give careful attention to avoid condensation.

Storage

Store the display in a dark place where the temperature is 25°C ± 10°C and the humidity below 50%RH. Store the display in a clean environment, free from dust, organic solvents and corrosive gases. Do not crash, shake or jolt the display (including accessories).