



BUK7Y3R5-40H

N-channel 40 V, 3.5 mΩ standard level MOSFET in LFPK56

14 September 2017

Product data sheet

1. General description

Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a robust LFPK56 package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Fully automotive qualified to AEC-Q101:
 - 175 °C rating suitable for thermally demanding environments
- Trench 9 Superjunction technology:
 - Reduced cell pitch enables enhanced power density and efficiency with lower R_{DSon} in same footprint
 - Improved SOA and avalanche capability compared to standard TrenchMOS
 - Tight $V_{GS(th)}$ limits enable easy paralleling of MOSFETs
- LFPK Gull Wing leads:
 - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
 - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
 - Easy solder wetting for good mechanical solder joint
- LFPK copper clip technology:
 - Improved reliability, with reduced R_{th} and R_{DSon}
 - Increases maximum current capability and improved current spreading

3. Applications

- 12 V automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

4. Quick reference data

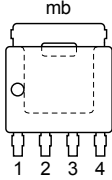
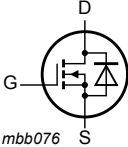
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	120	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	115	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11		2	2.9	3.5	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 13 ; Fig. 14		-	6	15	nC
Source-drain diode							
Q_r	recovered charge	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A/}\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; Fig. 17		-	16	-	nC
S	softness factor	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A/}\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $T_j = 25\text{ °C}$		-	0.8	-	

[1] 120A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56; Power-SO8 (SOT669)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7Y3R5-40H	LPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals; 4.9 mm x 4.45 mm x 1 mm body	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7Y3R5-40H	73H540

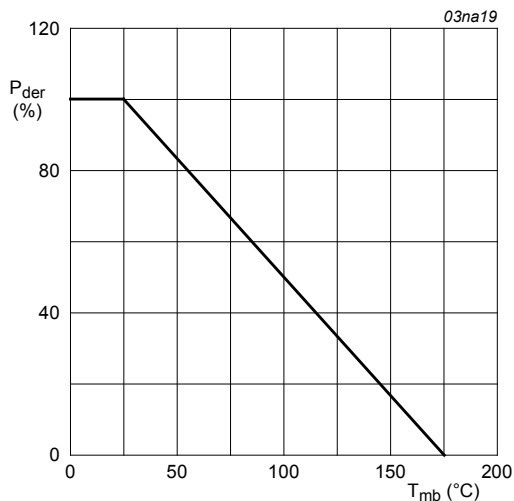
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

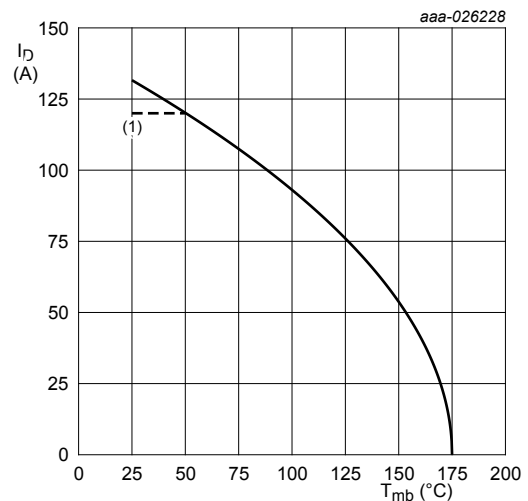
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	40	V
V_{GS}	gate-source voltage	DC; $T_j \leq 175\text{ °C}$		-10	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	115	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	120	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	[1]	-	93	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3		-	526	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	[1]	-	120	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	526	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 120\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; Fig. 4	[2] [3]	-	45	mJ

- [1] 120A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
 [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
 [3] Refer to application note AN10273 for further information.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq 10\text{ V}$

(1) 120A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature

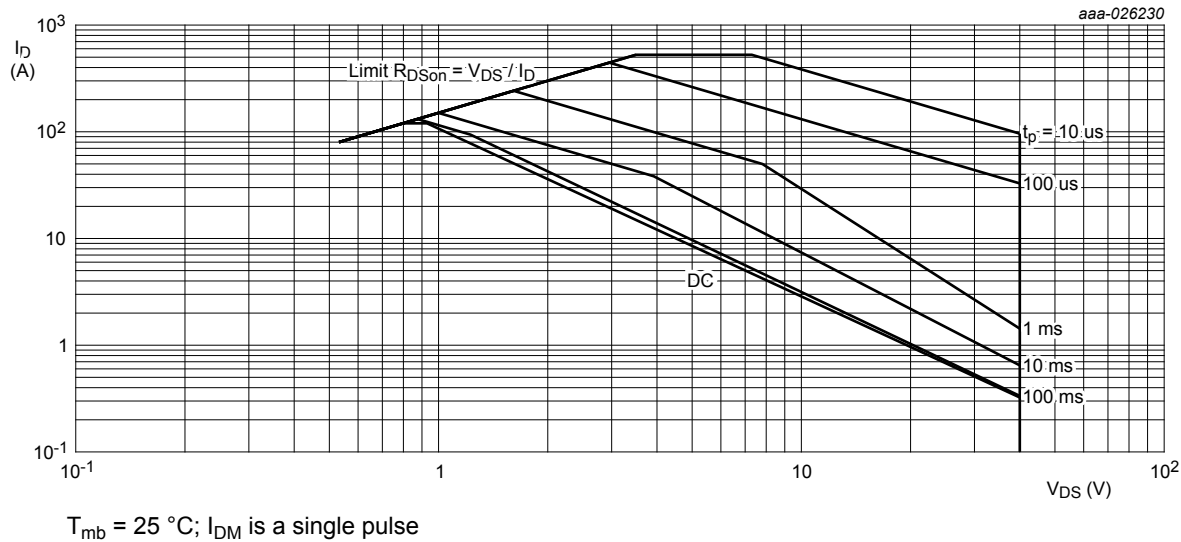


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

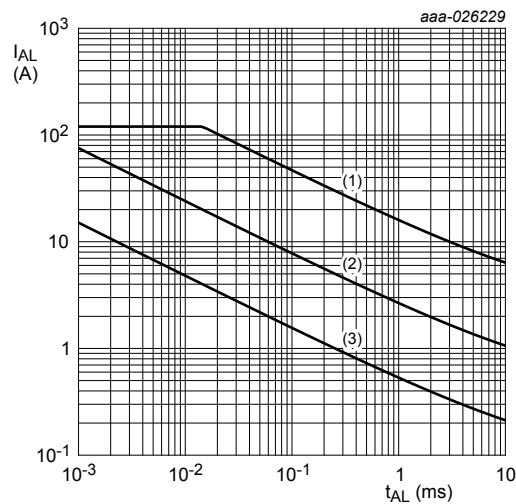
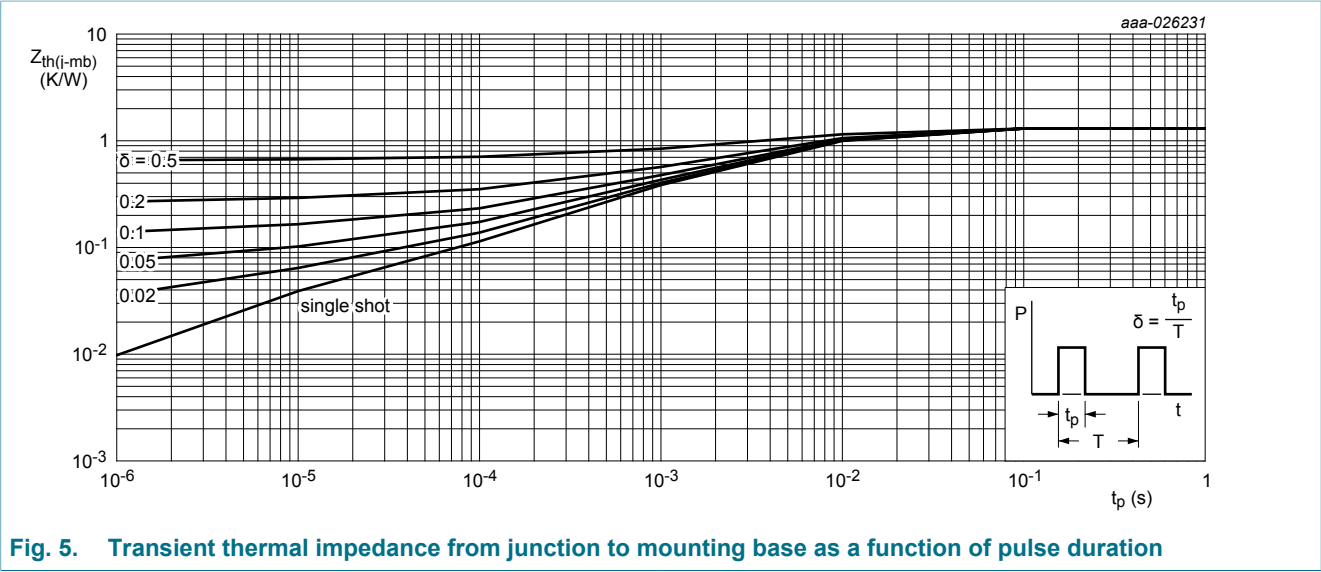


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	1.18	1.3	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		40	42.7	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -40 °C		-	40.1	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C		36	39.7	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 25 °C; Fig. 9 ; Fig. 10		2.4	3	4	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = -55 °C; Fig. 9		-	-	4.5	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 175 °C; Fig. 9		1	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _j = 25 °C		-	0.03	1	μA
		V _{DS} = 16 V; V _{GS} = 0 V; T _j = 125 °C		-	1	10	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _j = 175 °C		-	37	500	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 11		2	2.9	3.5	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 105 °C; Fig. 12		2.7	4.1	5.2	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 125 °C; Fig. 12		2.9	4.5	5.6	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 12		3.4	5.4	6.7	mΩ
R _G	gate resistance	f = 1 MHz; T _j = 25 °C		0.32	0.8	2	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 10 V; Fig. 13 ; Fig. 14		-	31	53	nC
Q _{GS}	gate-source charge			-	10	15	nC
Q _{GD}	gate-drain charge			-	6	15	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 15		-	2294	3441	pF
C _{oss}	output capacitance			-	682	954	pF
C _{rss}	reverse transfer capacitance			-	112	247	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω		-	10	-	ns
t _r	rise time			-	8	-	ns
t _{d(off)}	turn-off delay time			-	19	-	ns
t _f	fall time			-	9	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 16		-	0.8	1.2	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; Fig. 17	-	25	-	ns
Q _r	recovered charge		-	16	-	nC
S	softness factor	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _J = 25 °C	-	0.8	-	
		I _S = 25 A; dI _S /dt = -500 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _J = 25 °C; Fig. 17	-	0.6	-	

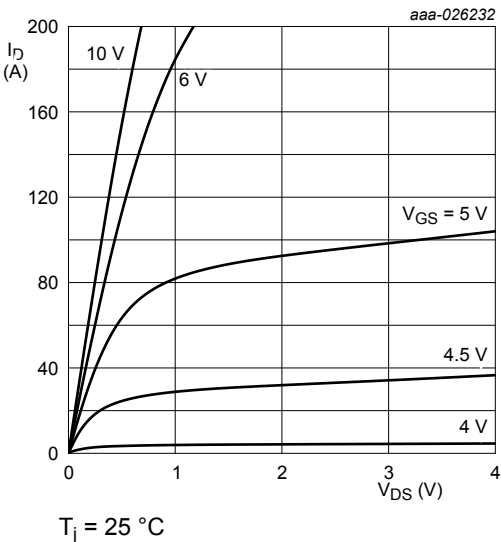


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

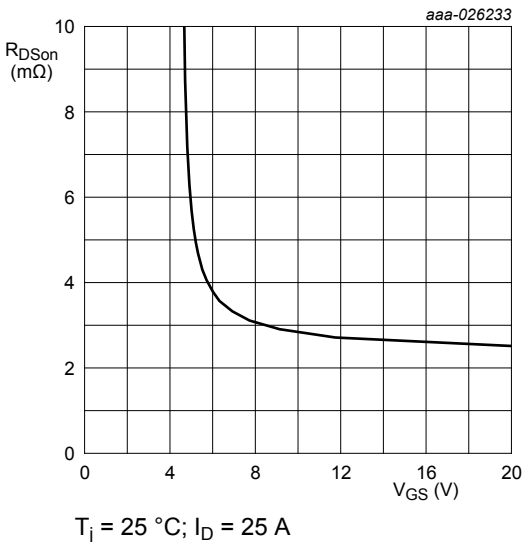


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

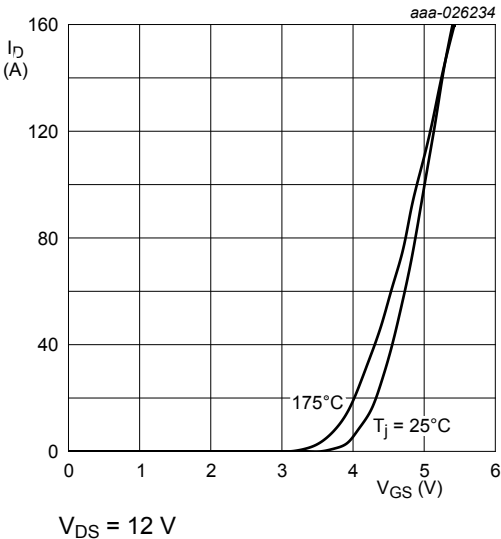


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

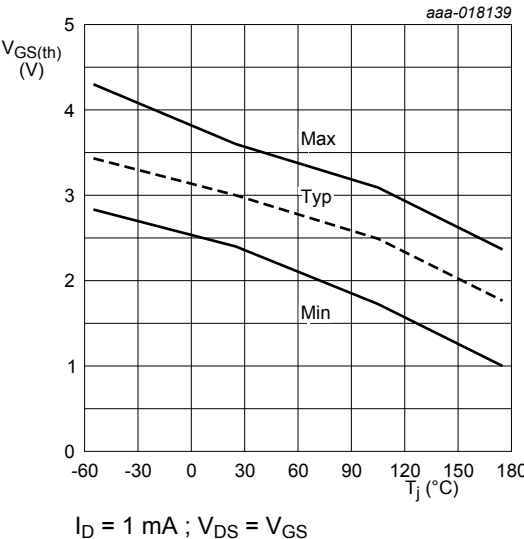


Fig. 9. Gate-source threshold voltage as a function of junction temperature

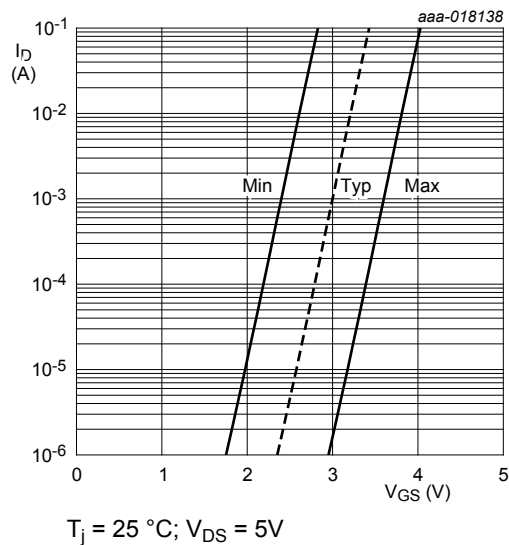


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

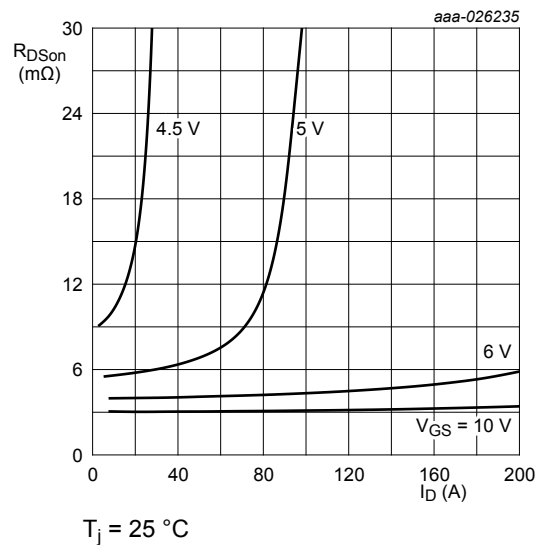


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

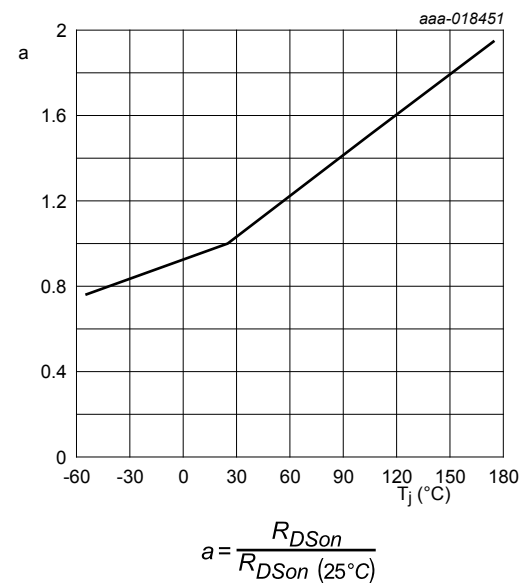


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

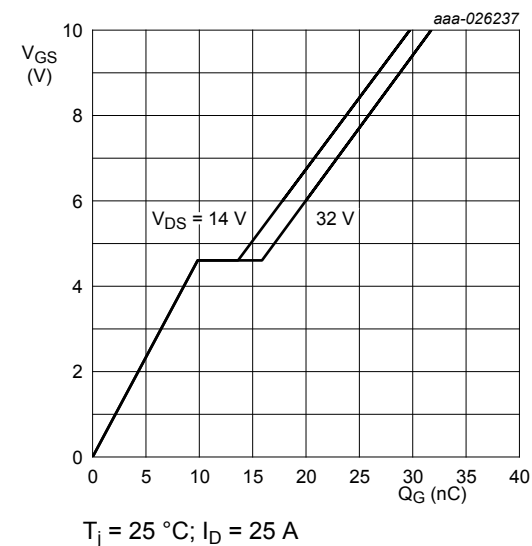


Fig. 13. Gate-source voltage as a function of gate charge; typical values

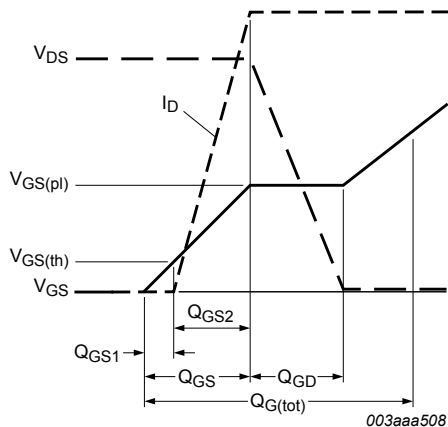
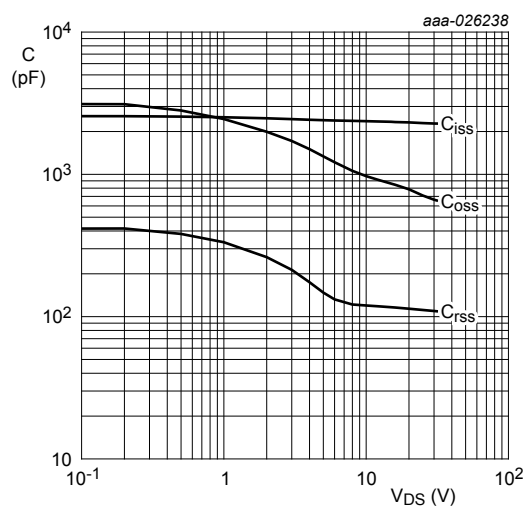
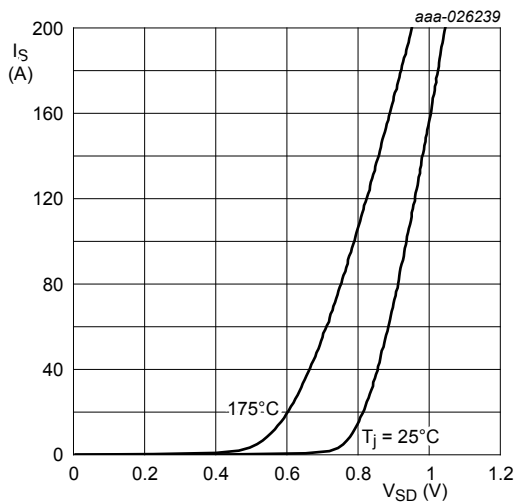


Fig. 14. Gate charge waveform definitions



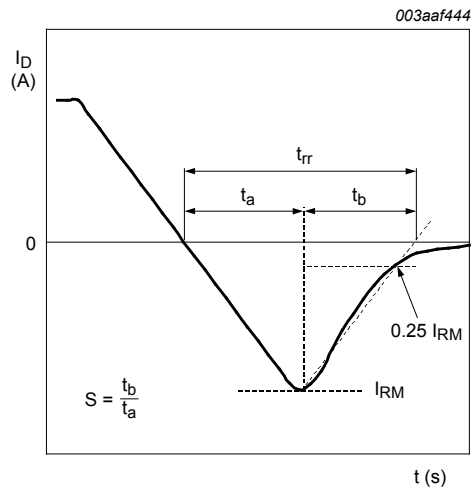
$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0 \text{ V}$

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values



$t_{rr} = t_a + t_b$

Fig. 17. Reverse recovery waveform definitions

11. Soldering

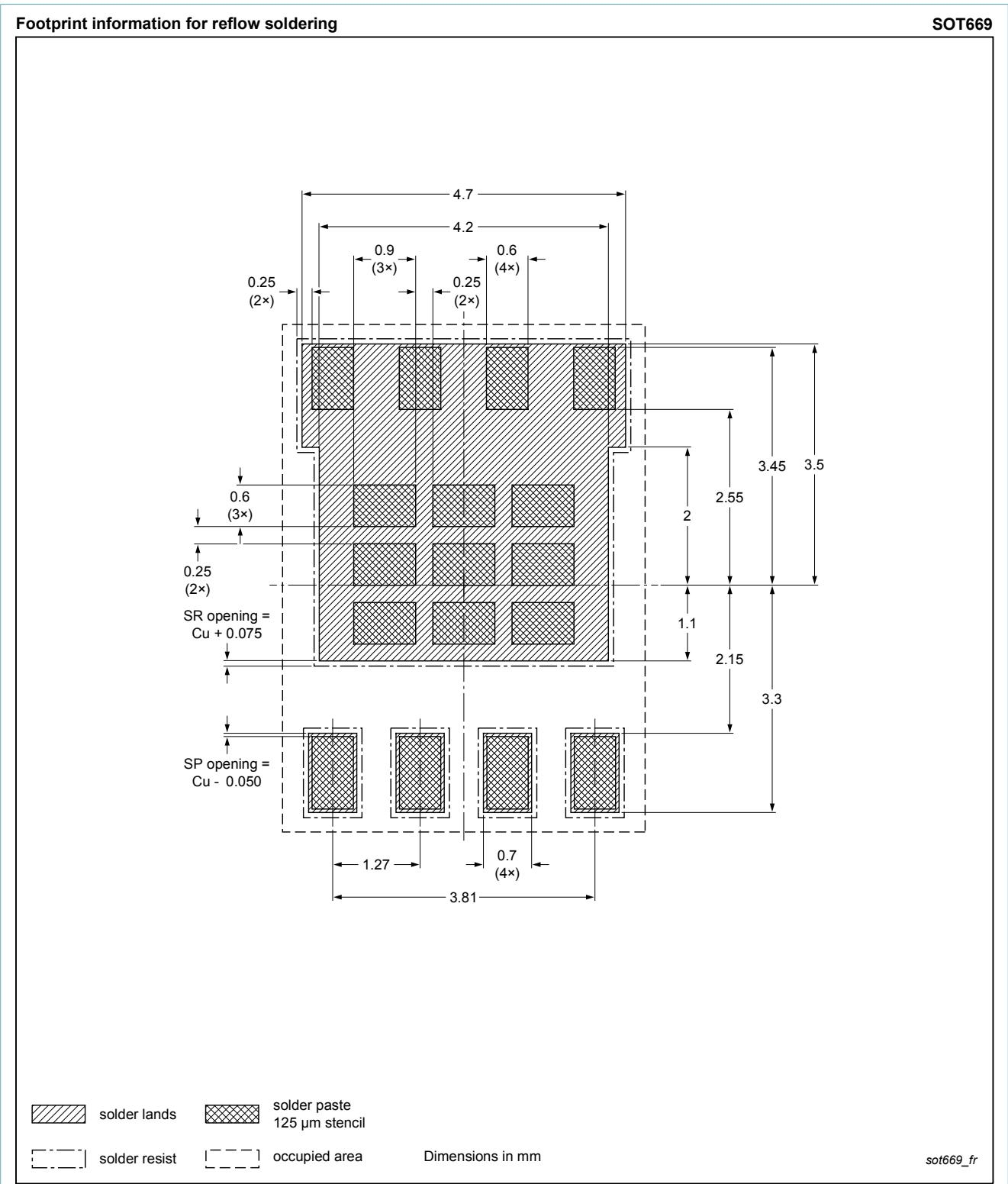


Fig. 18. Reflow soldering footprint for LPAK56; Power-SO8 (SOT669)

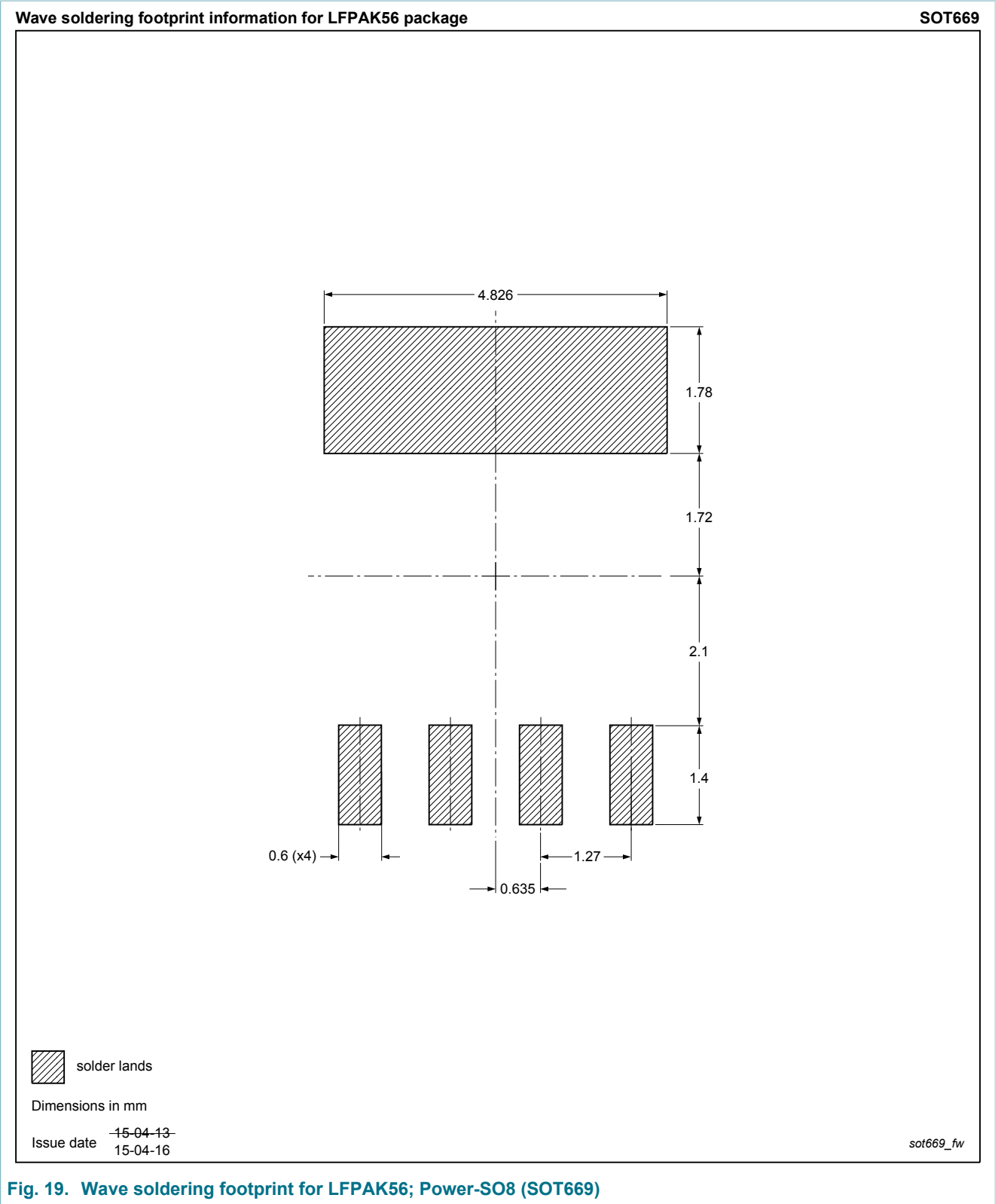


Fig. 19. Wave soldering footprint for LPAK56; Power-SO8 (SOT669)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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13. Contents

1. General description..... 1

2. Features and benefits..... 1

3. Applications..... 1

4. Quick reference data..... 2

5. Pinning information..... 3

6. Ordering information..... 3

7. Marking..... 3

8. Limiting values..... 4

9. Thermal characteristics..... 5

10. Characteristics..... 7

11. Soldering..... 11

12. Legal information..... 13

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