



BUK7Y2R0-40H

N-channel 40 V, 2.0 mΩ standard level MOSFET in LFPK56

14 September 2017

Product data sheet

1. General description

Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a robust LFPK56 package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Fully automotive qualified to AEC-Q101:
 - 175 °C rating suitable for thermally demanding environments
- Trench 9 Superjunction technology:
 - Reduced cell pitch enables enhanced power density and efficiency with lower $R_{DS(on)}$ in same footprint
 - Improved SOA and avalanche capability compared to standard TrenchMOS
 - Tight $V_{GS(th)}$ limits enable easy paralleling of MOSFETs
- LFPK Gull Wing leads:
 - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
 - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
 - Easy solder wetting for good mechanical solder joint
- LFPK copper clip technology:
 - Improved reliability, with reduced R_{th} and $R_{DS(on)}$
 - Increases maximum current capability and improved current spreading

3. Applications

- 12 V automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

4. Quick reference data

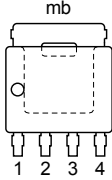
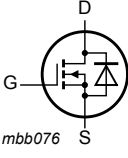
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$	-	-	120	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	217	W

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_J = 25\text{ }^{\circ}\text{C}$; Fig. 10		1.07	1.53	2	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 12 ; Fig. 13		-	10.8	27.3	nC
Source-drain diode							
Q_r	recovered charge	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; Fig. 16		-	21	-	nC
S	softness factor	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $T_J = 25\text{ }^{\circ}\text{C}$; Fig. 16		-	0.8	-	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56; Power-SO8 (SOT669)	 <i>mbb076</i>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7Y2R0-40H	LPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals; 4.9 mm x 4.45 mm x 1 mm body	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7Y2R0-40H	72H040

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	40	V
V_{GS}	gate-source voltage	DC; $T_j \leq 175\text{ °C}$		-10	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	217	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$		-	120	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 2		-	600	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	[1]	-	120	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	600	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 120\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; Fig. 3	[2] [3]	-	108	mJ

- [1] 120A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
 [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
 [3] Refer to application note AN10273 for further information.

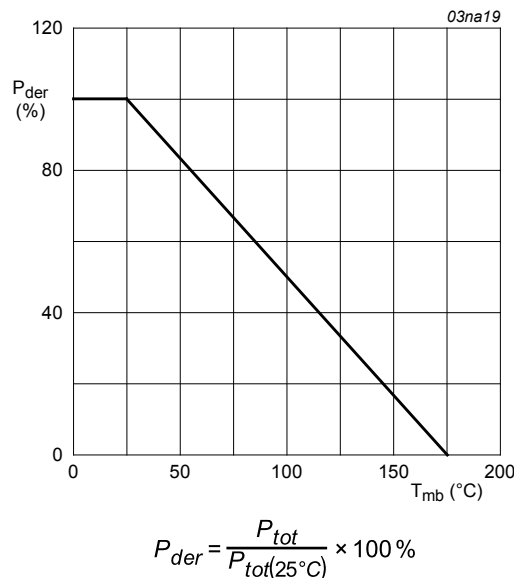


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

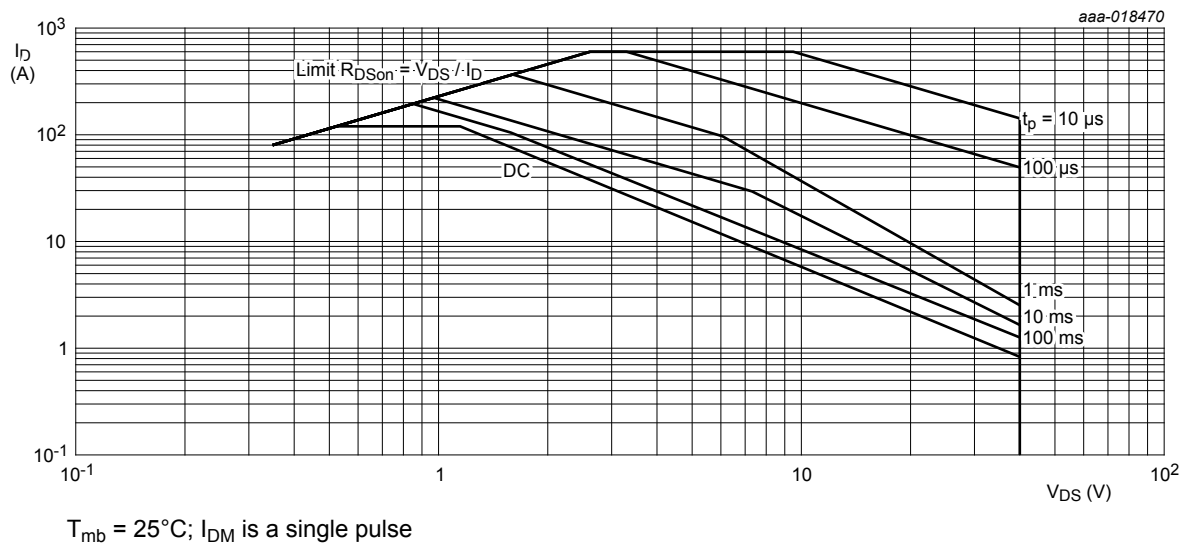
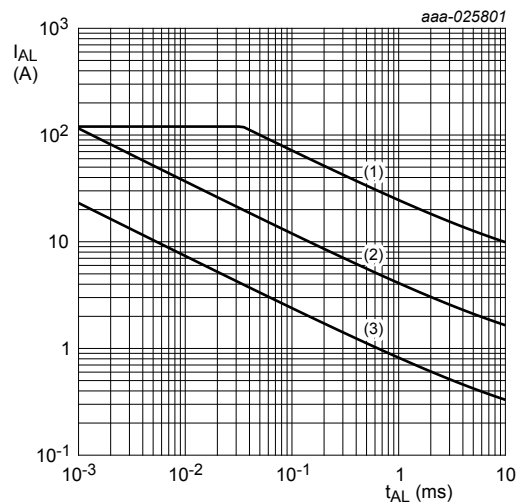


Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



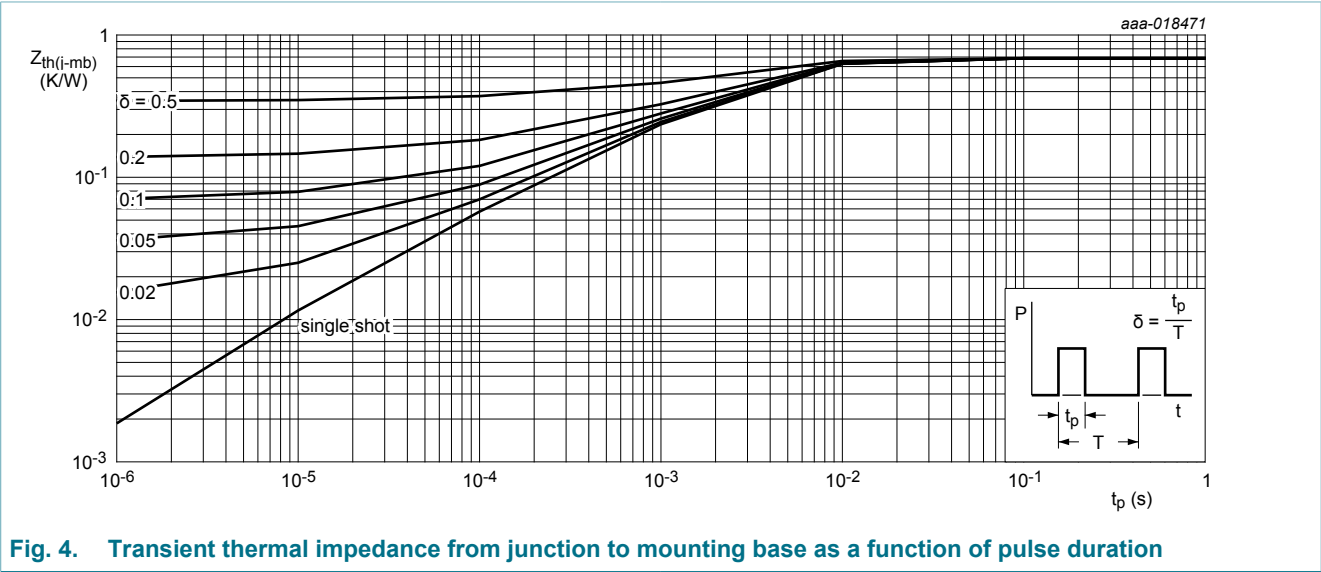
(1) $T_{j (init)} = 25^\circ C$; (2) $T_{j (init)} = 150^\circ C$; (3) Repetitive Avalanche

Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	0.5	0.69	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		40	42.7	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -40 °C		-	40.3	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C		36	39.7	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 25 °C; Fig. 8 ; Fig. 9		2.4	3	3.6	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = -55 °C; Fig. 8		-	-	4.3	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 175 °C; Fig. 8		1	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _j = 25 °C		-	0.2	1	μA
		V _{DS} = 16 V; V _{GS} = 0 V; T _j = 125 °C		-	2	10	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _j = 175 °C		-	180	500	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 10		1.07	1.53	2	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 105 °C; Fig. 11		1.52	2.33	3.18	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 125 °C; Fig. 11		1.68	2.59	3.5	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 11		2.11	3.24	4.36	mΩ
R _G	gate resistance	f = 1 MHz; T _j = 25 °C		0.36	0.9	2.3	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 10 V; Fig. 12 ; Fig. 13		-	52.6	90.5	nC
Q _{GS}	gate-source charge			-	14.8	22.5	nC
Q _{GD}	gate-drain charge			-	10.8	27.3	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 14		-	3633	5450	pF
C _{oss}	output capacitance			-	984	1377	pF
C _{rss}	reverse transfer capacitance			-	188	415	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.5 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω		-	13.5	-	ns
t _r	rise time			-	12	-	ns
t _{d(off)}	turn-off delay time			-	31.4	-	ns
t _f	fall time			-	15.1	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 15		-	0.8	1.2	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; Fig. 16	-	29	-	ns
Q_r	recovered charge		-	21	-	nC
S	softness factor	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 16	-	0.8	-	
		$I_S = 25\text{ A}$; $dI_S/dt = -500\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 16	-	0.7	-	

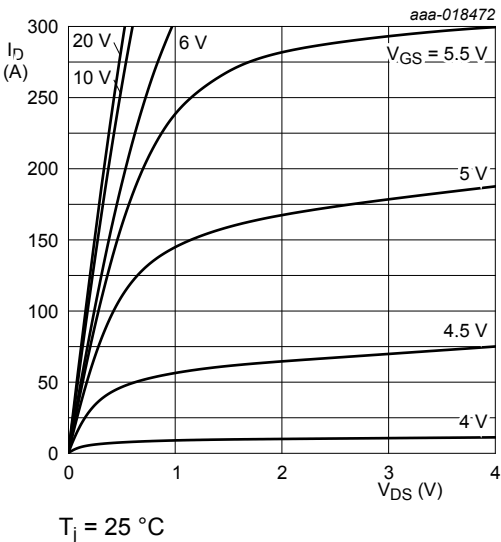


Fig. 5. Output characteristics; drain current as a function of drain-source voltage; typical values

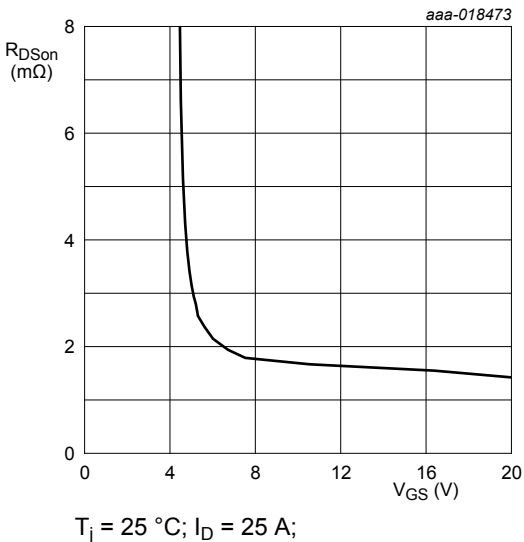


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

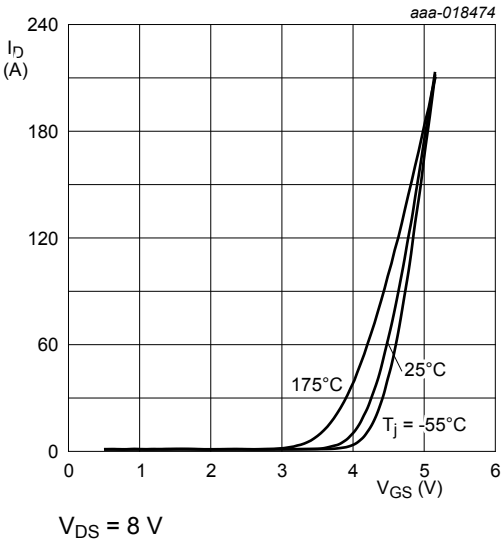


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

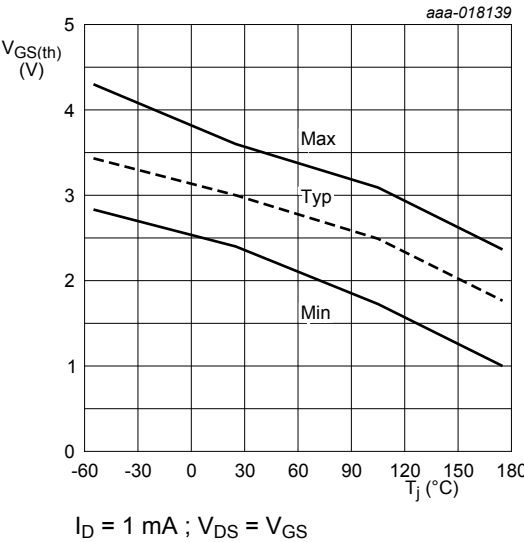
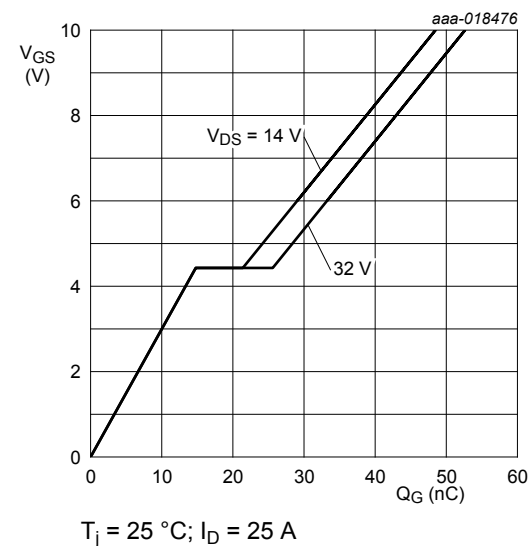
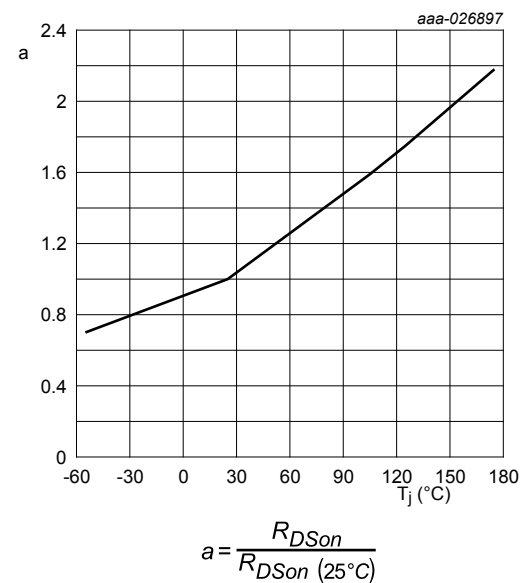
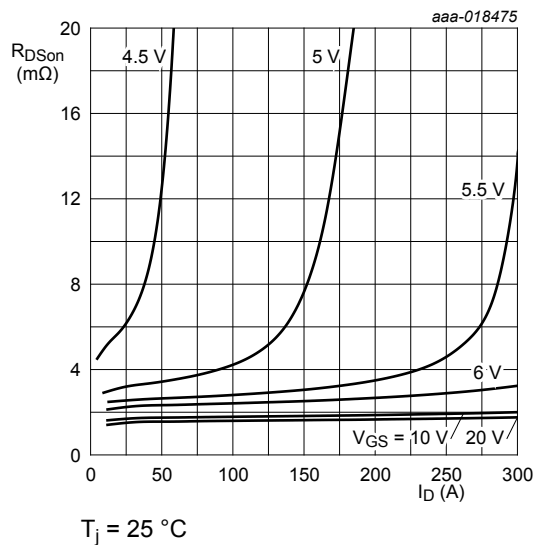
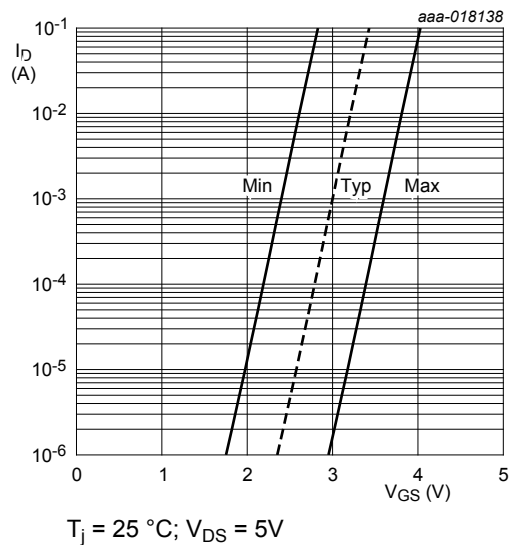


Fig. 8. Gate-source threshold voltage as a function of junction temperature



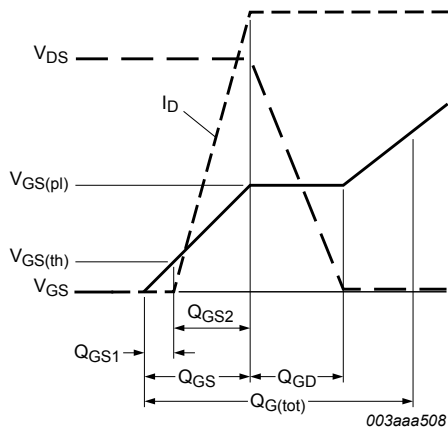
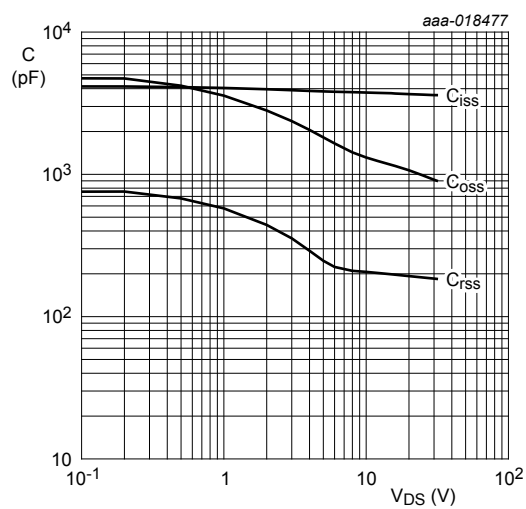
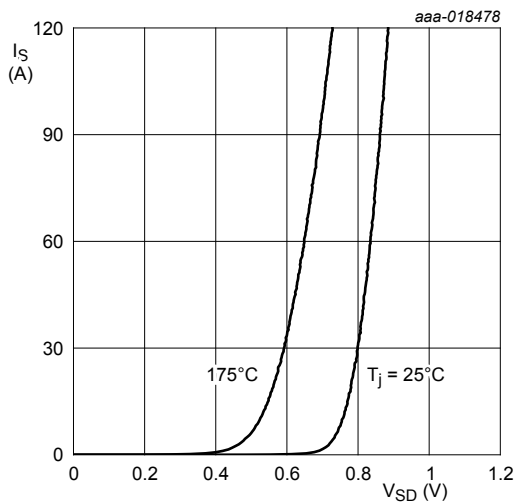


Fig. 13. Gate charge waveform definitions



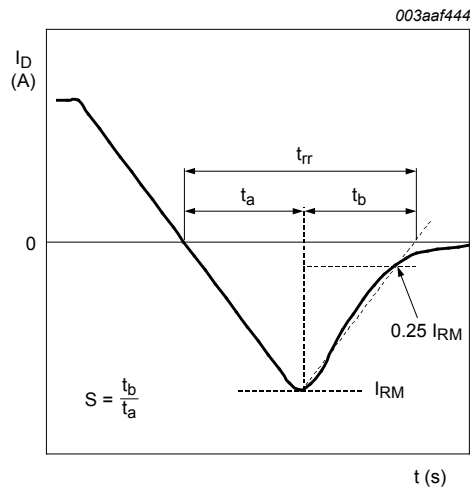
$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0 \text{ V}$

Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values



$t_{rr} = t_a + t_b$

Fig. 16. Reverse recovery waveform definitions

11. Package outline

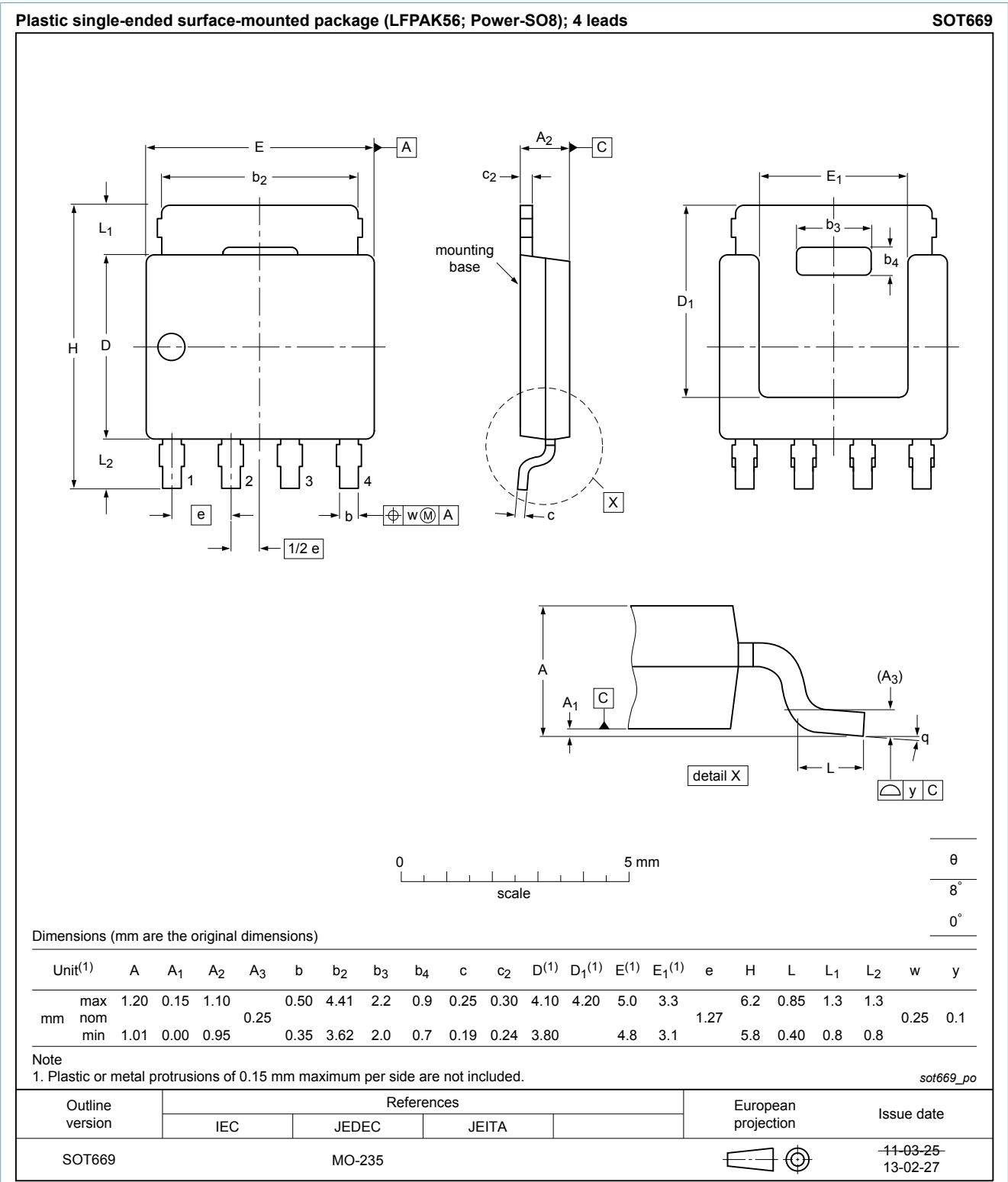


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

12. Legal information

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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