Half-Bridge IPM for Low Voltage Applications

μIPM™

80A, 40V

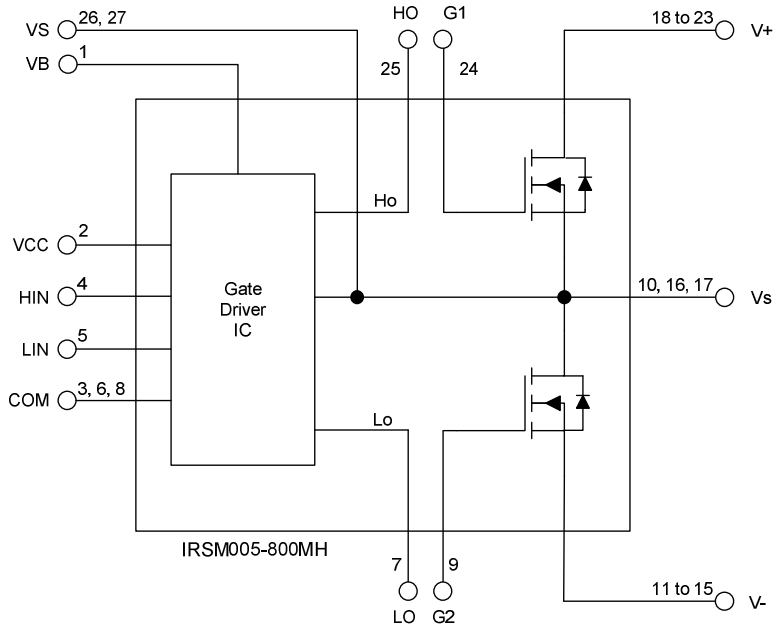
Description

The IRSM005-800MH is a general purpose half-bridge with integrated gate driver in an attractive 7x8mm PQFN package. It is a general purpose building block suitable for a variety of low voltage applications where power density is of critical importance. Typical examples would be advanced motor drives, dc-to-ac and dc-to-dc converters.

Features

- Package with low thermal resistance and minimal parasitics
- Low on-resistance HEXFETs: 2.7 mΩ typ.
- Undervoltage lockout on logic supply
- Independent gate drive in phase with logic input
- Gate drive supply range from 10V to 20V
- Propagation delay matched to defined spec
- 3.3V, 5V and 15V logic input compatible
- RoHS compliant

Internal Electrical Schematic



Ordering Information

Orderable Part Number	Package Type	Form	Quantity
IRSM005800MH	PQFN 7x8mm	Tray	1300
IRSM005800MHTR	PQFN 7x8mm	Tape and Reel	2000

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the module may occur. These are not tested at manufacturing. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise stated in the table. The thermal resistance rating is measured under board mounted and still air conditions.

Symbol	Description	Min	Max	Unit
V_{DS}	MOSFET Drain-to-Source Voltage	---	40	V
I_o	Maximum DC current per MOSFET @ T_C=25°C (Note1)	---	80	A
P_d	Maximum Power dissipation per MOSFET @ T_C =100°C	---	13	W
T_J (MOSFET & IC)	Maximum Operating Junction Temperature	---	150	°C
T_S	Storage Temperature Range	-40	150	°C
V_{GS}	Gate to Source voltage	+/- 20		V
V_B	High side floating absolute supply voltage	-0.3	225	
V_S	High side floating supply offset voltage	V_B - 20	V_B + 0.3	
V_{CC}	Low Side fixed supply voltage	-0.3	25	
V_{LO}	Low side output voltage	-0.3	V_{CC} +0.3V	
V_{HO}	High side output voltage	-0.3	V_{CC} +0.3V	
V_{IN}	Logic input voltage LIN, HIN	-0.3	V_{CC} +0.3V	

Note1: Calculated based on maximum junction temperature. Bond wires current limit is 49A

Inverter Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS})=15V, TJ=25ºC, unless otherwise specified.

Symbol	Description	Min	Typ	Max	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	---	---	V	H_{IN}=L_{IN}=0V, I_D=250µA
$V_{GS(TH)}$	Gate Threshold Voltage	2	---	4	V	I_D=100µA
$R_{DS(ON)}$	Drain-to-Source Voltage	---	2.7	5.0	mΩ	I_D=10A, T_J=25°C
		---	4.2			I_D=10A, T_J=150°C
I_{DSS}	Zero Gate Voltage Drain Current	---		20	µA	H_{IN}=L_{IN}=0V, V^+=40V
		---	---	150		H_{IN}=L_{IN}=0V, V^+=40V, T_J=125°C
I_{GSS}	Gate to Source Forward Leakage	---	---	100	nA	V_{GS}=20V
	Gate to Source Reverse Leakage	---	---	-100		V_{GS}=-20V
R_G	Internal Gate Resistance	---	1.5	---	Ω	
V_{SD}	Mosfet Diode Forward Voltage Drop	---	0.8	0.9	V	I_F=10A
		---	0.55			I_F=10A, T_J=150°C
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE, limited by T_{Jmax}				V^+= 40V, V_{CC}=+15V to 0V
I_o @ T_A=60°C	RMS Phase Current, sinusoidal modulation, 5kHz	---	13.5	---	A_{RMS}	V+=32V, TJ=125°C, MI=1, PF=0.8, typical board mount. See Figure 2.
I_o @ T_A=60°C	RMS Phase Current, sinusoidal modulation, 20kHz	---	6	---	A_{RMS}	
EAS	Single Pulse Avalanche Energy	9.2	---	---	mJ	

Inverter Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS})=15V, TJ=25ºC, unless otherwise specified.

gfs	Forward Transconductance	159	---	---	S	I_D =50A V_{DS} = 10V
Q_G	Total Gate Charge	---	65	98	nC	I_D =50A V_{DS} = 20V V_{GS}=10V
Q_{GS}	Gate to Source Charge	---	16	---		
Q_{GD}	Gate to Drain Charge	---	23	---		
Q_{SYNC}	Total Gate Charge Sync. (Q_G - Q_{GD})	---	42	---		I_D =50A,V_{DS} = 0V,V_{GS} = 10V
T_{DON}	Mosfet Turn On Delay Time	---	11	---	ns	I_D =30A V_{DD} = 20V V_{GS}=10V R_G=2.7Ω
T_R	Mosfet Rise Time	---	37	---		
T_{DOFF}	Mosfet Turn Off Delay Time	---	33	---		
T_F	Mosfet Fall Time	---	26	---		
C_{ISS}	Input Capacitance	---	3174	---	pF	F= 1.0MHz V_{DS} = 25V V_{GS}=0V
C_{OSS}	Output Capacitance	---	479	---		
C_{RSS}	Reverse Transfer Capacitance	---	332	---		
T_{RR}	Reverse Recovery TIme	---	16	---	ns	I_F =50A V_R =34V dI/dt= 100A/us
Q_{RR}	Reverse Recovery Charge	---	5	---	nC	
I_{RRM}	Reverse Recovery Current	---	0.5	---	A	

Recommended Operating Conditions Driver Function

For proper operation the device should be used within the recommended conditions. All voltages are absolute referenced to COM. The VS offset is tested with all supplies biased at 15V differential.

Symbol	Definition	Min	Typ	Max	Units
V_B	High side floating supply voltage	V_S+10	V_S+15	V_S+20	V
V_S	High side floating supply offset voltage	Note 1	---	40	V
V_{CC}	Low side and logic fixed supply voltage	10	15	20	V
V_{IN}	Logic input voltage LIN, HIN	COM	---	V_{CC}	V
HIN	High side PWM pulse width	1	---	---	µs
Deadtime	Suggested dead time between HIN and LIN	0.3	0.5	---	µs

Static Electrical Characteristics Driver Function

V_{BIAS} (V_{CC}, V_{BS})=15V, T_J=25ºC, unless otherwise specified. The V_{IN}, and I_{IN} parameters are referenced to COM

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IH}	Positive going input threshold for LIN, HIN	2.5	---	---	V	V_{CC}=10 to 20V
V_{IL}	Negative going input threshold for LIN, HIN	---	---	0.8		
V_{OH}	High Level Output Voltage	---	0.05	0.2		I_O=2mA
V_{OL}	Low Level Output Voltage	---	0.02	0.1		
V_{CCUV+} V_{BSUV+}	V_{CC}/V_{BS} supply undervoltage, Positive going threshold	8.0	8.9	9.8		
V_{CCUV-} V_{BSUV-}	V_{CC}/V_{BS} supply undervoltage, Negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUH}	V_{CC}/V_{BS} supply undervoltage lock-out hysteresis	---	0.8	---		
I_{LK}	Offset Supply Leakage Current	---	---	50	µA	V_B=V_S=200V
I_{QBS}	Quiescent V_{BS} supply current	---	45	75		V_{IN} =0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	---	250	500		
I_{IN+}	Input bias current V_{IN}=5V for LIN, HIN	---	4	10		V_{IN} = 5V
I_{IN-}	Input bias current V_{IN}=0V for LIN, HIN	---	0.5	1		V_{IN} =0V
I_{O+}	IC high output short circuit current	200	290	---	mA	V_O= 0V, V_{IN} = 5V, PW <10us
I_{O-}	IC low output short circuit current	420	600	---		

Dynamic Electrical Characteristics Driver Function

V_{BIAS} (V_{CC}, V_{BS})=15V, TJ=25ºC unless otherwise specified, C_L = 1000 pF, Driver only timing.

Symbol	Description	Min	Typ	Max	Units	Conditions
T_R	IC Turn on Rise Time	---	50	150	ns	
T_F	IC Turn off Fall Time	---	35	90		
T_{ON}	IC Input to Output propagation turn-on delay time	---	160	220		
T_{OFF}	IC Input to Output propagation turn-off delay time	---	150	220		
MT	IC Delay matching, HS and LS turn-on/off	---	---	50		

Thermal and Mechanical Characteristics

Symbol	Description	Min	Typ	Max	Units	Conditions
$R_{th(J-B)}$	Thermal resistance, junction to mounting pad, each MOSFET	---	3.8	---	°C/W	Standard reflow-solder process
$R_{th(J-A)}$	Thermal resistance, junction to ambient, each MOSFET	---	40	---	°C/W	Mounted on 50mm^2 of four-layer FR4 with 28 vias

Input-Output Logic Level Table

HIN	LIN	U,V,W
HI	HI	Shoot-through
LO	LO	**
HI	LO	V+
LO	HI	0

* V+ if motor current is flowing into VS, 0 if current is flowing out of VS into the motor winding

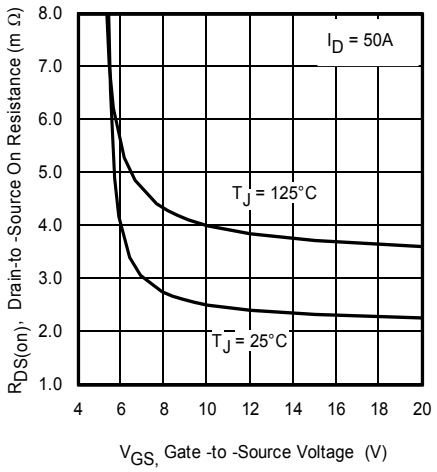


Fig. 1 Typical On Resistance vs Gate Voltage

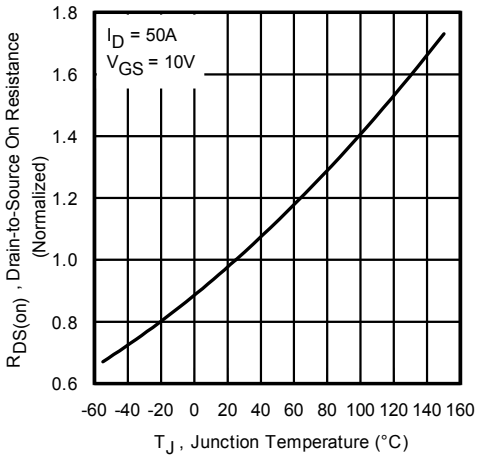


Fig.2 Normalized On Resistance vs Temperature

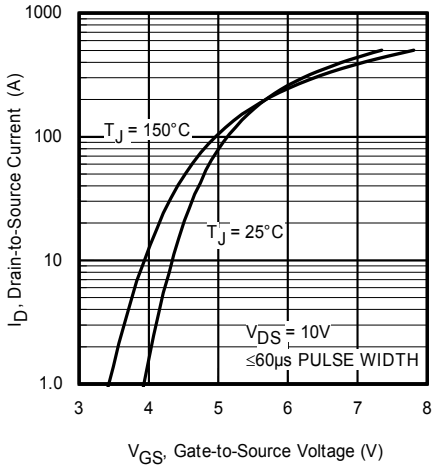


Fig. 3 Typical Transfer Characteristic

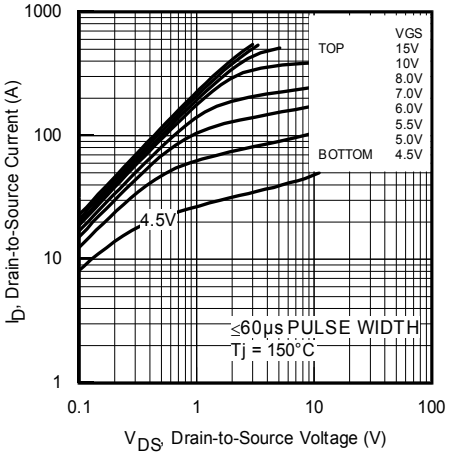


Fig.4 Typical Output Characteristic @ 150C

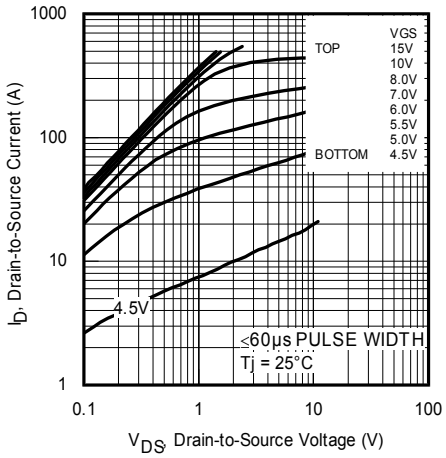


Fig. 5 Typical Output Characteristic @ 25C

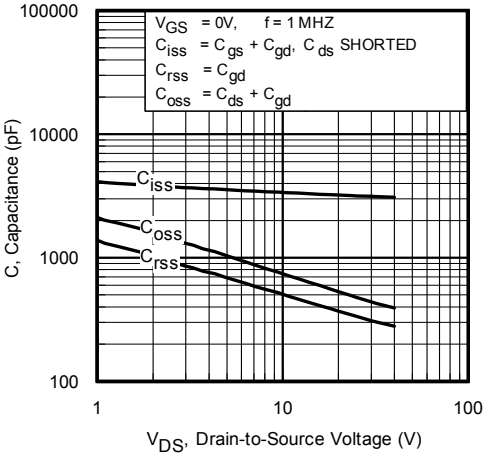


Fig. 6 Typical Capacitance vs Drain to Source Voltage

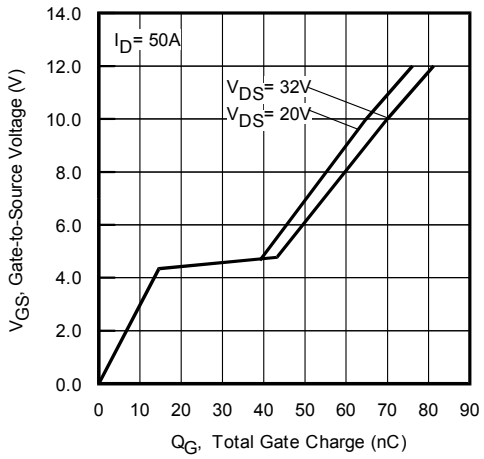


Fig. 7 Typical Gate Charge vs Gate Voltage

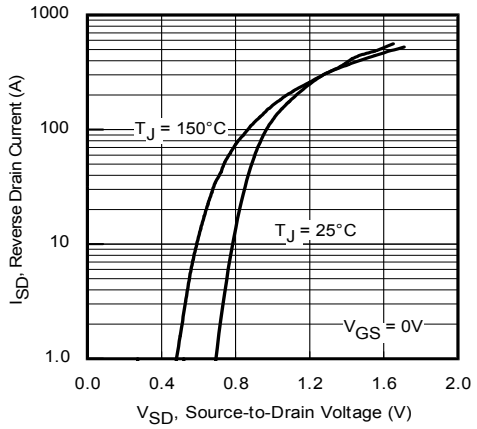


Fig.8 Typical Diode Forward Voltage Drop

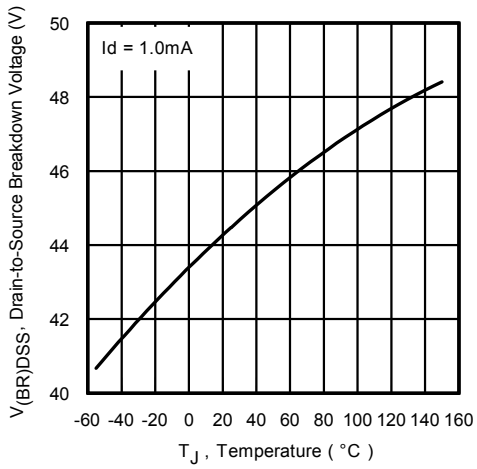


Fig. 9 Typical Breakdown Voltage vs Temperature

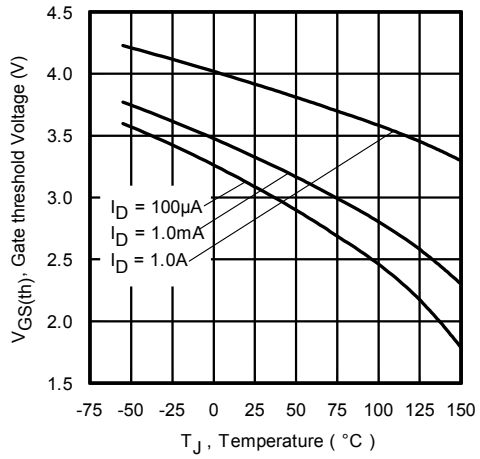


Fig.10 Threshold Voltage vs Temperature

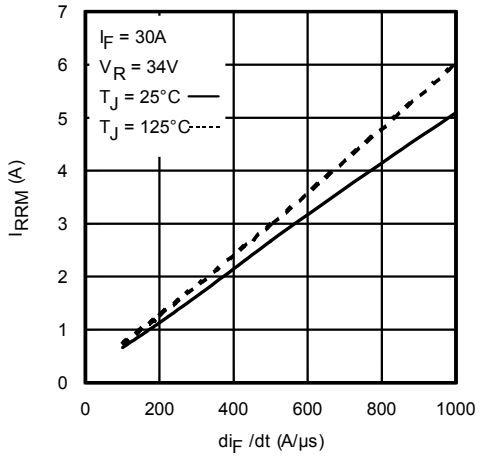


Fig. 11 Typical Recovery Current vs dI/dt

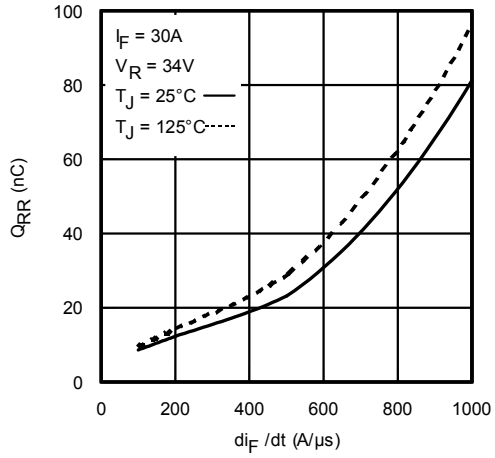
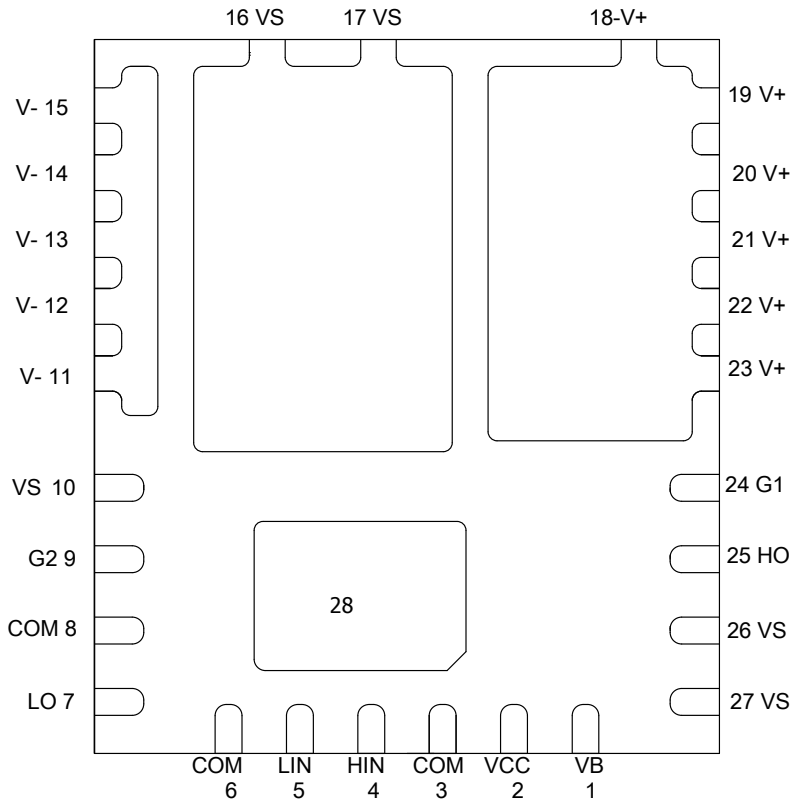


Fig. 12 Typical Recovery Charge vs Temperature

Module Pin-Out Description

Pin	Name	Description
3, 6, 8	COM	Negative of Gate Drive Supply Voltage
2	V_{CC}	15V Gate Drive Supply
4	HIN	Logic Input for High Side (Active High)
5	LIN	Logic Input for Low Side (Active High)
7	LO	Low Side FET Gate
9	G2	Low Side Gate Drive Output
10, 16, 17	V_S	Phase Output
11 – 15	V-	Low Side Source Connection
18 – 23	V+	DC Bus
24	G1	High Side Gate Drive Output
25	HO	High Side FET Gate
26 – 27	V_S	Negative of Bootstrap Supply
1	V_B	Positive of Bootstrap Supply



BOTTOM OF PACKAGE VIEW

Exposed pad (Pin 28) has to be connected to COM for better electrical performance

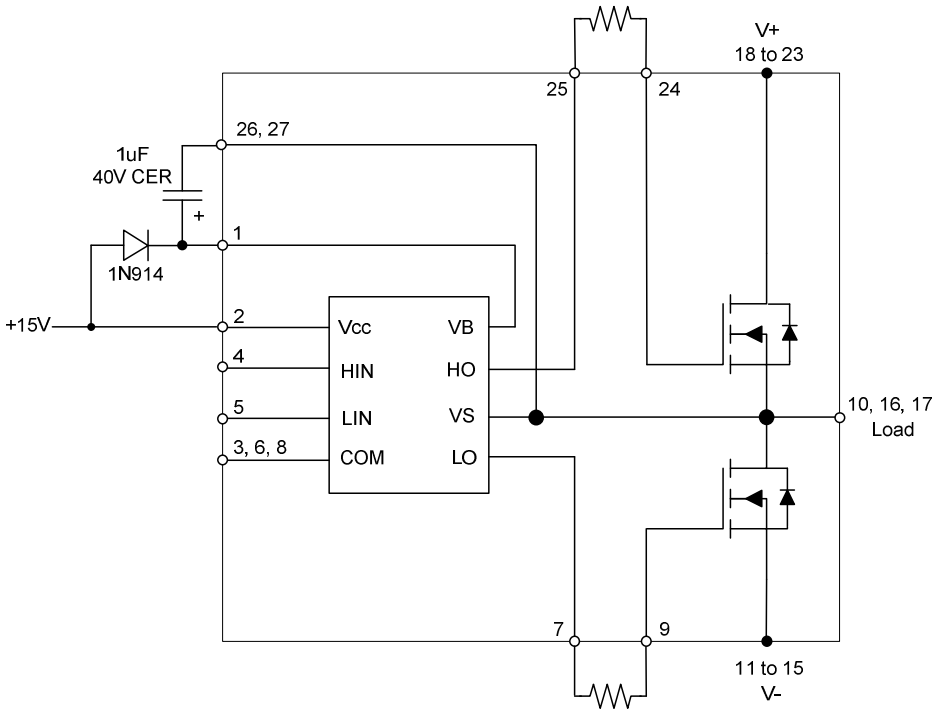


Figure 13: Typical Application Connection

1. Bus capacitors should be mounted as close to the module bus terminals as possible to reduce ringing and EMI problems. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
2. Value of the boot-strap capacitors depends upon the switching frequency. Their selection should be made based on IR Design tip DT04-4 or application note AN-1044.

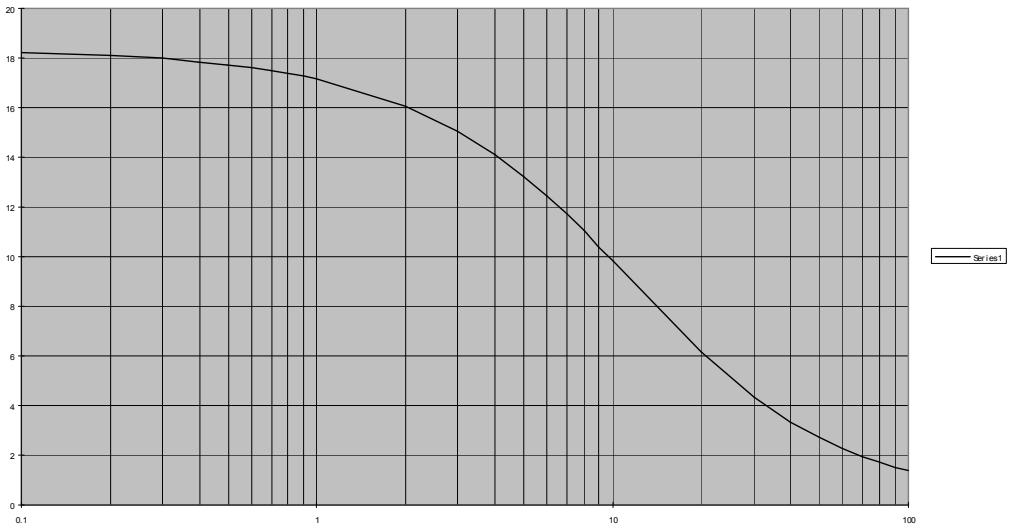


Figure 14: Typical Output Current (RMS of fundamental) vs. Modulation Frequency
Sinusoidal Modulation, V^+=32V, T_J=125°C, T_A=60°C, MI=1, PF=0.8, mounted on 50 mm^2 of FR4

Qualification

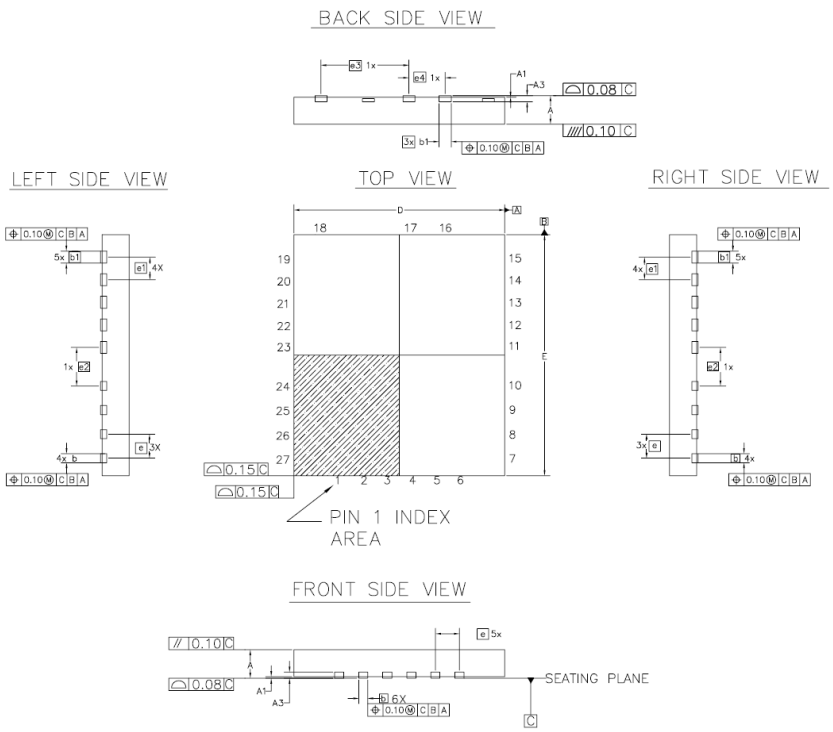
Qualification Level		Industrial†† (per JEDEC JESD 47E)
Moisture Sensitivity Level		MSL3††† (per IPC/JEDEC J-STD-020C)
ESD	Machine Model	Class B (±200V) (per JEDEC standard JESD22-A115A)
	Human Body Model	Class 1C (±1000V) (per EIA/JEDEC standard EIA/JES-001A-2011)
RoHS Compliant		Yes

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

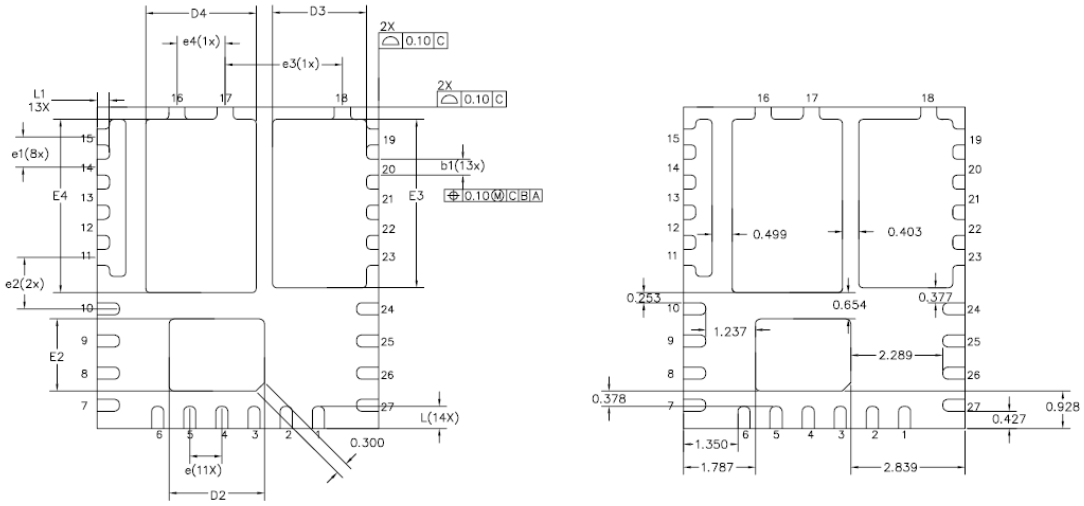
Package Outline (Top & Side view)



SYMBOL	DIMENSIONS IN MILLIMETER		
	MIN.	NOM.	MAX.
A	0.800	0.900	1.000
A1	0.000	–	0.050
A3	0.203 REF.		
b	0.250	0.300	0.350
b1	0.350	0.400	0.450
D	6.900	7.000	7.100
E	7.900	8.000	8.100
D2	2.323	2.373	2.423
E2	1.748	1.798	1.848
D3	2.290	2.340	2.390
E3	4.144	4.194	4.244
D4	2.698	2.748	2.798
E4	4.267	4.317	4.367
e	0.800 BSC		
e1	0.750 BSC		
e2	1.281 BSC		
e3	2.918 BSC		
e4	1.200 BSC		
L	0.500	0.550	0.600
L1	0.253	0.303	0.353

Package Outline (Bottom View, 1 of 2)

PACKAGE BOTTOM VIEW



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e4	1.200 BSC		
L	0.500	0.550	0.600
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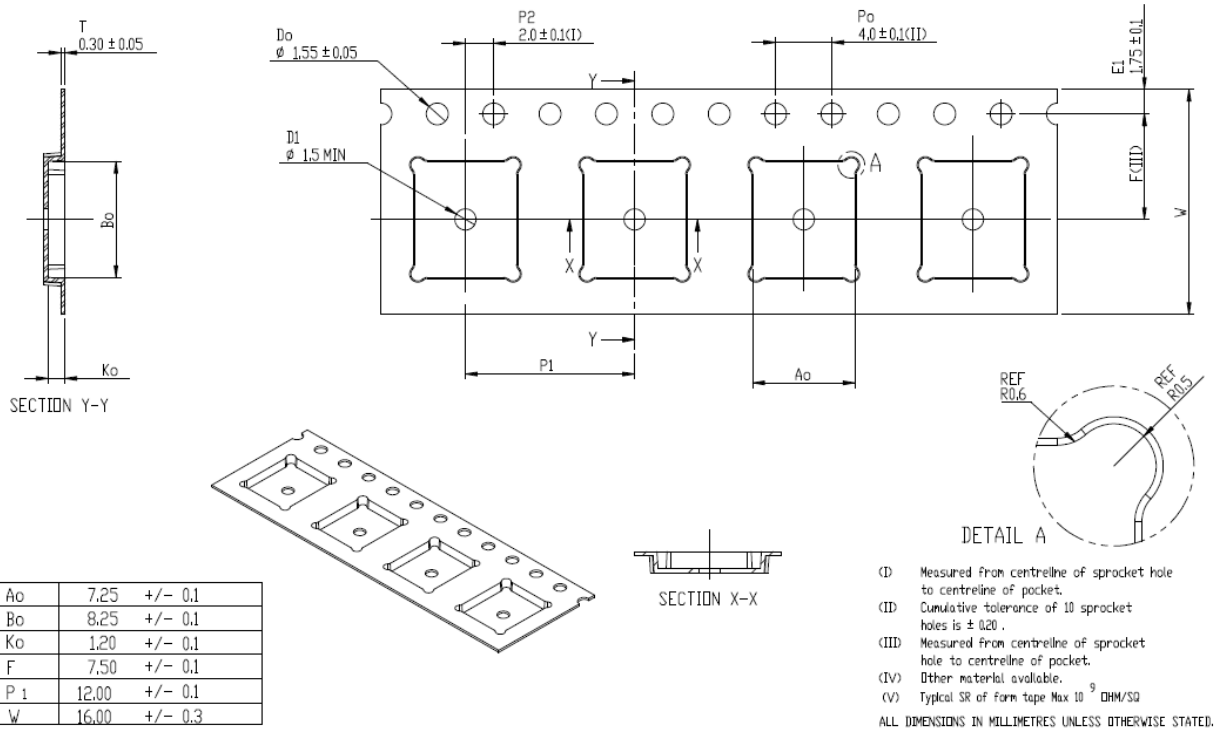
1. For mounting instruction see AN-1178.
2. For recommended PCB via design see AN-1091.
3. For recommended design, solder profile, integration and rework guidelines see AN-1028.
4. For board inspection guidelines see AN-1133.

Tape and Reel Details



Ao	7.25	+/- 0.1
Bo	8.25	+/- 0.1
Ko	1.20	+/- 0.1
F	7.50	+/- 0.1
P 1	12.00	+/- 0.1
W	16.00	+/- 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Typical SR of form tape Max 10^{9} OHM/SQ

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

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