

IRL1404ZPbF
IRL1404ZSPbF
IRL1404ZLPbF

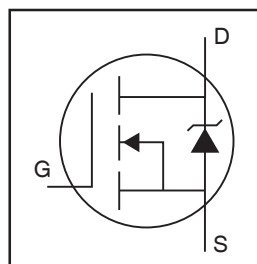
Features

- Logic Level
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free

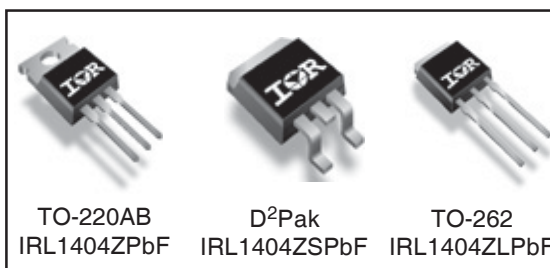
Description

This HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.

HEXFET® Power MOSFET



$V_{DSS} = 40V$
$R_{DS(on)} = 3.1m\Omega$
$I_D = 120A$



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	200 ^①	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	140 ^①	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	120 ^①	
I_{DM}	Pulsed Drain Current ^①	790	
$P_D @ T_C = 25^\circ C$	Power Dissipation	230	W
	Linear Derating Factor	1.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ^②	220	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ^⑥	490	
I_{AR}	Avalanche Current ^①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ^⑤		mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting Torque, 6-32 or M3 screw	300 (1.6mm from case) 10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.65	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ^⑦	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ^⑦	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ^⑧	—	40	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{BRDSS}	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{\text{GS}} = 0\text{V}$, $I_D = 250\mu\text{A}$
$\Delta V_{\text{BRDSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.034	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
$R_{\text{DS(on)}}$	Static Drain-to-Source On-Resistance	—	2.5	3.1	$\text{m}\Omega$	$V_{\text{GS}} = 10\text{V}$, $I_D = 75\text{A}$ ③⑩
		—	—	4.7		$V_{\text{GS}} = 5.0\text{V}$, $I_D = 40\text{A}$ ③
		—	—	5.9		$V_{\text{GS}} = 4.5\text{V}$, $I_D = 40\text{A}$ ③
$V_{\text{GS(th)}}$	Gate Threshold Voltage	1.4	—	2.7	V	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = 250\mu\text{A}$
g_{fs}	Forward Transconductance	120	—	—	S	$V_{\text{DS}} = 10\text{V}$, $I_D = 75\text{A}$ ⑩
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{\text{DS}} = 40\text{V}$, $V_{\text{GS}} = 0\text{V}$
		—	—	250		$V_{\text{DS}} = 40\text{V}$, $V_{\text{GS}} = 0\text{V}$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{\text{GS}} = 16\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{\text{GS}} = -16\text{V}$
Q_g	Total Gate Charge	—	75	110	nC	$I_D = 75\text{A}$ ⑩
Q_{gs}	Gate-to-Source Charge	—	28	—		$V_{\text{DS}} = 32\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	40	—		$V_{\text{GS}} = 5.0\text{V}$ ③
$t_{\text{d(on)}}$	Turn-On Delay Time	—	19	—	ns	$V_{\text{DD}} = 20\text{V}$
t_r	Rise Time	—	180	—		$I_D = 75\text{A}$ ⑩
$t_{\text{d(off)}}$	Turn-Off Delay Time	—	30	—		$R_G = 4.0\Omega$
t_f	Fall Time	—	49	—		$V_{\text{GS}} = 5.0\text{V}$ ③
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	5080	—	pF	$V_{\text{GS}} = 0\text{V}$
C_{oss}	Output Capacitance	—	970	—		$V_{\text{DS}} = 25\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	570	—		$f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	3310	—		$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 1.0\text{V}$, $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	870	—		$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 32\text{V}$, $f = 1.0\text{MHz}$
$C_{\text{oss eff.}}$	Effective Output Capacitance	—	1280	—		$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 0\text{V}$ to 32V ④

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	200 ⑤	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	790		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$, $I_S = 75\text{A}$ ⑩, $V_{\text{GS}} = 0\text{V}$ ③
t_{rr}	Reverse Recovery Time	—	26	39	ns	$T_J = 25^\circ\text{C}$, $I_F = 75\text{A}$ ⑩, $V_{\text{DD}} = 20\text{V}$
Q_{rr}	Reverse Recovery Charge	—	18	27	nC	$di/dt = 100\text{A}/\mu\text{s}$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$,
 $L = 0.079\text{mH}$, $R_G = 25\Omega$, $I_{\text{AS}} = 75\text{A}$, $V_{\text{GS}} = 10\text{V}$.
Part not recommended for use above this value.
- ③ Pulse width $\leq 1.0\text{ms}$; duty cycle $\leq 2\%$.
- ④ $C_{\text{oss eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

- ⑥ This value determined from sample failure population. 100% tested to this value in production.
- ⑦ This is only applied to TO-220AB package.
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
- ⑩ All AC and DC test condition based on former Package limited current of 75A.

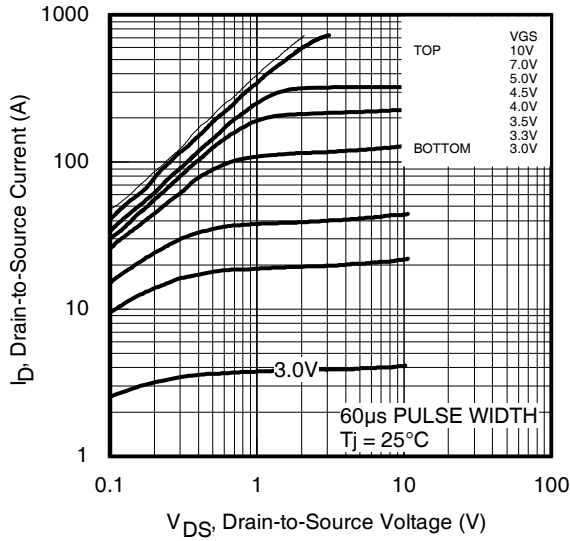


Fig 1. Typical Output Characteristics

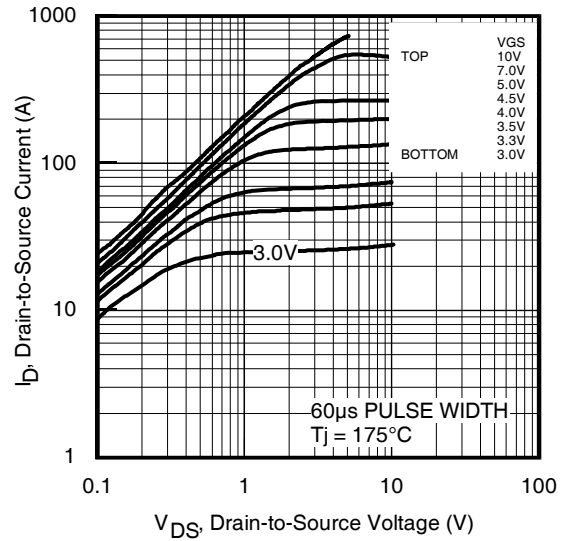


Fig 2. Typical Output Characteristics

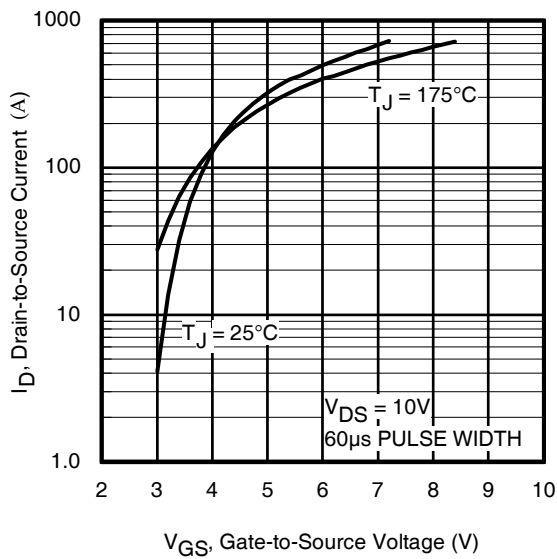


Fig 3. Typical Transfer Characteristics

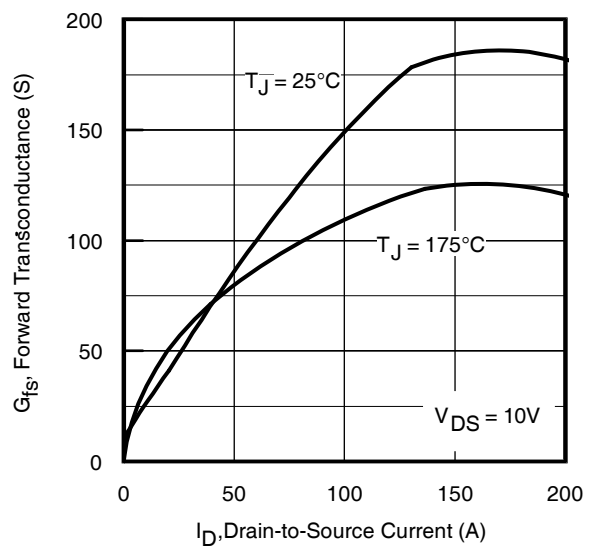


Fig 4. Typical Forward Transconductance vs. Drain Current

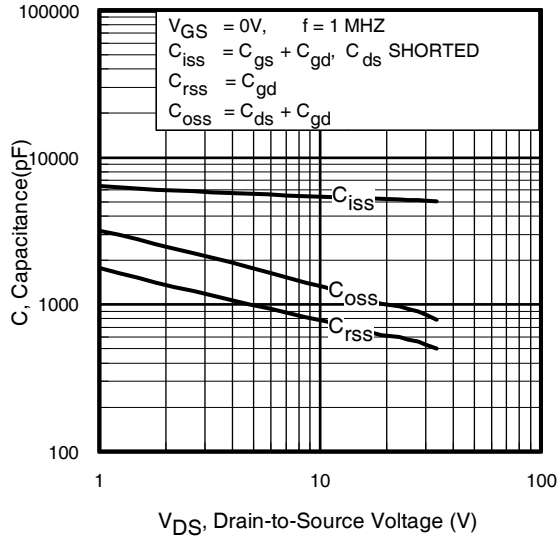


Fig 5. Typical Capacitance vs.
Drain-to-Source Voltage

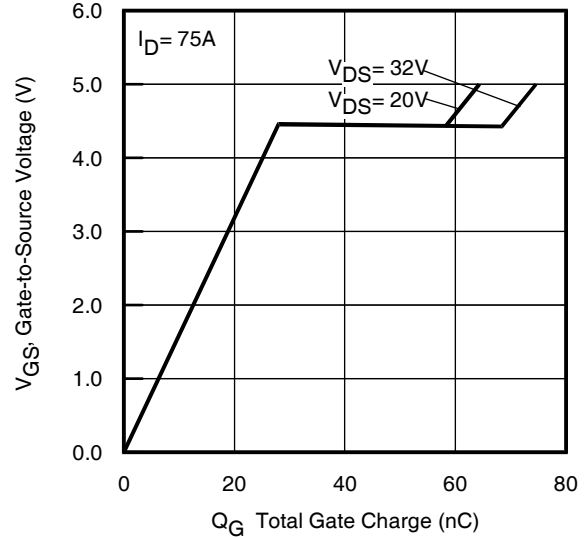


Fig 6. Typical Gate Charge vs.
Gate-to-Source Voltage

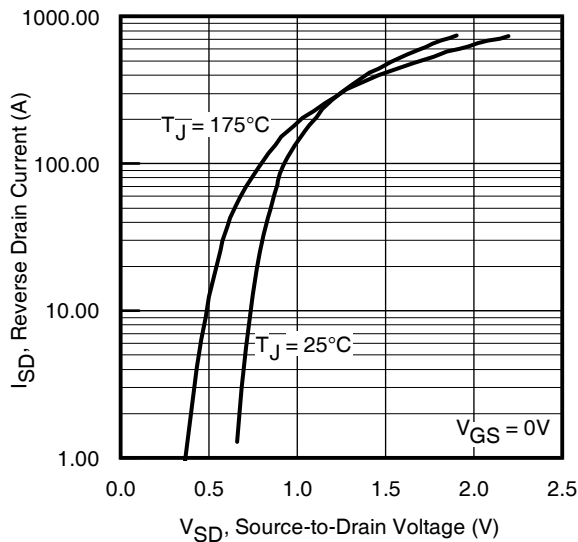


Fig 7. Typical Source-Drain Diode
Forward Voltage

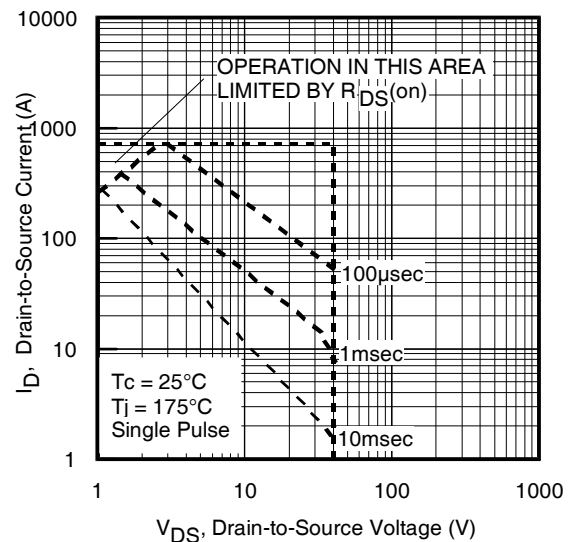


Fig 8. Maximum Safe Operating Area

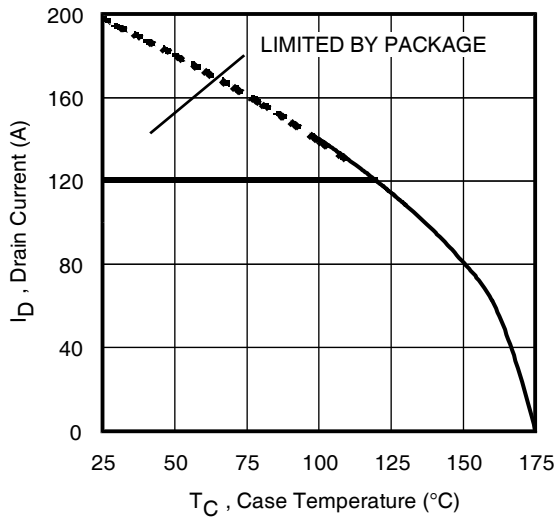


Fig 9. Maximum Drain Current vs. Case Temperature

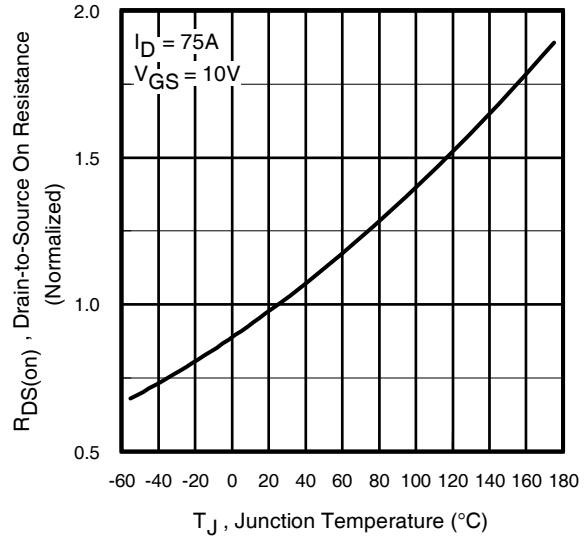


Fig 10. Normalized On-Resistance vs. Temperature

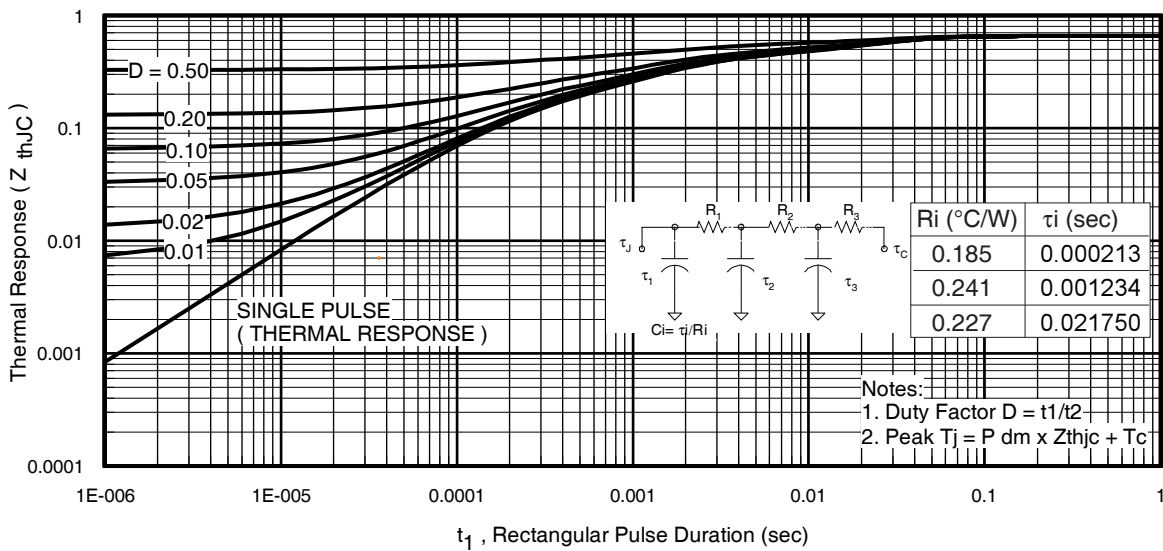


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRL1404Z/S/LPbF

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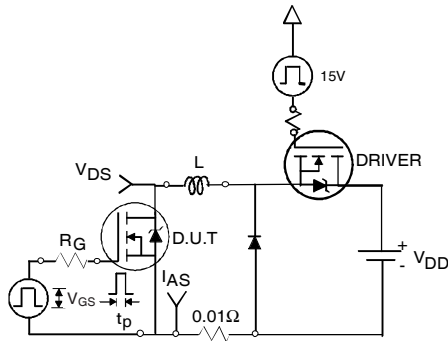


Fig 12a. Unclamped Inductive Test Circuit

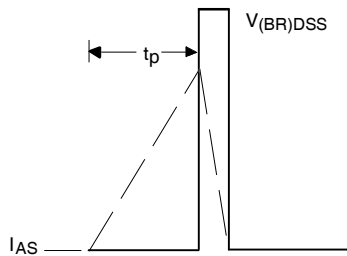


Fig 12b. Unclamped Inductive Waveforms

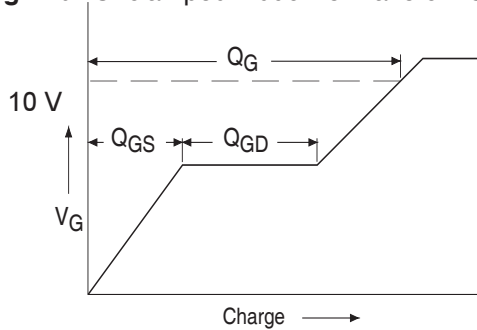


Fig 13a. Basic Gate Charge Waveform

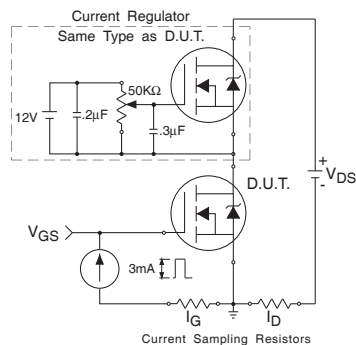


Fig 13b. Gate Charge Test Circuit

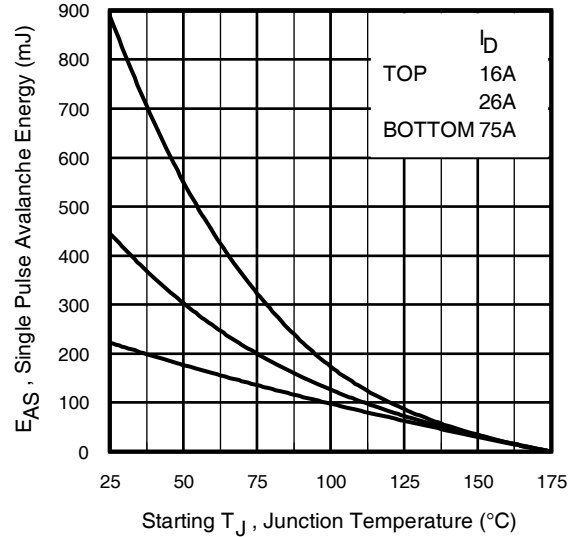


Fig 12c. Maximum Avalanche Energy vs. Drain Current

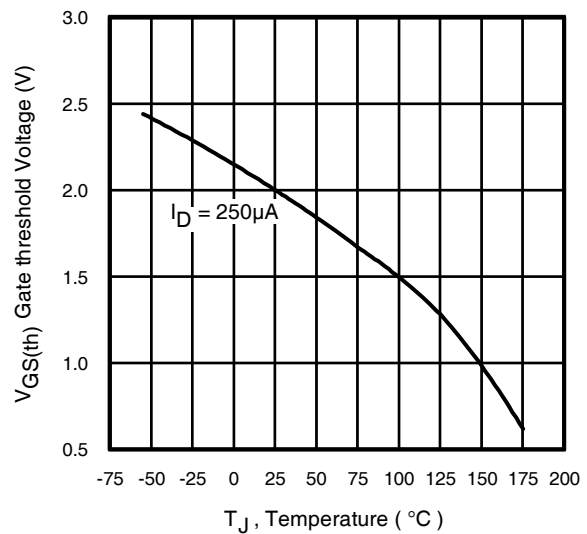


Fig 14. Threshold Voltage vs. Temperature

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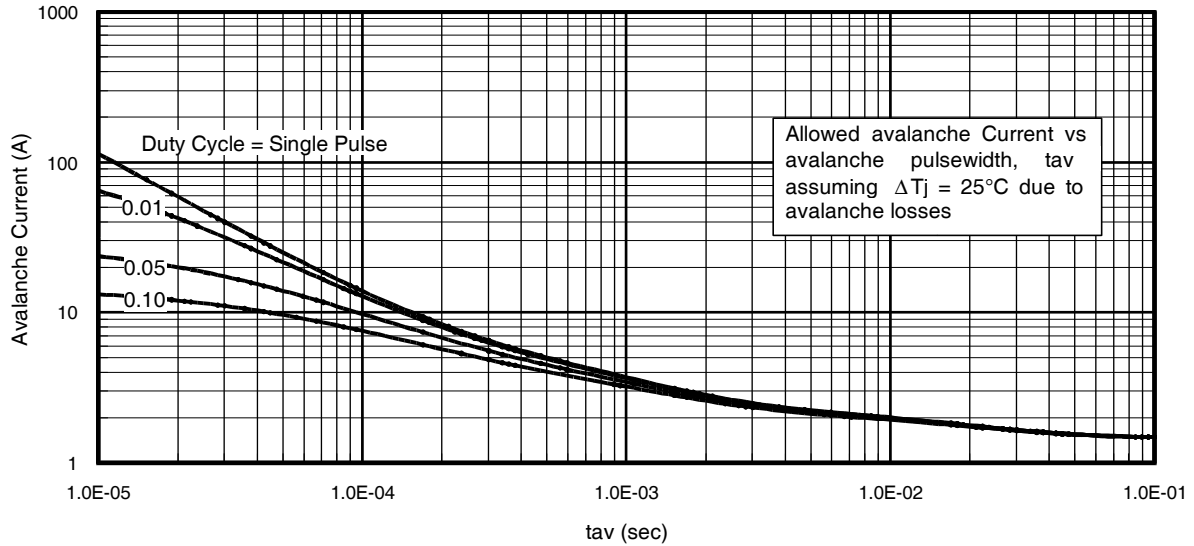


Fig 15. Typical Avalanche Current vs. Pulsewidth

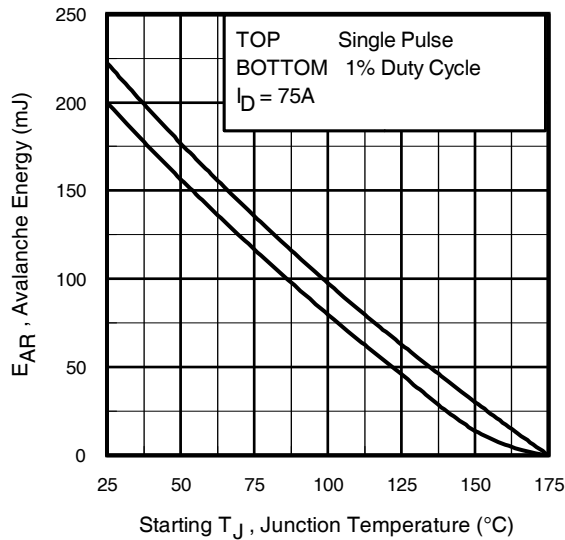


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

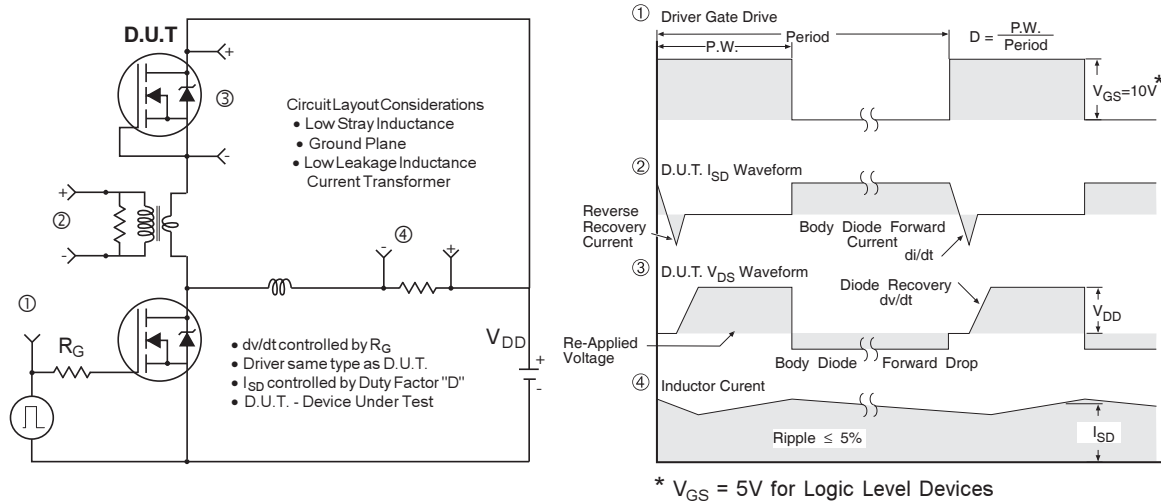


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

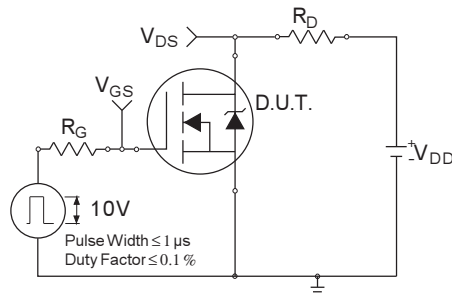


Fig 18a. Switching Time Test Circuit

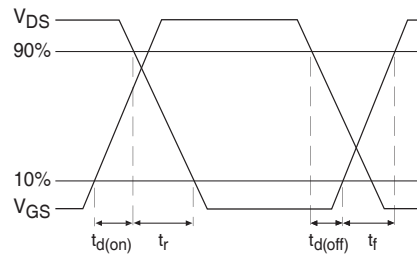
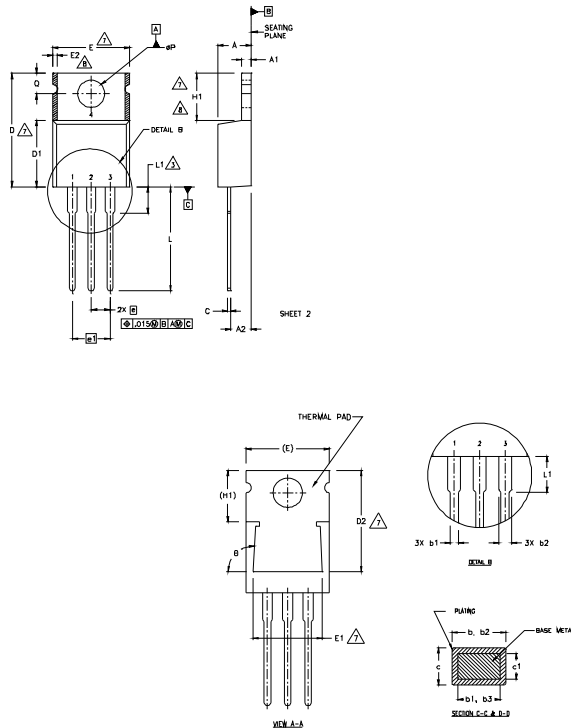


Fig 18b. Switching Time Waveforms

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5 M-1994.
2. DIMENSIONS ARE SHOWN IN INCHES (MILLIMETERS).
3. LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DIMENSION b1 & c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCHES.
7. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E, H1, D2 & E1.
8. DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.

LEAD ASSIGNMENTS

HEBET

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

06E1, 06P2, 06Q3

- 1 - GATE
- 2 - COLLECTOR
- 3 - EMITTER

06E1, 06P2, 06Q3

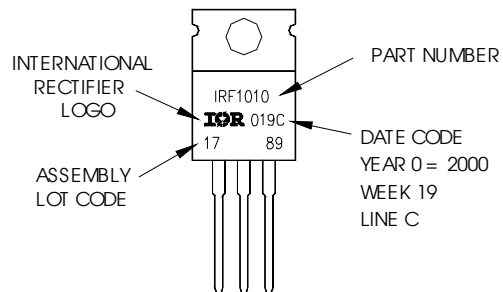
- 1 - ANODE/OPEN
- 2 - CATHODE
- 3 - ANODE

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.82	.140	.190	5
A1	0.51	1.40	.020	.055	
A2	2.04	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.96	.015	.038	
b2	1.15	1.77	.045	.070	5
b3	1.15	1.73	.045	.068	
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	
D	14.22	16.51	.560	.650	
D1	8.38	9.02	.330	.355	7
D2	12.19	12.88	.480	.507	
E	9.66	10.66	.380	.420	
E1	8.38	8.89	.330	.350	
e	2.54 BSC		.100 BSC		
e1	5.08		.200 BSC		7,8
H1	5.85	6.55	.230	.270	
L	12.70	14.73	.500	.580	
L1	-	6.35	-	.250	
#P	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	3
Ø	90°-93°		90°-93°		

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position
indicates "Lead - Free"

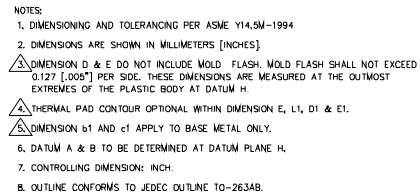


Notes:

1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

International
IOR Rectifier

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	.160	.190
A1	0.00	0.254	.000	.010
b	0.51	0.99	.020	.039
b1	0.51	0.89	.020	.035
b2	1.14	1.78	.045	.070
c	0.14	1.73	.005	.068
c1	0.34	0.76	0.015	.030
c2	0.38	0.68	.015	.023
d	1.14	1.65	.045	.065
D	8.38	9.65	.330	.380
D1	6.86	-	.270	-
E	9.65	10.67	.380	.420
E1	6.22	-	.245	-
E2	2.54	2.98	.100	.120
H	14.61	0.89	.575	.625
L	1.14	2.78	.070	.110
L1	-	1.65	-	.066
L2	1.27	1.78	-	.070
L3	0.25 BSC		.010 BSC	
L4	4.78	5.28	.188	.208

HEXFET

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

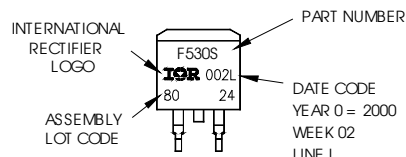
1. - GATE
2, 4. - COLLECTOR
3. - EMITTER

- 1.- ANODE *
- 2, 4.- CATHODE
- 3.- ANODE

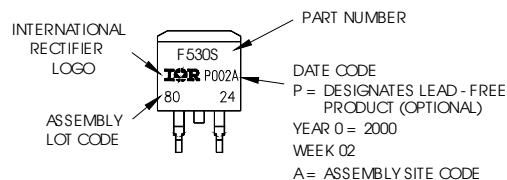
* PART DEPENDENT.

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead - Free"



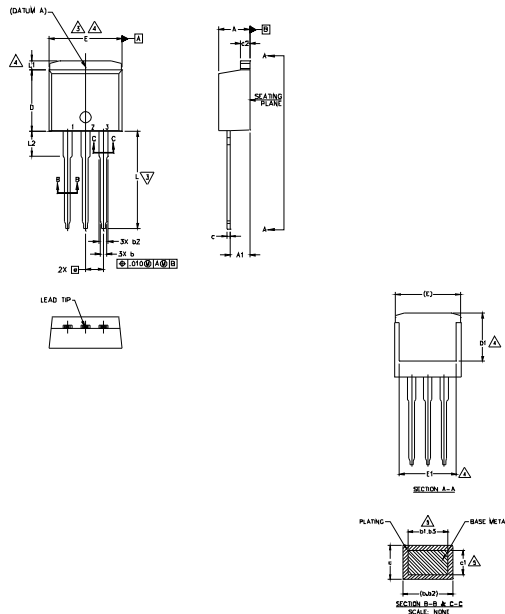
OR



1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

TO-262 Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b1(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	5
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	5
b3	1.14	1.73	.045	.068	
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	3
D	8.38	9.65	.330	.380	
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3, 4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		4
L	13.46	14.10	.530	.555	
L1	—	1.65	—	.065	
L2	3.56	3.71	.140	.146	

LEAD ASSIGNMENTS

HEXFET

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

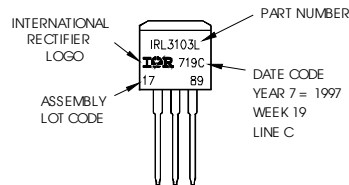
IGBTs, CoPACK

1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

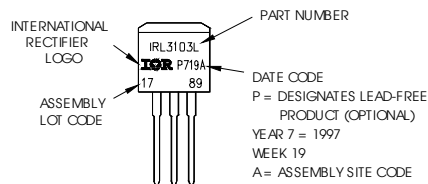
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL1303L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position
indicates "Lead - Free"



OR



Notes:

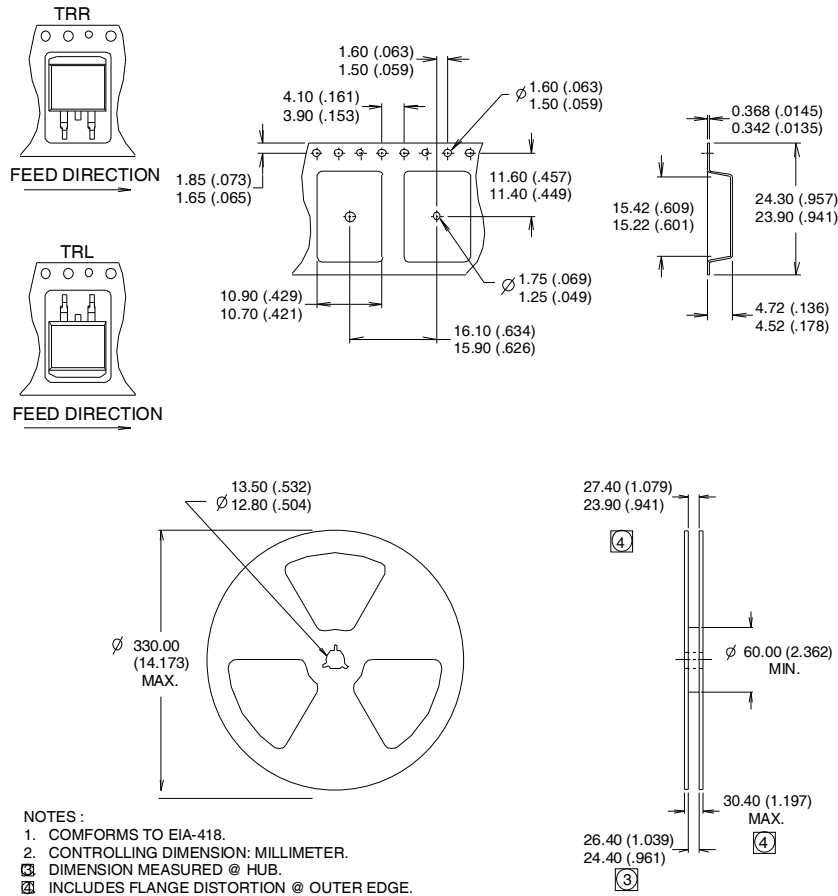
1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

IRL1404Z/S/LPbF

International
IR Rectifier

D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier

IR WORLD HEADQUARTERS: 101N.Sepulveda blvd, El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

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