

MOSFET

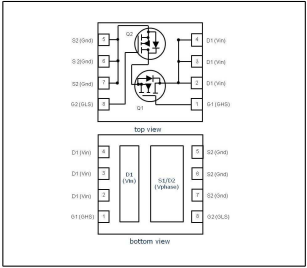
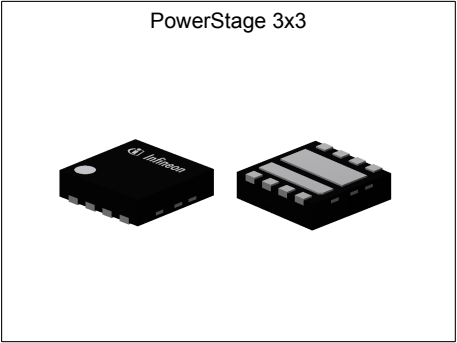
PowerStage 3x3

Features

- Dual N-channel OptiMOS™ MOSFET
- Enhancement mode
- Logic level (4.5V rated)
- Avalanche rated
- 100% Lead-free; RoHS compliant
- Halogen-free according to IEC61249-2-21

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	30	V
$R_{DS(on),max}$	18	mΩ
I_D	20	A
Q_{OSS}	2.3	nC
$Q_G(0V..4.5V)$	1.8	nC



Type / Ordering Code	Package	Marking	Related Links
BSZ0909ND	PG-WISON-8	0909ND	-

Table of Contents

Description 1

Maximum ratings 3

Thermal characteristics 3

Electrical characteristics 4

Electrical characteristics diagrams 6

Package Outlines 10

Revision History 11

Trademarks 11

Disclaimer 11

1 Maximum ratings

at $T_j=25\text{ }^{\circ}\text{C}$, unless otherwise specified, one transistor active

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	20 8.1 5.5 4.1	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ }^{\circ}\text{C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ }^{\circ}\text{C}^{1)}$ $V_{GS}=4.5\text{ V}$, $T_A=70\text{ }^{\circ}\text{C}^{1)}$ $V_{GS}=4.5\text{ V}$, $T_A=25\text{ }^{\circ}\text{C}^{2)}$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	40	A	$T_C=25\text{ }^{\circ}\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	4	mJ	$I_D=9\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	17 1.9	-	W	$T_C=25\text{ }^{\circ}\text{C}$ $T_A=25\text{ }^{\circ}\text{C}$, $R_{thJA}=65\text{ }^{\circ}\text{C/W}^{1)}$
Operating and storage temperature	T_j , T_{stg}	-55	-	150	$^{\circ}\text{C}$	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	7.5	$^{\circ}\text{C/W}$	-
Device on PCB, minimal footprint	R_{thJA}	-	-	180	$^{\circ}\text{C/W}$	-
Device on PCB, 6 cm ² cooling area	R_{thJA}	-	-	65	$^{\circ}\text{C/W}$	-

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

²⁾ device mounted on a minimum pad (one layer, 70 μm thick)

³⁾ See Diagram 3 for more detailed information

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2	V	$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	-	1 100	μA	$V_{DS}=30\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=30\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=150\text{ }^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	20 14.5	25 18	m Ω	$V_{GS}=4.5\text{ V}$, $I_D=9\text{ A}$ $V_{GS}=10\text{ V}$, $I_D=9\text{ A}$
Gate resistance ¹⁾	R_G	3.5	7	14	Ω	-
Transconductance	g_{fs}	-	22	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=9\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	270	360	pF	$V_{GS}=0\text{ V}$, $V_{DS}=15\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	88	120	pF	$V_{GS}=0\text{ V}$, $V_{DS}=15\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	11	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=15\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	5	-	ns	$V_{DD}=15\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=9\text{ A}$, $R_{G,ext}=6\text{ }\Omega$
Rise time	t_r	-	2.5	-	ns	$V_{DD}=15\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=9\text{ A}$, $R_{G,ext}=6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	15	-	ns	$V_{DD}=15\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=9\text{ A}$, $R_{G,ext}=6\text{ }\Omega$
Fall time	t_f	-	2	-	ns	$V_{DD}=15\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=9\text{ A}$, $R_{G,ext}=6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	0.8	-	nC	$V_{DD}=15\text{ V}$, $I_D=9\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	0.4	-	nC	$V_{DD}=15\text{ V}$, $I_D=9\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge	Q_{gd}	-	0.5	-	nC	$V_{DD}=15\text{ V}$, $I_D=9\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	Q_{sw}	-	0.8	-	nC	$V_{DD}=15\text{ V}$, $I_D=9\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total	Q_g	-	1.8	2.6	nC	$V_{DD}=15\text{ V}$, $I_D=9\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	2.8	-	V	$V_{DD}=15\text{ V}$, $I_D=9\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total	Q_g	-	3.7	5.2	nC	$V_{DD}=15\text{ V}$, $I_D=9\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	1.5	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Output charge	Q_{oss}	-	2.3	-	nC	$V_{DD}=15\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	17	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	40	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.92	1.2	V	$V_{GS}=0\text{ V}$, $I_F=9\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery charge	Q_{rr}	-	5	-	nC	$V_R=15\text{ V}$, $I_F=9\text{ A}$, $di_F/dt=400\text{ A}/\mu\text{s}$

4 Electrical characteristics diagrams

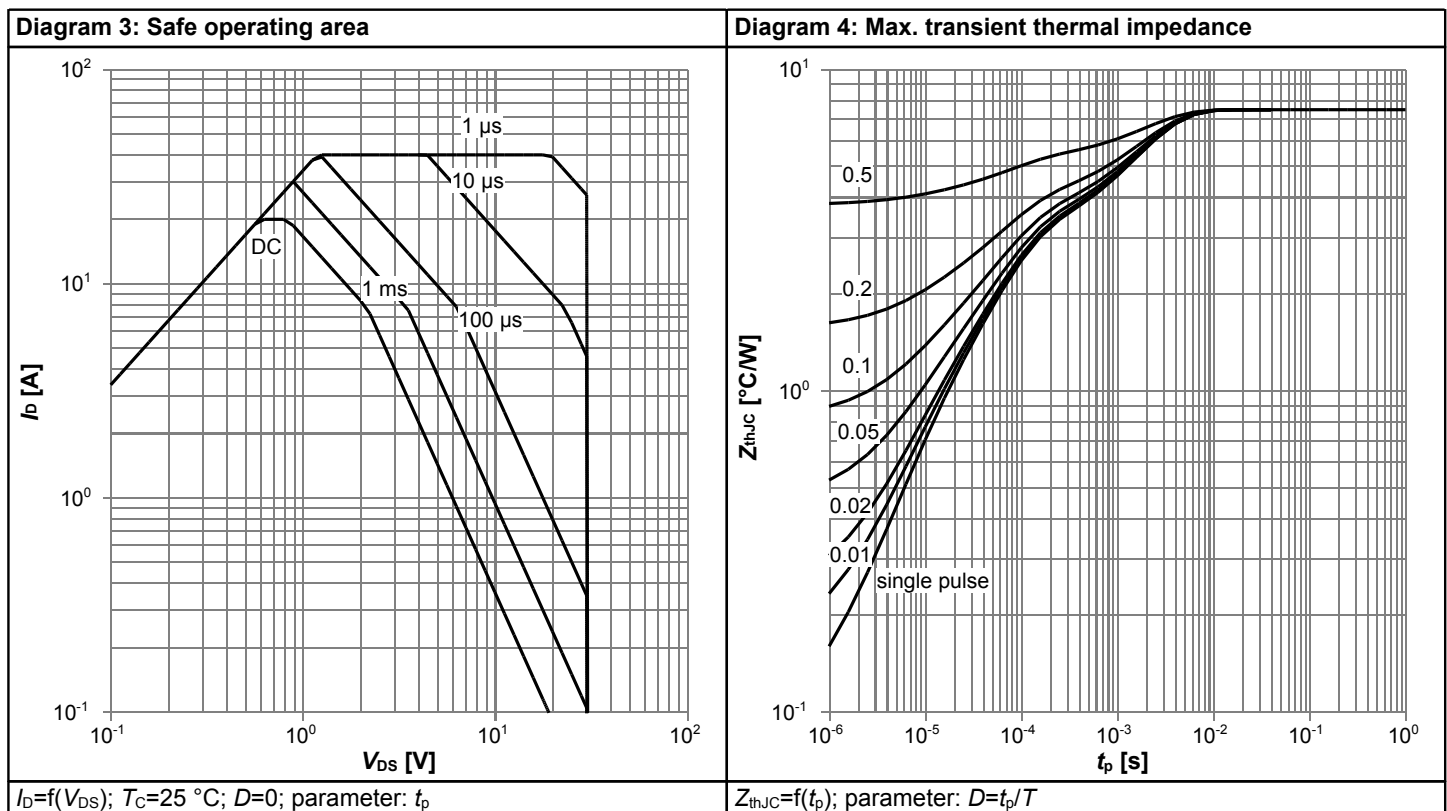
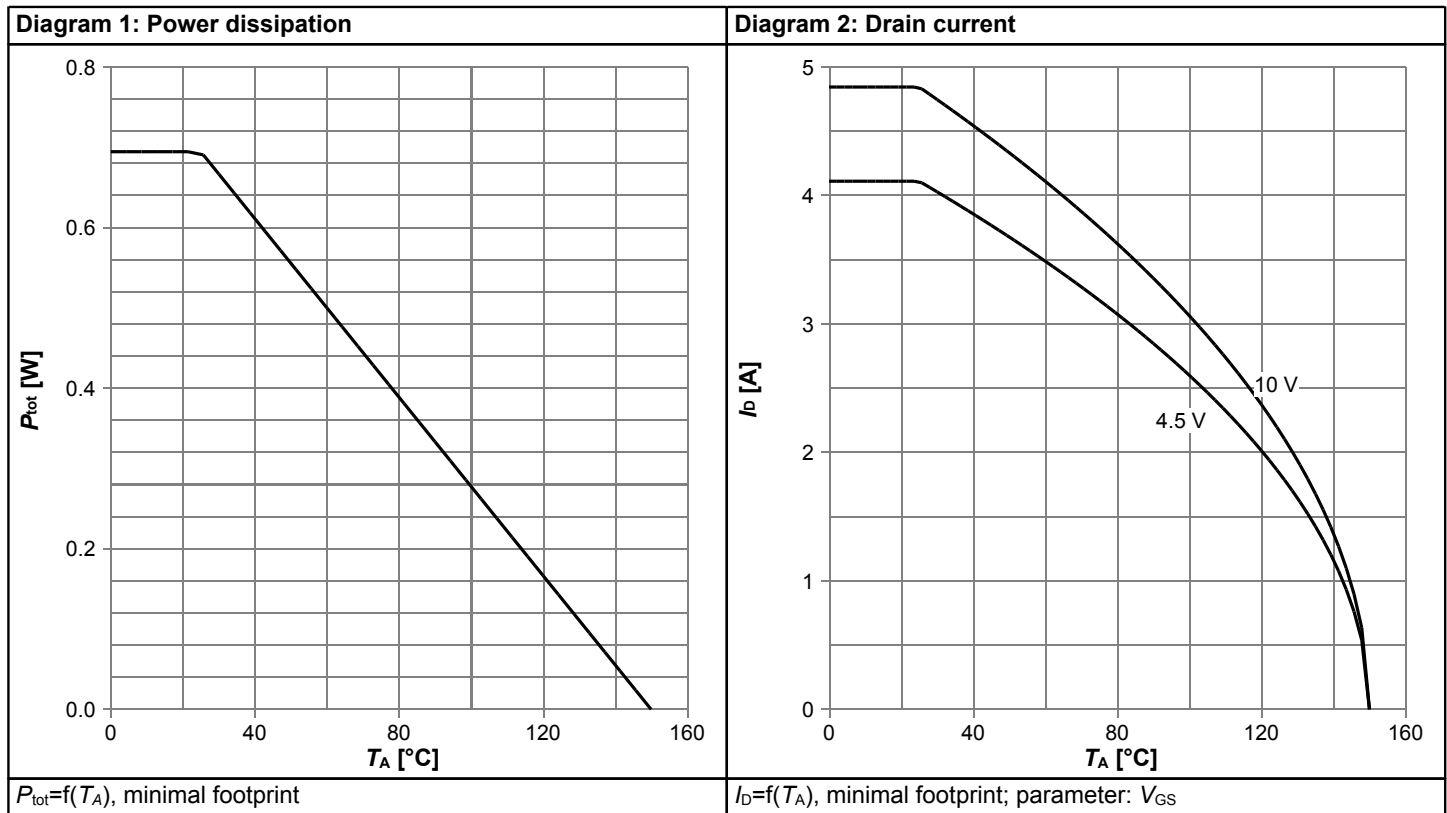
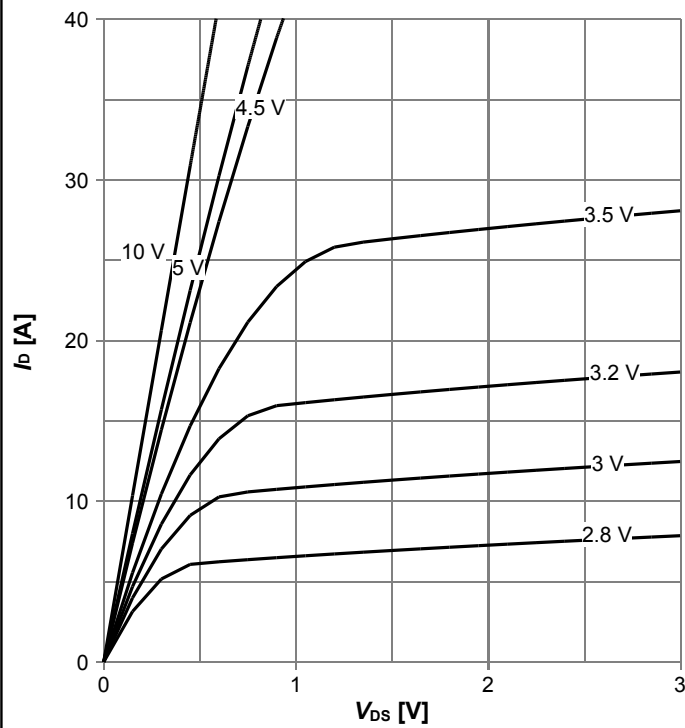
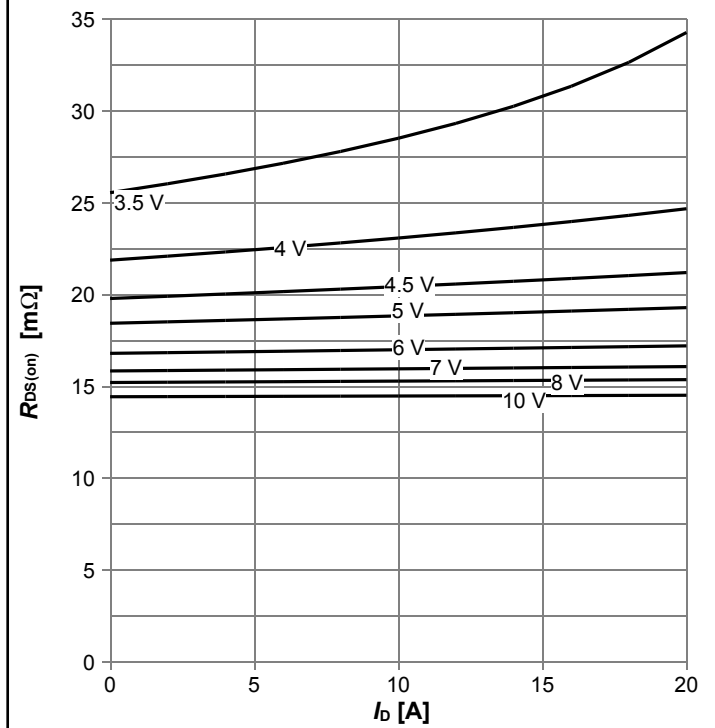


Diagram 5: Typ. output characteristics



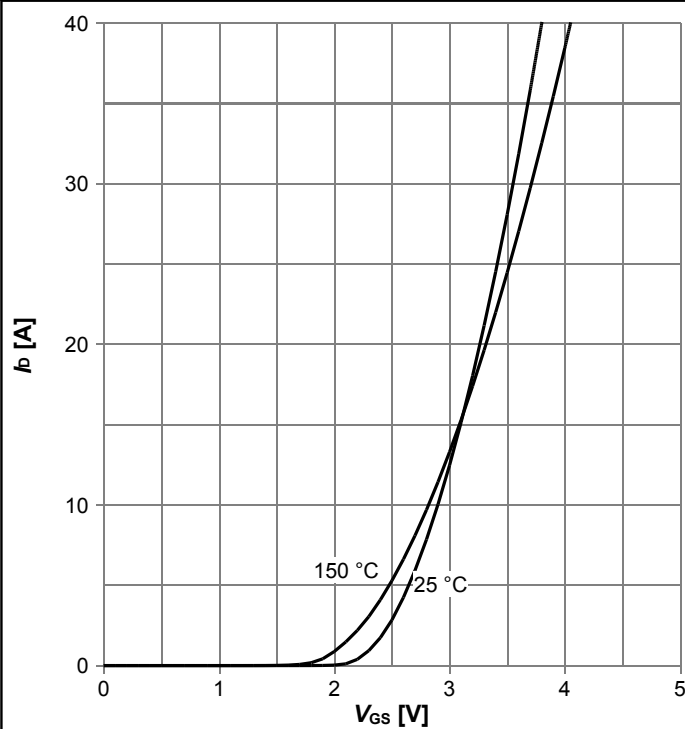
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



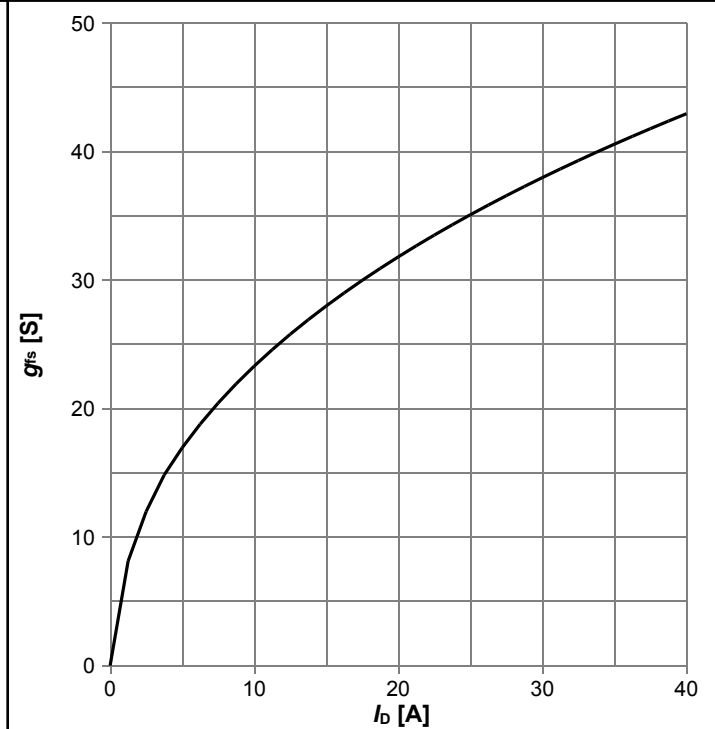
$R_{DS(on)} = f(I_D)$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



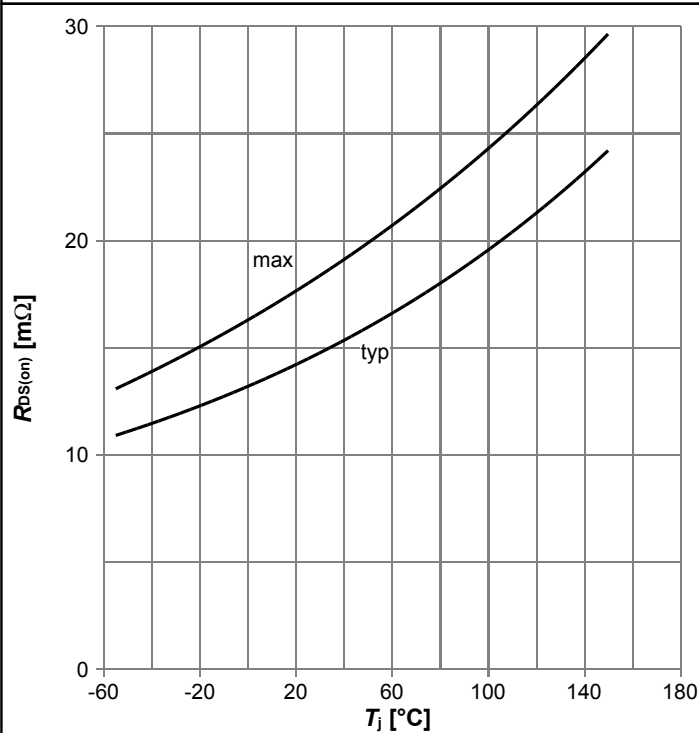
$I_D = f(V_{GS})$; $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



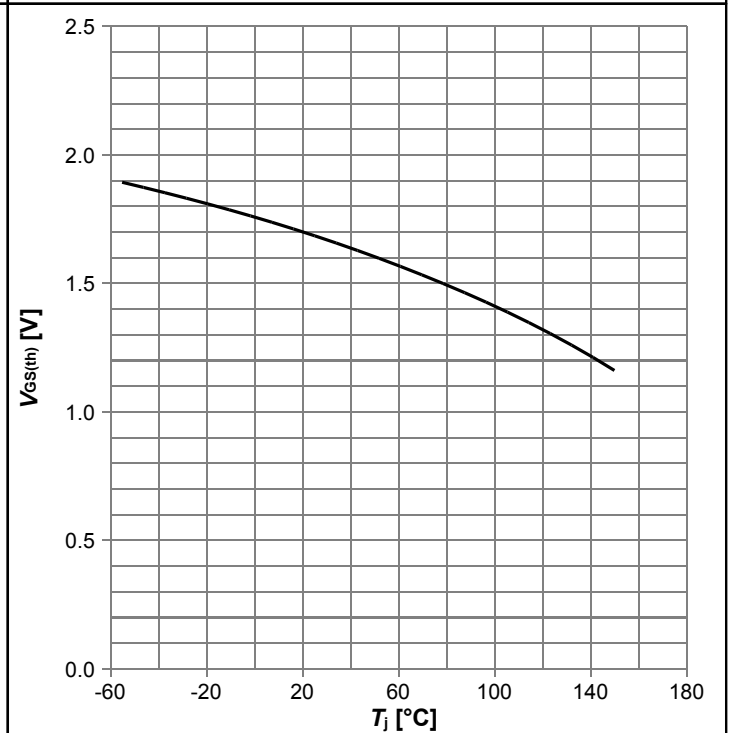
$g_{fs} = f(I_D)$; $T_j = 25^\circ\text{C}$

Diagram 9: Drain-source on-state resistance



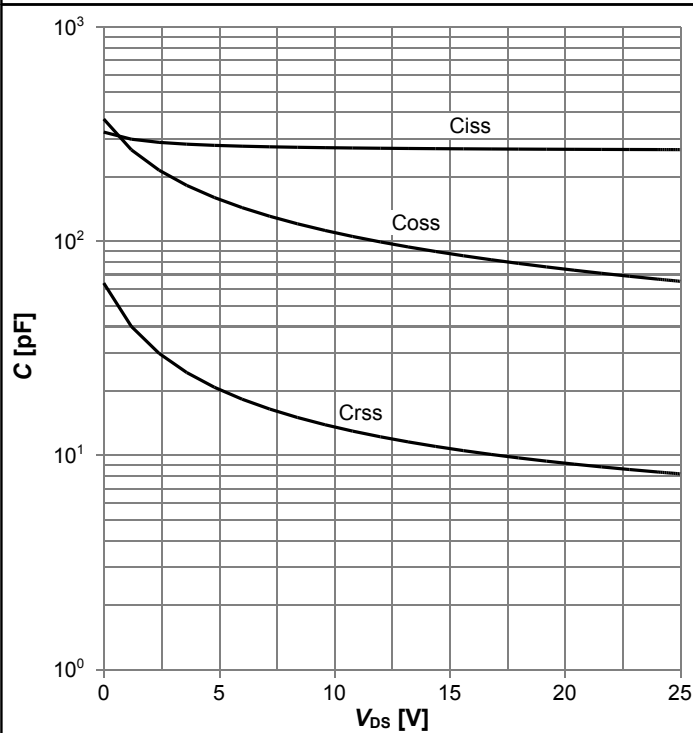
$R_{DS(on)}=f(T_j)$; $I_D=9$ A; $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



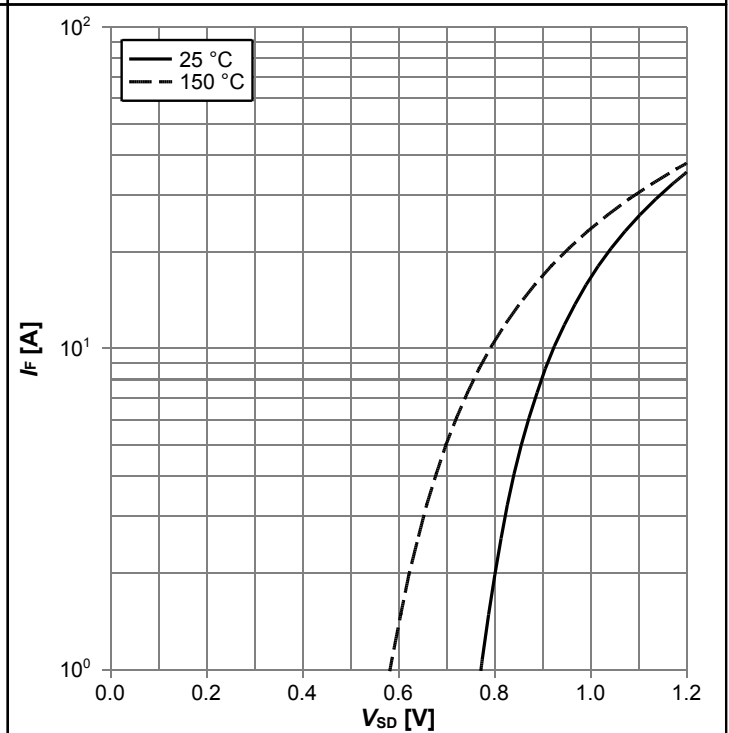
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; $I_D=250$ μ A

Diagram 11: Typ. capacitances



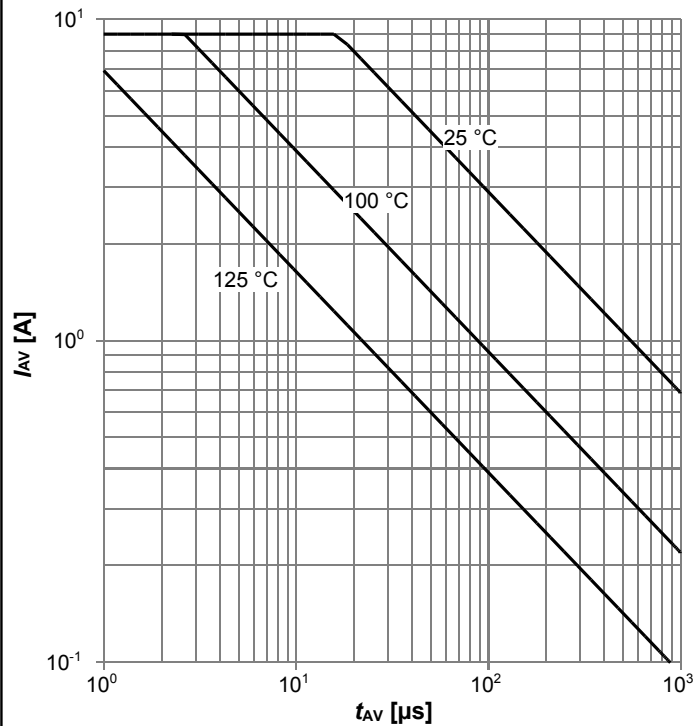
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode



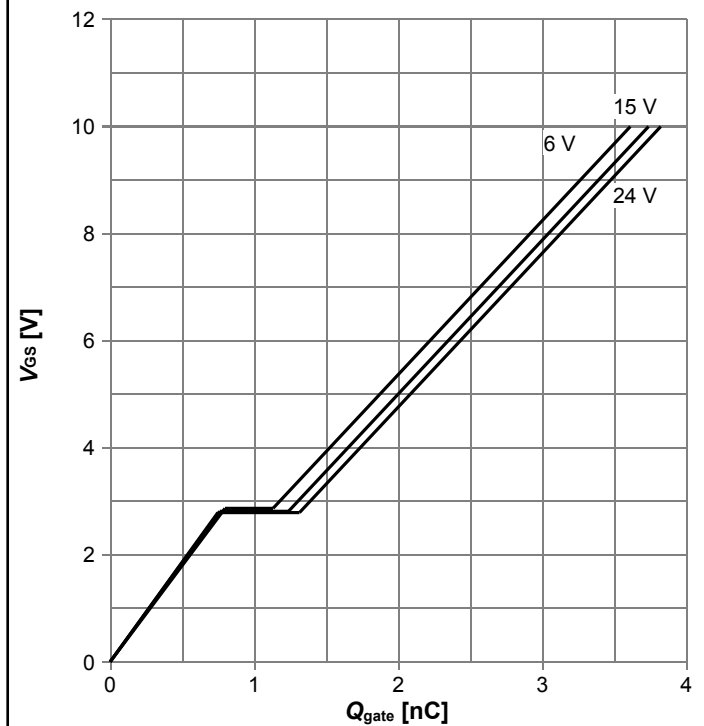
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



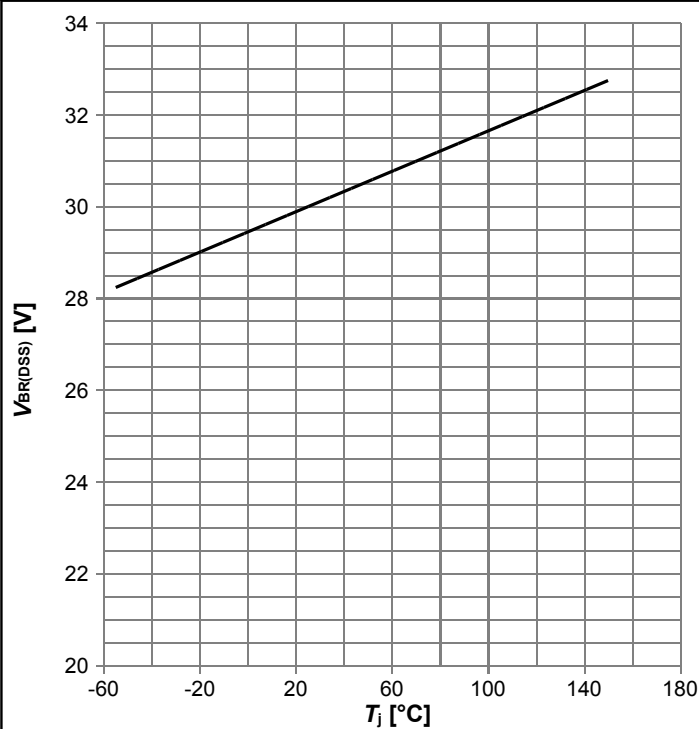
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



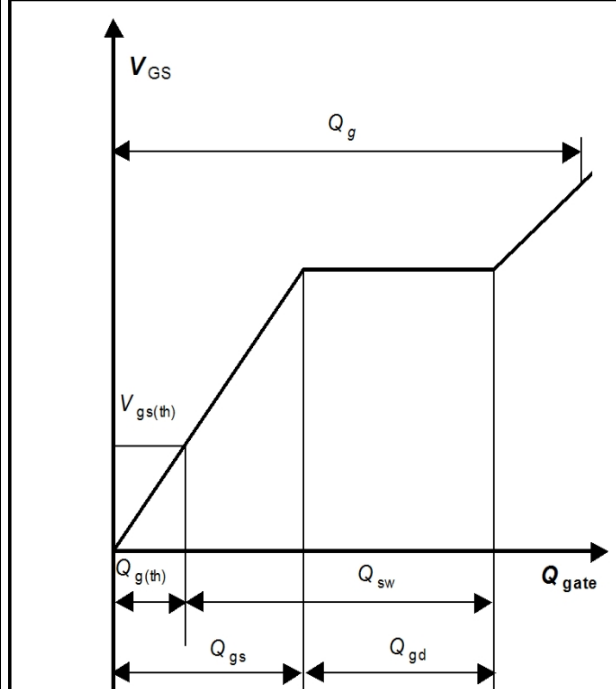
$V_{GS}=f(Q_{gate})$; $I_D=9\text{ A}$ pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

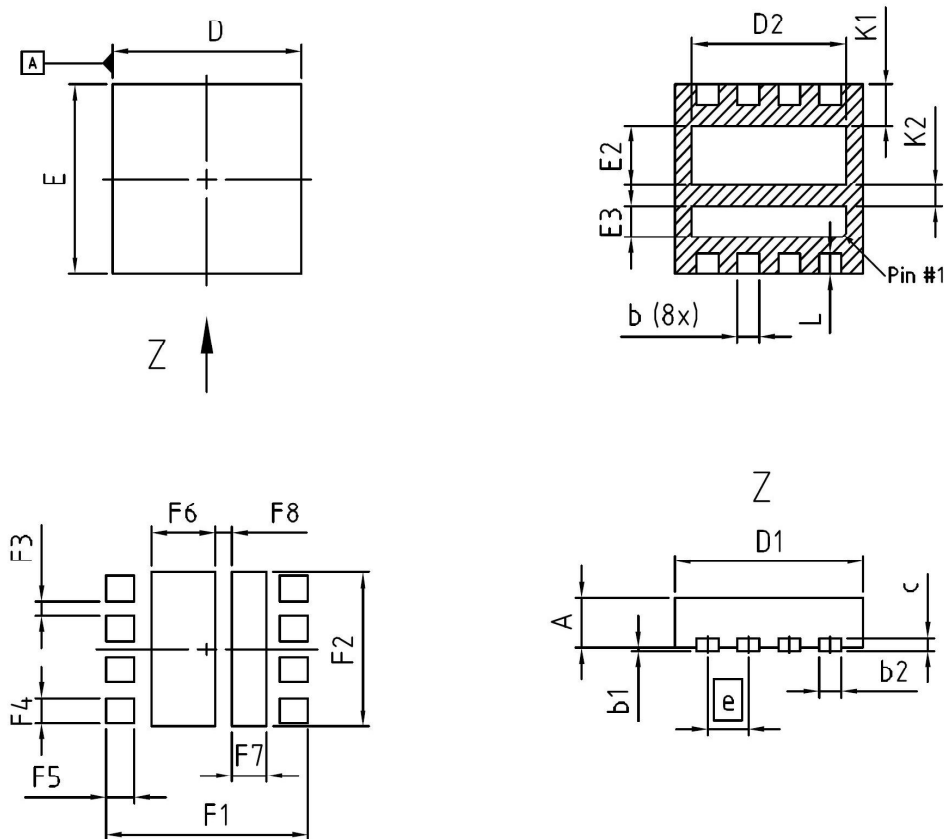


$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Gate charge waveforms



5 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.90	0.028	0.035
b	0.25	0.45	0.010	0.018
b1	0.00	0.05	0.000	0.002
b2	0.25	0.45	0.010	0.018
c	0.10	0.30	0.004	0.012
D=D1	2.90	3.10	0.114	0.122
D2	2.35	2.55	0.093	0.100
E=E1	2.90	3.10	0.114	0.122
E2	0.85	1.05	0.033	0.041
E3	0.39	0.59	0.015	0.023
K1	0.55	0.75	0.022	0.030
K2	0.23	0.43	0.009	0.017
e	0.65 (BSC)		0.026 (BSC)	
N	8		8	
L	0.22	0.42	0.009	0.017
F1	3.21		0.126	
F2	2.45		0.096	
F3	0.25		0.010	
F4	0.40		0.016	
F5	0.45		0.018	
F6	1.01		0.040	
F7	0.55		0.022	
F8	0.27		0.011	

DOCUMENT NO. Z8B00158767	
SCALE	0 2.5 5mm
EUROPEAN PROJECTION	
ISSUE DATE 15-09-2010	
REVISION 01	

Figure 1 Outline PG-WISON-8, dimensions in mm/inches

Revision History

BSZ0909ND

Revision: 2016-12-05, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-12-05	Release of final version

Trademarks of Infineon Technologies AG

AURIX™, C166™, CanPAK™, CIPOS™, CoolGaN™, CoolMOS™, CoolSET™, CoolSiC™, CORECONTROL™, CROSSAVE™, DAVE™, DI-POL™, DrBlade™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, Infineon™, ISOFACE™, IsoPACK™, i-Wafer™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OmniTune™, OPTIGA™, OptiMOS™, ORIGA™, POWERCODE™, PRIMARION™, PrimePACK™, PrimeSTACK™, PROFET™, PRO-SiL™, RASIC™, REAL3™, ReverSave™, SatRIC™, SIEGET™, SiPMOS™, SmartLEWIS™, SOLID FLASH™, SPOC™, TEMPFET™, thinQ!™, TRENCHSTOP™, TriCore™.

Trademarks updated August 2015

Other Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

erratum@infineon.com

Published by
Infineon Technologies AG
81726 München, Germany
© 2016 Infineon Technologies AG
All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.