

CTVS — Ceramic transient voltage suppressors

SMD multilayer transient voltage suppressors,
high-speed series

Series/Type:

Date: February 2016

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Multilayer varistors (MLVs)

High-speed series

SMD

EPCOS type designation system for high-speed series, single chips

CT	0402	V150	HS	G
Construction: CT $\triangle$ Single chip with nickel barrier termination (AgNiSn)				
Case sizes: 0402 0603				
Maximum RMS operating voltage (V_{RMS}): S5 $\triangle$ 4 V S14 $\triangle$ 14 V L25 $\triangle$ 25 V Or: Indication of the varistor voltage: V150 $\triangle$ 150 V V275 $\triangle$ 275 V				
Internal coding				
Taping mode: G $\triangle$ 180-mm reel, 7" G2 $\triangle$ 330-mm reel, 13"				

Multilayer varistors (MLVs)

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EPCOS type designation system for high-speed series, array

CA	05	M2	S10	T	100H	G
Construction: CA $\triangleq$ Chip array with nickel barrier termination (AgNiSn)						
Case sizes: 05 $\triangleq$ 0508 array 06 $\triangleq$ 0612 array						
Number of elements per component: M2 $\triangleq$ Array with two elements P4 $\triangleq$ Array with four elements						
Maximum RMS operating voltage (V_{RMS}): S10 $\triangleq$ 10 V S14 $\triangleq$ 14 V Typical varistor voltage (V_v): V150 $\triangleq$ 150 V						
Internal coding						
High-speed series 100H $\triangleq$ Matched capacitance varistor (MCV array with $C_{yp} = 10 \cdot 10^0 = 10$ pF) HS $\triangleq$ 4-fold array						
Taping mode: G $\triangleq$ 180-mm reel, 7"						

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Description

The high-speed series comprises a range of multilayer ceramic varistors for protection against ESD on data lines.

Features

- ESD protection level acc. to ISO 10605, IEC 61000-4-2 level 4
- Capacitance ratings down to 0.6 pF
- Low insertion loss
- Low leakage current
- No signal distortion
- Long-term ESD stability
- Bidirectional protection
- RoHS-compatible
- Suitable for lead-free soldering
- PSpice simulation models available

Applications

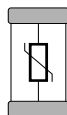
- ESD protection for high-speed data lines such as USB 2.0, firewire, IEEE 1394 interfaces, RF antennas, RF modules
- Selected types for ESD protection for high-speed automotive data lines (e.g. CAN bus, FlexRay)
- ESD protection for I/O ports of video and audio lines
- Integrated solutions for connectors in mobile communication and handheld devices

Design

- Multilayer technology
- Flammability rating better than UL 94 V-0
- Termination (see “Soldering directions”):
 - CT and CA types with nickel barrier terminations (AgNiSn), recommended for lead-free soldering, and compatible with tin/lead solder.

Single chip

Internal circuit



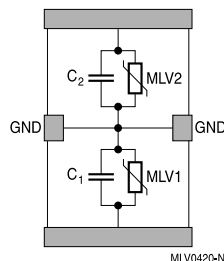
MLV0006-H

Available case sizes:

EIA	Metric
0402	1005
0603	1608

Matched capacitance varistor array (MCV array)

Internal circuit



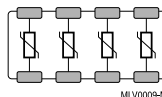
MLV0420-N

Available case sizes:

EIA	Metric	Version
0508	1220	2-fold array

4-fold array

Internal circuit



MLV0009-M

Available case sizes:

EIA	Metric	Version
0508	1220	4-fold array
0612	1632	4-fold array

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General technical data for single chips

Maximum RMS operating voltage		$V_{RMS,max}$	4 ... 25	V
Maximum DC operating voltage		$V_{DC,max}$	5.5 ... 32	V
Contact discharge ESD capability	to IEC 61000-4-2	$V_{ESD,contact}$	8	kV
Air discharge ESD capability	to IEC 61000-4-2	$V_{ESD,air}$	15	kV
Maximum surge current	(8/20 μ s)	$I_{surge,max}$	1 ... 5	A
Typical capacitance	(1 MHz, 1 V)	C_{typ}	0.6 ... 15	pF
Maximum clamping voltage		$V_{clamp,max}$	66 ... 290	V
Operating temperature	for 0402	T_{op}	−40/+85	°C
Operating temperature	for 0603	T_{op}	−55/+125	°C
Operating temperature	for 0603, automotive types	T_{op}	−55/+150	°C
Storage temperature	for 0402	LCT/UCT	−40/+125	°C
Storage temperature	for 0603	LCT/UCT	−55/+150	°C
Response time		t_{resp}	< 0.5	ns

General technical data for arrays

Maximum RMS operating voltage		$V_{RMS,max}$	10 ... 14	V
Maximum DC operating voltage		$V_{DC,max}$	12 ... 16	V
Contact discharge ESD capability	to IEC 61000-4-2	$V_{ESD,contact}$	8	kV
Air discharge ESD capability	to IEC 61000-4-2	$V_{ESD,air}$	15	kV
Maximum surge current	(8/20 μ s)	$I_{surge,max}$	1 ... 5	A
Typical capacitance for 4-fold array	(1 MHz, 1 V)	C_{typ}	4 x 3 ... 4 x 10	pF
Typical capacitance for MCV array	(1 MHz, 1 V)	C_{typ}	Matched capacitance 2 x 10 (ΔC between elements < 3%)	pF
Maximum clamping voltage		$V_{clamp,max}$	59 ... 350	V
Operating temperature	for 4-fold arrays	T_{op}	−40/+125	°C
Operating temperature	for MCV arrays	T_{op}	−55/+125	°C
Storage temperature	for 4-fold arrays	LCT/UCT	−40/+125	°C
Storage temperature	for MCV arrays	LCT/UCT	−55/+150	°C
Response time		t_{resp}	< 0.5	ns

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Electrical specifications and ordering codes for single chips

Maximum ratings ($T_{op,max}$)

Type	Ordering code	$V_{RMS,max}$ V	$V_{DC,max}$ V	$I_{surge,max}$ (8/20 μ s) A	W_{max} (ESD) ¹⁾ mJ	$T_{op,max}$ °C
Single chip						
CT0402S5ARFG	B72590T7050S160	4	5.5	-	-	+85
CT0603S5ARFG	B72500T7050S160	4	5.5	-	-	+125
CT0402S14AHSG	B72590T8140S160	14	16	2	30	+85
CT0402V150HSG	B72590T8151V060	14	16	1	30	+85
CT0402V150RFG	B72590T7151V060	14	16	-	-	+85
CT0402V275RFG	B72590T7271V060	14	16	-	-	+85
CT0402V90RFG	B72590T7900V060	14	16	-	-	+85
CT0603S14AHSG	B72500T8140S160	14	16	5	30	+125
CT0603S14AHSG_E	B72500E8140S160	14	16	5	30	+150 ²⁾
CT0603V150RFG	B72500T7151V060	14	16	-	-	+125
CT0603V150RFG_E	B72500E7151V060	14	16	-	-	+150 ²⁾
CT0603L25HSG	B72500T8250L060	25	32	5	50	+125
CT0603L25HSG_E	B72500E8250L060	25	32	5	50	+150 ²⁾

Characteristics ($T_A = 25\text{ °C}$)

Type	V_V (1 mA) V	ΔV_V %	$V_{clamp,max}$ V	I_{clamp} (8/20 μ s) A	C_{typ} (1 MHz, 1 V) pF	C_{max} (1 MHz, 1 V) pF
Single chip						
CT0402S5ARFG	255	± 15	-	-	0.6	1
CT0603S5ARFG	255	± 15	-	-	0.6	1
CT0402S14AHSG	28	± 20	66	1	10	15
CT0402V150HSG	150	± 35	290	1	2	3
CT0402V150RFG	150	± 35	-	-	2	3
CT0402V275RFG	275	± 30	-	-	1.5	2
CT0402V90RFG	105	± 15	-	-	2.2	3
CT0603S14AHSG	28	± 20	66	1	15	30
CT0603S14AHSG_E	28	± 20	66	1	15	30
CT0603V150RFG	150	± 35	-	-	3	5
CT0603V150RFG_E	150	± 35	290	1	3	5
CT0603L25HSG	61	± 15	120	1	10	15
CT0603L25HSG_E	61	± 15	120	1	10	15

Note:

Typ CT0603S14AHSG_E, CT0603V150RFG_E and CT0603L25HSG_E are qualified acc. to AEC-Q200 with $T_{op} = 150\text{ °C}$.

- 1) To IEC 61000-4-2, level 4
- 2) Qualified acc. to AEC-Q200

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Electrical specifications and ordering codes for arrays

Maximum ratings ($T_{op,max}$)

Type	Ordering code	$V_{RMS,max}$ V	$V_{DC,max}$ V	$I_{surge,max}$ (8/20 μ s) A	W_{max} (ESD) ¹⁾ mJ	$T_{op,max}$ °C
2-fold array						
CA05M2S10T100HG	B72812Q1120S160	10	12	5	-	+125 ²⁾
4-fold array						
CA05P4S14THSG	B72714A8140S160	14	16	2	30	+85
CA06P4V150THSG	B72724A8151V062	14	16	1	30	+85

Characteristics ($T_A = 25\text{ °C}$)

Type	V_V (1 mA) V	ΔV_V %	$V_{clamp,max}$ V	I_{clamp} (8/20 μ s) A	C_{typ} (1 MHz, 1 V) pF	C_{max} (1 MHz, 1 V) pF
2-fold array						
CA05M2S10T100HG	26	± 20	60	1	10	15
4-fold array						
CA05P4S14THSG	28	± 15	59	1	10	15
CA06P4V150THSG	150	± 20	350	1	3	5

Further characteristics

Type	Absolute capacitance deviation between array elements ³⁾ %	Maximum relative capacitance change %/ K	Dissipation factor $\tan \delta$ (@ 1 MHz, 1 V_{RMS} , 25 °C)	$P_{diss,max}$ mW	V_{LD} (300 ms) V	V_{jump} (60 s) V
2-fold array						
CA05M2S10T100HG	≤ 3	0.1	$< 50 \cdot 10^{-3}$	3	27	28

1) To IEC 61000-4-2, level 4

2) Qualified acc. to AEC-Q200

3) Absolute value of $(C_1 - C_2) / \text{minimum } \{C_1, C_2\}$, with C_1, C_2 denoting the two individual capacitances of the 2-fold array.

Multilayer varistors (MLVs)

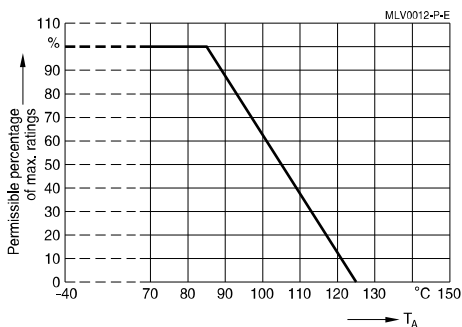
High-speed series

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Temperature derating

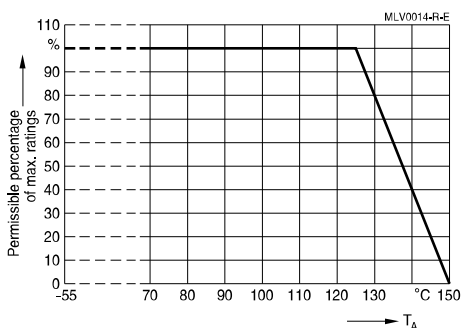
Climatic category:

–40/+85 °C for chip size 0402 single chip and 4-fold arrays



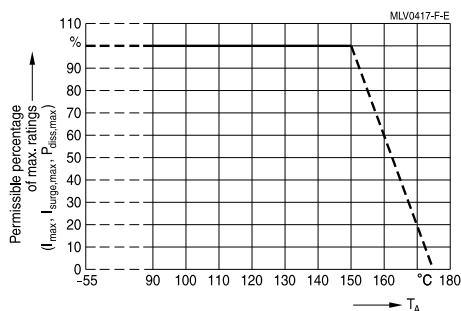
Climatic category:

–55/+125 °C for chip size 0603 single chip and MCV arrays



Climatic category:

–55/+150 °C for chip size 0603 single chip, only automotive types



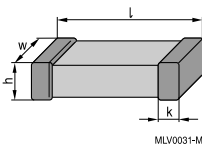
Multilayer varistors (MLVs)

High-speed series

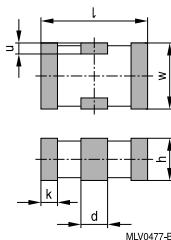
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Dimensional drawings

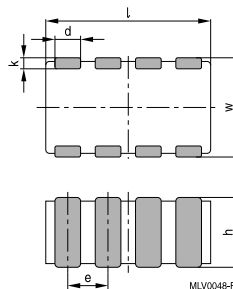
Single chip



2-fold MCV array



4-fold array



Dimensions in mm

Case size EIA / mm	l	w	h	d	e	k	u
0201 / 0603 Single chip	0.60 ±0.03	0.30 ±0.03	0.33 max.	-	-	0.15 ±0.05	-
0402 / 1005 Single chip	1.00 ±0.15	0.50 ±0.10	0.6 max.	-	-	0.10 ... 0.30	-
0508 / 1220 2-fold MCV array	2.00 ±0.20	1.25 ±0.15	0.9 max.	0.50 ±0.20	-	0.30 ±0.20	0.20 ±0.10
0508 / 1220 4-fold array	2.00 ±0.20	1.25 ±0.20	0.9 max.	0.30 ±0.10	0.50 ±0.10	0.20 +0.2/-0.1	-
0603 / 1608 Single chip	1.60 ±0.15	0.80 ±0.10	0.9 max.	-	-	0.10 ... 0.40	-
0612 / 1632 4-fold array	3.20 ±0.20	1.60 ±0.15	0.9 max.	0.40 ±0.15	0.80 ±0.15	0.20 ±0.10	-

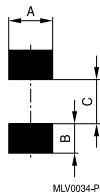
Multilayer varistors (MLVs)

High-speed series

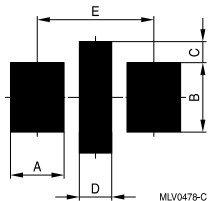
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Recommended solder pad layout

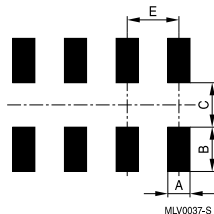
Single chip



2-fold MCV array



4-fold array



Dimensions in mm

Case size EIA / mm		A	B	C	D	E
0201 / 0603	Single chip	0.30	0.25	0.30	-	-
0402 / 1005	Single chip	0.60	0.60	0.50	-	-
0508 / 1220	2-fold MCV array	1.00	1.30	0.40	0.60	2.16
0508 / 1220	4-fold array	0.35	0.90	0.40	-	0.50
0603 / 1608	Single chip	1.00	1.00	1.00	-	-
0612 / 1632	4-fold array	0.50	0.70	1.20	-	0.76

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Delivery mode

EIA case size	Taping	Reel size mm	Packing unit pcs.	Type	Ordering code
2-fold array					
0508	Cardboard	180	4000	CA05M2S10T100HG	B72812Q1120S160
4-fold array					
0508	Cardboard	180	4000	CA05P4S14THSG	B72714A8140S160
0612	Blister	180	3000	CA06P4V150THSG	B72724A8151V062
Single chip					
0402	Cardboard	180	10000	CT0402S14AHSG	B72590T8140S160
0402	Cardboard	180	10000	CT0402S5ARFG	B72590T7050S160
0402	Cardboard	180	10000	CT0402V150HSG	B72590T8151V060
0402	Cardboard	180	10000	CT0402V150RFG	B72590T7151V060
0402	Cardboard	180	10000	CT0402V275RFG	B72590T7271V060
0402	Cardboard	180	10000	CT0402V90RFG	B72590T7900V060
0603	Cardboard	180	4000	CT0603L25HSG	B72500T8250L060
0603	Cardboard	180	4000	CT0603L25HSG_E	B72500E8250L060
0603	Cardboard	180	4000	CT0603S14AHSG	B72500T8140S160
0603	Cardboard	180	4000	CT0603S14AHSG_E	B72500E8140S160
0603	Cardboard	180	4000	CT0603S5ARFG	B72500T7050S160
0603	Cardboard	180	4000	CT0603V150RFG	B72500T7151V060
0603	Cardboard	180	4000	CT0603V150RFG_E	B72500E7151V060

Multilayer varistors (MLVs)

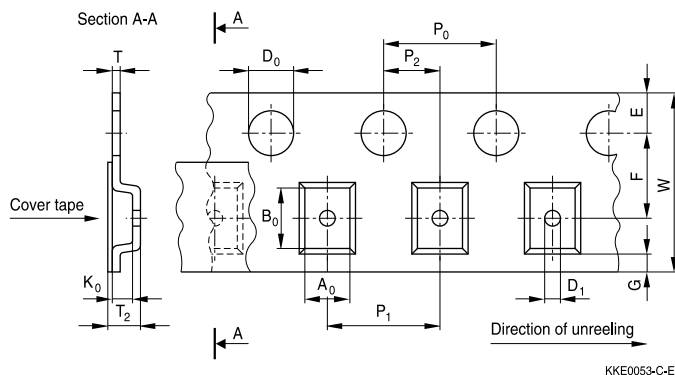
High-speed series

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Taping and packing

1 Taping and packing for SMD components

1.1 Blister tape (taping to IEC 60286-3)



Dimensions in mm

	8-mm tape					12-mm tape		Tolerance
	Case size (inch/mm)					Case size (inch/mm)		
			0508/ 1220	0612/ 1632	1012/ 2532			
	0603/ 1608	0506/ 1216	0805/ 2012	1206/ 3216	1210/ 3225	1812/ 4532	2220/ 5750	
A ₀	0.9 ±0.10	1.50	1.50	1.80	2.80	3.50	5.10	±0.20
B ₀	1.75 ±0.10	1.80	2.30	3.40	3.50	4.80	6.00	±0.20
K ₀	1.0	0.80	1.80			3.40		max.
T	0.30					0.30		max.
T ₂	1.3	1.20	2.50			3.90		max.
D ₀	1.50					1.50		+0.10/−0
D ₁	0.3					1.50		min.
P ₀	4.00					4.00		±0.10 ¹⁾
P ₂	2.00					2.00		±0.05
P ₁	4.00					8.00		±0.10
W	8.00					12.00		±0.30
E	1.75					1.75		±0.10
F	3.50					5.50		±0.05
G	0.75					0.75		min.

1) ≤±0.2 mm over 10 sprocket holes.

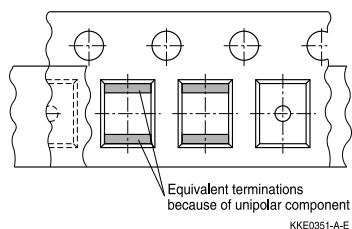
Multilayer varistors (MLVs)

High-speed series

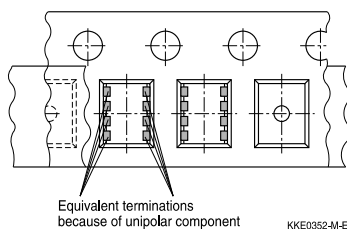
SMD

Part orientation in tape pocket for blister tape

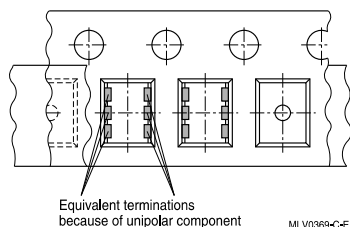
For discrete chip, EIA case sizes 0603, 0805, 1206, 1210, 1812 and 2220



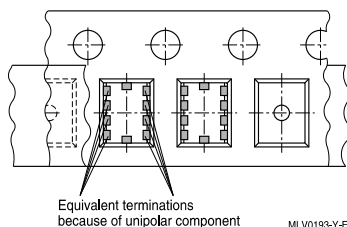
For array, EIA case size 0612



For arrays, EIA case sizes 0506 and 1012



For filter array, EIA case size 0508



Additional taping information

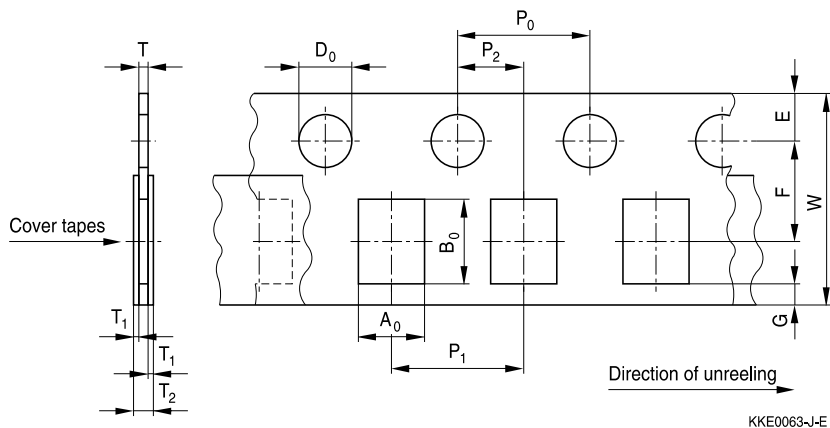
Reel material	Polystyrol (PS)
Tape material	Polystyrol (PS) or Polycarbonat (PC) or PVC
Tape break force	min. 10 N
Top cover tape strength	min. 10 N
Top cover tape peel force	0.1 to 1.0 N for 8-mm tape and 0.1 to 1.3 N for 12-mm tape at a peel speed of 300 mm/min
Tape peel angle	Angle between top cover tape and the direction of feed during peel off: 165° to 180°
Cavity play	Each part rests in the cavity so that the angle between the part and cavity center line is no more than 20°

Multilayer varistors (MLVs)

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1.2 Cardboard tape (taping to IEC 60286-3)



Dimensions in mm

	8-mm tape						Tolerance
	Case size (inch/mm)					Case size (inch/mm)	
	0201/0603	0402/1005	0405/1012	0603/1608	1003/2508	0508/1220	
A ₀	0.38 ±0.05	0.60	1.05	0.95	1.00	1.60	±0.20
B ₀	0.68 ±0.05	1.15	1.60	1.80	2.85	2.40	±0.20
T	0.42 ±0.02	0.60	0.75	0.95	0.95	0.95	max.
T ₂	0.4 min.	0.70	0.90	1.10	1.10	1.10	max.
D ₀	1.50 ±0.1	1.50				1.50	+0.10/−0
P ₀	4.00						±0.10 ²⁾
	2.00						±0.05
P ₁	2.00 ±0.05	2.00	4.00	4.00	4.00	4.00	±0.10
W	8.00						±0.30
E	1.75						±0.10
F	3.50						±0.05
G	0.75						min.

2) ≤0.2 mm over 10 sprocket holes.

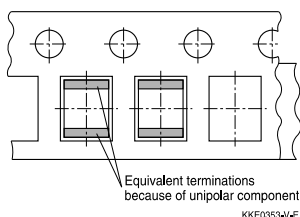
Multilayer varistors (MLVs)

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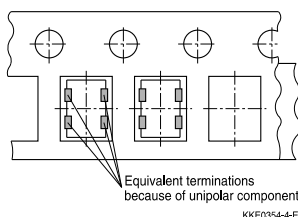
SMD

Part orientation in tape pocket for cardboard tape

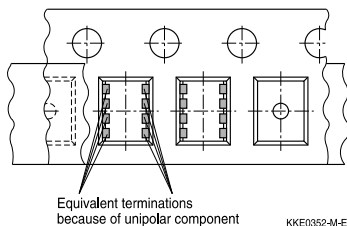
For discrete chip, EIA case sizes 0201, 0402, 0603 and 1003



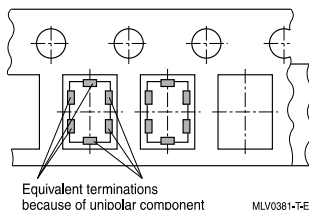
For array, EIA case size 0405



For array, EIA case size 0508



For filter array, EIA case size 0405



Additional taping information

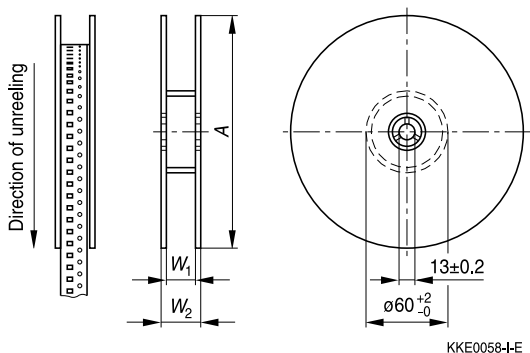
Reel material	Polystyrol (PS)
Tape material	Cardboard
Tape break force	min. 10 N
Top cover tape strength	min. 10 N
Top cover tape peel force	0.1 to 1.0 N at a peel speed of 300 mm/min
Tape peel angle	Angle between top cover tape and the direction of feed during peel off: 165° to 180°
Cavity play	Each part rests in the cavity so that the angle between the part and cavity center line is no more than 20°

Multilayer varistors (MLVs)

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1.3 Reel packing

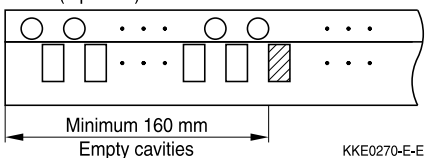


Dimensions in mm

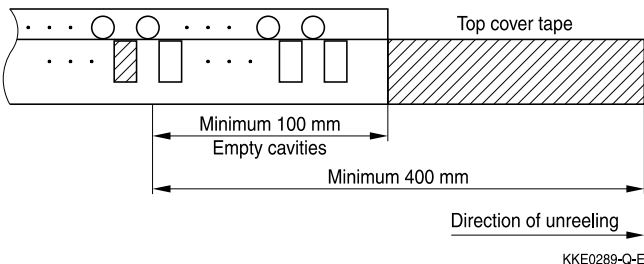
	8-mm tape		12-mm tape	
	180-mm reel	330-mm reel	180-mm reel	330-mm reel
A	180 $\pm 0/-3$	330 $\pm 0/-2.0$	180 $\pm 0/-3$	330 $\pm 0/-2.0$
W_1	8.4 $\pm 1.5/-0$	8.4 $\pm 1.5/-0$	12.4 $\pm 1.5/-0$	12.4 $\pm 1.5/-0$
W_2	14.4 max.	14.4 max.	18.4 max.	18.4 max.

Leader, trailer

Trailer (tape end)



Leader

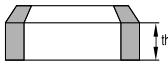
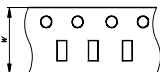
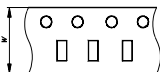


Multilayer varistors (MLVs)

High-speed series

SMD

1.4 Packing units for discrete chip and array chip

					
Case size inch/mm	Chip thickness th	Cardboard tape W	Blister tape W	Ø 180-mm reel pcs.	Ø 330-mm reel pcs.
0201/0603	0.33 mm	8 mm	—	15000	—
0402/1005	0.6 mm	8 mm	—	10000	50000
0405/1012	0.7 mm	8 mm	—	5000	—
0506/1216	0.5 mm	—	8 mm	4000	—
0508/1220	0.9 mm	8 mm	8 mm	4000	—
0603/1608	0.9 mm	8 mm	8 mm	4000	16000
0612/1632	0.7 mm	—	8 mm	3000	—
0805/2012	0.7 mm	—	8 mm	3000	—
	0.9 mm	—	8 mm	3000	12000
	1.3 mm	—	8 mm	3000	12000
1003/2508	0.9 mm	8 mm	—	4000	—
1012/2532	1.0 mm	—	8 mm	2000	—
1206/3216	0.9 mm	—	8 mm	3000	—
	1.3 mm	—	8 mm	3000	12000
	1.4 mm	—	8 mm	2000	8000
	1.6 mm	—	8 mm	2000	8000
1210/3225	0.9 mm	—	8 mm	3000	—
	1.3 mm	—	8 mm	3000	12000
	1.4 mm	—	8 mm	2000	8000
	1.6 mm	—	8 mm	2000	8000
1812/4532	1.3 mm	—	12 mm	1500	—
	1.4 mm	—	12 mm	1000	—
	1.6 mm	—	12 mm	1000	4000
	2.0 mm	—	12 mm	—	3000
	2.3 mm	—	12 mm	—	3000
2220/5750	1.3 mm	—	12 mm	1500	—
	1.4 mm	—	12 mm	1000	—
	1.6 mm	—	12 mm	1000	—
	2.0 mm	—	12 mm	—	3000
	2.3 mm	—	12 mm	—	3000
	2.7 mm	—	12 mm	600	—
	3.0 mm	—	12 mm	600	—

Multilayer varistors (MLVs)**High-speed series****SMD****2 Delivery mode for leaded SHCV varistors**

Standard delivery mode for SHCV types is bulk. Alternative taping modes (AMMO pack or taped on reel) are available upon request.

Packing units for:

Type	Pieces
SR6	2000
SR1 / SR2	1000

For types not listed in this data book please contact EPCOS.

Multilayer varistors (MLVs)

High-speed series

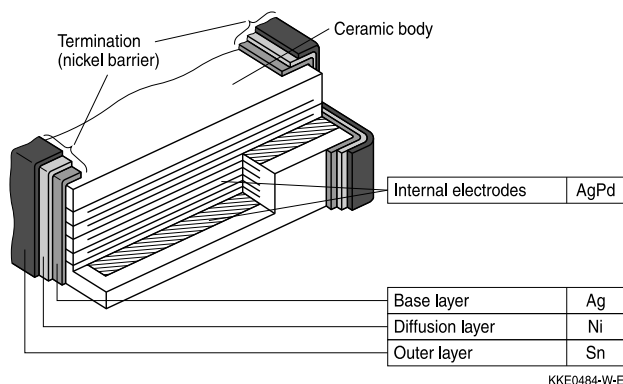
SMD

Soldering directions

1 Terminations

1.1 Nickel barrier termination

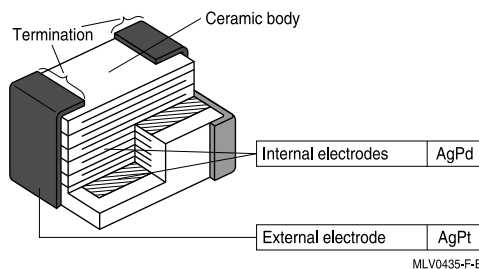
The nickel barrier layer of the silver/nickel/tin termination prevents leaching of the silver base metallization layer. This allows great flexibility in the selection of soldering parameters. The tin prevents the nickel layer from oxidizing and thus ensures better wetting by the solder. The nickel barrier termination is suitable for all commonly-used soldering methods, including lead-free soldering.



Multilayer CTVS: Structure of nickel barrier termination

1.2 Silver-platinum termination

Silver-platinum terminations are mainly used for the large EIA case sizes 1812 and 2220. The silver-platinum termination is approved for reflow soldering, SnPb soldering and lead-free soldering with a silver containing solder paste. In case of SnPb soldering, a solder paste Sn62Pb36Ag2 is recommended. For lead-free reflow soldering, a solder paste SAC, e.g. Sn95.5Ag3.8Cu0.7, is recommended.



Multilayer varistor: Structure of silver-platinum termination

Multilayer varistors (MLVs)

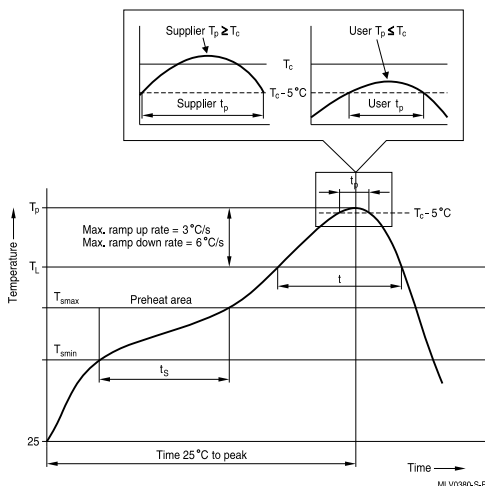
High-speed series

SMD

2 Recommended soldering temperature profiles

2.1 Reflow soldering temperature profile

Recommended temperature characteristic for reflow soldering following JEDEC J-STD-020D



Profile feature		Sn-Pb eutectic assembly	Pb-free assembly
Preheat and soak			
- Temperature min	T_{smin}	100 °C	150 °C
- Temperature max	T_{smax}	150 °C	200 °C
- Time	t_{smin} to t_{smax}	60 ... 120 s	60 ... 180 s
Average ramp-up rate	T_{smax} to T_p	3 °C/ s max.	3 °C/ s max.
Liquidous temperature	T_L	183 °C	217 °C
Time at liquidous	t_L	60 ... 150 s	60 ... 150 s
Peak package body temperature	$T_p^{1)}$	220 °C ... 235 °C ²⁾	245 °C ... 260 °C ²⁾
Time (t_p) ³⁾ within 5 °C of specified classification temperature (T_c)		20 s ³⁾	30 s ³⁾
Average ramp-down rate	T_p to T_{smax}	6 °C/ s max.	6 °C/ s max.
Time 25 °C to peak temperature		maximum 6 min	maximum 8 min

1) Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

2) Depending on package thickness. For details please refer to JEDEC J-STD-020D.

3) Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Note: All temperatures refer to topside of the package, measured on the package body surface.
Number of reflow cycles: 3

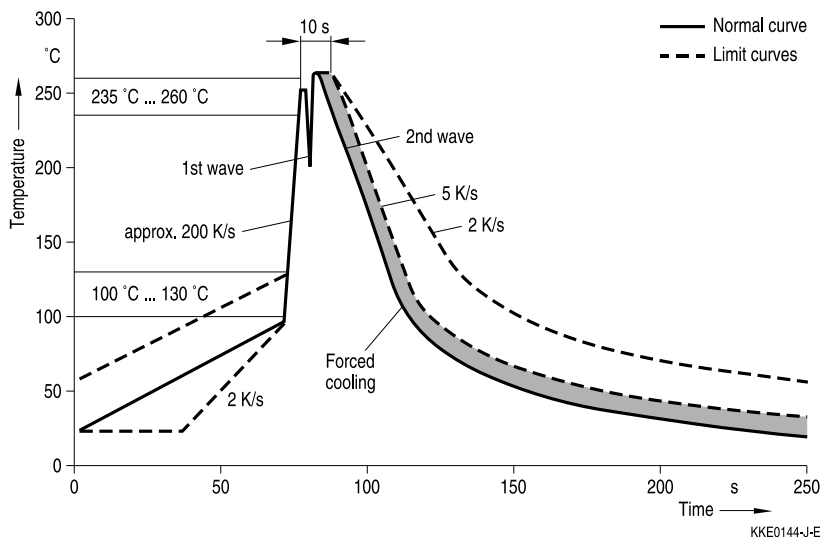
Multilayer varistors (MLVs)

High-speed series

SMD

2.2 Wave soldering temperature profile

Temperature characteristics at component terminal with dual-wave soldering



2.3 Lead-free soldering processes

EPCOS multilayer CTVS with AgNiSn termination are designed for the requirements of lead-free soldering processes only.

Soldering temperature profiles to JEDEC J-STD-020D, IEC 60068-2-58 and ZVEI recommendations.

3 Recommended soldering methods - type-specific releases by EPCOS

3.1 Overview

Type	EIA case size	Reflow soldering		Wave soldering	
		SnPb	Lead-free	SnPb	Lead-free
CT... / CD...	0201/ 0402	Approved	Approved	No	No
CT... / CD...	0603 ... 2220	Approved	Approved	Approved	Approved
CN...K2	1812, 2220	Approved	Approved	No	No
Arrays	0405 ... 1012	Approved	Approved	No	No
ESD/EMI filters	0405, 0508	Approved	Approved	No	No
SHCV	-	No	No	Approved	Approved

Multilayer varistors (MLVs)

High-speed series

SMD

3.2 Nickel barrier and AgPt terminated multilayer MLVs

All EPCOS MLVs with nickel barrier and AgPt termination are suitable and fully qualified for lead-free soldering. The nickel barrier layer is 100% matte tin-plated.

3.3 Silver-platinum terminated MLVs

The silver-platinum termination is approved for reflow soldering, SnPb soldering and lead-free with a silver containing solder paste. In case of SnPb soldering, a solder paste Sn62Pb36Ag2 is recommended. For lead-free reflow soldering, a solder paste SAC, e.g. Sn95.5Ag3.8Cu0.7, is recommended.

3.4 Tinned iron wire

All EPCOS SHCV types with tinned termination are approved for lead-free and SnPb soldering.

4 Solder joint profiles / solder quantity

4.1 Nickel barrier termination

If the meniscus height is too low, that means the solder quantity is too low, the solder joint may break, i.e. the component becomes detached from the joint. This problem is sometimes interpreted as leaching of the external terminations.

If the solder meniscus is too high, i.e. the solder quantity is too large, the vise effect may occur. As the solder cools down, the solder contracts in the direction of the component. If there is too much solder on the component, it has no leeway to evade the stress and may break, as in a vise.

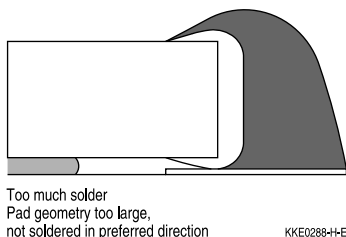
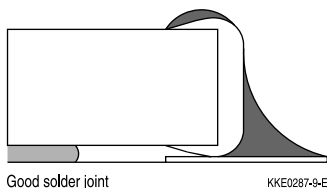
The figures below show good and poor solder joints for dual-wave and infrared soldering.

Multilayer varistors (MLVs)

High-speed series

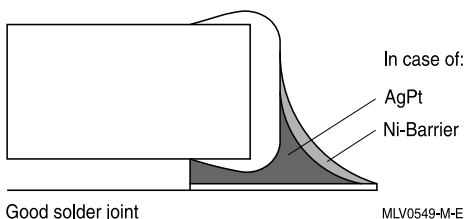
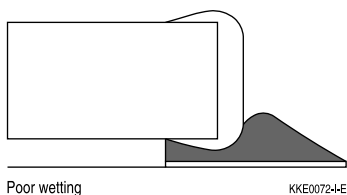
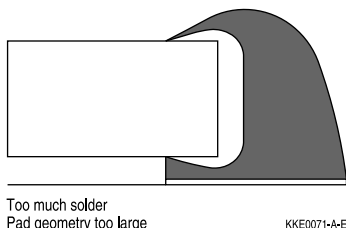
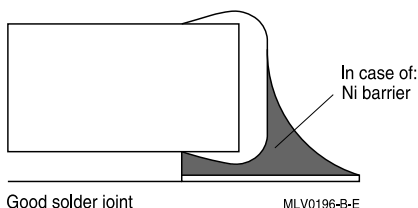
SMD

4.1.1 Solder joint profiles for nickel barrier termination - dual-wave soldering



Good and poor solder joints caused by amount of solder in dual-wave soldering.

4.1.2 Solder joint profiles for nickel barrier termination / silver-platinum termination - reflow soldering



Good and poor solder joints caused by amount of solder in reflow soldering.

Multilayer varistors (MLVs)

High-speed series

SMD

5 Solderability tests

Test	Standard	Test conditions Sn-Pb soldering	Test conditions Pb-free soldering	Criteria/ test results
Wettability	IEC 60068-2-58	Immersion in 60/40 SnPb solder using non-activated flux at 215 ± 3 °C for 3 ± 0.3 s	Immersion in Sn96.5Ag3.0Cu0.5 solder using non- or low activated flux at 245 ± 5 °C for 3 ± 0.3 s	Covering of 95% of end termination, checked by visual inspection
Leaching resistance	IEC 60068-2-58	Immersion in 60/40 SnPb solder using mildly activated flux without preheating at 260 ± 5 °C for 10 ± 1 s	Immersion in Sn96.5Ag3.0Cu0.5 solder using non- or low activated flux without preheating at 255 ± 5 °C for 10 ± 1 s	No leaching of contacts
Thermal shock (solder shock)		Dip soldering at 300 °C/5 s	Dip soldering at 300 °C/5 s	No deterioration of electrical parameters. Capacitance change: $ \Delta C/C_0 \leq 15\%$
Tests of resistance to soldering heat for SMDs	IEC 60068-2-58	Immersion in 60/40 SnPb for 10 s at 260 °C	Immersion in Sn96.5Ag3.0Cu0.5 for 10 s at 260 °C	Change of varistor voltage: $ \Delta V/V (1 \text{ mA}) \leq 5\%$
Tests of resistance to soldering heat for radial leaded components (SHCV)	IEC 60068-2-20	Immersion of leads in 60/40 SnPb for 10 s at 260 °C	Immersion of leads in Sn96.5Ag3.0Cu0.5 for 10 s at 260 °C	Change of varistor voltage: $ \Delta V/V (1 \text{ mA}) \leq 5\%$ Change of capacitance X7R: $\leq -5/+10\%$

Multilayer varistors (MLVs)

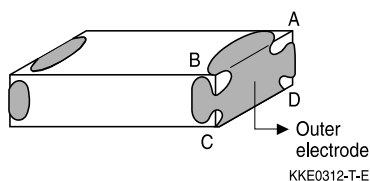
High-speed series

SMD

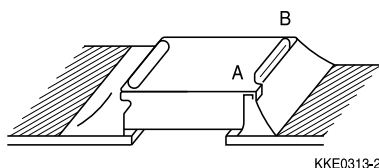
Note:

Leaching of the termination

Effective area at the termination might be lost if the soldering temperature and/or immersion time are not kept within the recommended conditions. Leaching of the outer electrode should not exceed 25% of the chip end area (full length of the edge A-B-C-D) and 25% of the length A-B, shown below as mounted on substrate.



As a single chip



As mounted on substrate

6 Notes for proper soldering

6.1 Preheating and cooling

■ According to JEDEC J-STD-020D. Please refer to section 2 of this chapter.

6.2 Repair/ rework

Manual soldering with a soldering iron must be avoided, hot-air methods are recommended for rework purposes.

6.3 Cleaning

All environmentally compatible agents are suitable for cleaning. Select the appropriate cleaning solution according to the type of flux used. The temperature difference between the components and cleaning liquid must not be greater than 100 °C. Ultrasonic cleaning should be carried out with the utmost caution. Too high ultrasonic power can impair the adhesive strength of the metallized surfaces.

6.4 Solder paste printing (reflow soldering)

An excessive application of solder paste results in too high a solder fillet, thus making the chip more susceptible to mechanical and thermal stress. Too little solder paste reduces the adhesive strength on the outer electrodes and thus weakens the bonding to the PCB. The solder should be applied smoothly to the end surface.

Multilayer varistors (MLVs)

High-speed series

SMD

6.5 Selection of flux

Used flux should have less than or equal to 0.1 wt % of halogenated content, since flux residue after soldering could lead to corrosion of the termination and/or increased leakage current on the surface of the component. Strong acidic flux must not be used. The amount of flux applied should be carefully controlled, since an excess may generate flux gas, which in turn is detrimental to solderability.

6.6 Storage of CTVSs

Solderability is guaranteed for one year from date of delivery for multilayer varistors, CeraDiodes and ESD/EMI filters (half a year for chips with AgPt terminations) and two years for SHCV components, provided that components are stored in their original packages.

Storage temperature: $-25\text{ }^{\circ}\text{C}$ to $+45\text{ }^{\circ}\text{C}$

Relative humidity: $\leq 75\%$ annual average, $\leq 95\%$ on 30 days a year

The solderability of the external electrodes may deteriorate if SMDs and leaded components are stored where they are exposed to high humidity, dust or harmful gas (hydrogen chloride, sulfurous acid gas or hydrogen sulfide).

Do not store SMDs and leaded components where they are exposed to heat or direct sunlight. Otherwise the packing material may be deformed or SMDs/ leaded components may stick together, causing problems during mounting.

After opening the factory seals, such as polyvinyl-sealed packages, it is recommended to use the SMDs or leaded components as soon as possible.

Solder CTVS components after shipment from EPCOS within the time specified:

CTVS with Ni barrier termination: 12 months

CTVS with AgPt termination: 6 months

SHCV (leaded components): 24 months

6.7 Placement of components on circuit board

Especially in the case of dual-wave soldering, it is of advantage to place the components on the board before soldering in that way that their two terminals do not enter the solder bath at different times.

Ideally, both terminals should be wetted simultaneously.

Multilayer varistors (MLVs)

High-speed series

SMD

6.8 Soldering cautions

- An excessively long soldering time or high soldering temperature results in leaching of the outer electrodes, causing poor adhesion and a change of electrical properties of the varistor due to the loss of contact between electrodes and termination.
- Wave soldering must not be applied for MLVs designated for reflow soldering only (see table "Overview", section 3.1).
- Keep the recommended down-cooling rate.

6.9 Standards

CECC 00802

IEC 60068-2-58

IEC 60068-2-20

JEDEC J-STD-020D

Multilayer varistors (MLVs)

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Symbols and terms

For ceramic transient voltage suppressors (CTVS)

Symbol	Term
$C_{\text{line,max}}$	Maximum capacitance per line
$C_{\text{line,min}}$	Minimum capacitance per line
$C_{\text{line,typ}}$	Typical capacitance per line
C_{max}	Maximum capacitance
C_{min}	Minimum capacitance
C_{nom}	Nominal capacitance
ΔC_{nom}	Tolerance of nominal capacitance
C_{typ}	Typical capacitance
$f_{\text{cut-off,max}}$	Maximum cut-off frequency
$f_{\text{cut-off,min}}$	Minimum cut-off frequency
$f_{\text{cut-off,typ}}$	Typical cut-off frequency
$f_{\text{res,typ}}$	Typical resonance frequency
I	Current
I_{clamp}	Clamping current
I_{leak}	Leakage current
$I_{\text{leak,max}}$	Maximum leakage current
$I_{\text{leak,typ}}$	Typical leakage current
I_{PP}	Peak pulse current
$I_{\text{surge,max}}$	Maximum surge current (also termed peak current)
LCT	Lower category temperature
L_{typ}	Typical inductance
$P_{\text{diss,max}}$	Maximum power dissipation
P_{PP}	Peak pulse power
R_{ins}	Insulation resistance
R_{min}	Minimum resistance
R_{S}	Resistance per line
$R_{\text{S,typ}}$	Typical resistance per line
T_{A}	Ambient temperature
T_{op}	Operating temperature
$T_{\text{op,max}}$	Maximum operating temperature
T_{stg}	Storage temperature

Multilayer varistors (MLVs)

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SMD

Symbol	Term
t_r	Duration of equivalent rectangular wave
t_{resp}	Response time
$t_{resp,max}$	Maximum response time
UCT	Upper category temperature
V	Voltage
$V_{BR,min}$	Minimum breakdown voltage
$V_{clamp,max}$	Maximum clamping voltage
$V_{DC,max}$	Maximum DC operating voltage (also termed working voltage)
$V_{ESD,air}$	Air discharge ESD capability
$V_{ESD,contact}$	Contact discharge ESD capability
V_{jump}	Maximum jump-start voltage
$V_{RMS,max}$	Maximum AC operating voltage, root-mean-square value
V_V	Varistor voltage (also termed breakdown voltage)
V_{LD}	Maximum load dump voltage
V_{leak}	Measurement voltage for leakage current
$V_{V,min}$	Minimum varistor voltage
$V_{V,max}$	Maximum varistor voltage
ΔV_V	Tolerance of varistor voltage
W_{LD}	Maximum load dump energy
W_{max}	Maximum energy absorption (also termed transient energy)
α_{typ}	Typical insertion loss
$\tan \delta$	Dissipation factor
e	Lead spacing
$\ll * \gg$	Maximum possible application conditions

All dimensions are given in mm.

The commas used in numerical values denote decimal points.

Multilayer varistors (MLVs)

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SMD

For CeraDiodes

CeraDiode	Semiconductor diode	
$C_{\max}$		Maximum capacitance
C_{typ}		Typical capacitance
I_{BR}	$I_{\text{R}}, I_{\text{T}}$	(Reverse) current @ breakdown voltage
I_{leak}	I_{RM}	(Reverse) leakage current
I_{PP}	$I_{\text{P}}, I_{\text{PP}}$	Current @ clamping voltage; peak pulse current
P_{PP}	P_{PP}	Peak pulse power
T_{op}		Operating temperature
T_{stg}		Storage temperature
V_{BR}	V_{BR}	(Reverse) breakdown voltage
$V_{\text{BR,min}}$		Minimum breakdown voltage
V_{clamp}	$V_{\text{cl}}, V_{\text{C}}$	Clamping voltage
$V_{\text{clamp,max}}$		Maximum clamping voltage
V_{DC}	$V_{\text{RM}}, V_{\text{RWM}}, V_{\text{WM}}, V_{\text{DC}}$	(Reverse) stand-off voltage, working voltage, operating voltage
$V_{\text{DC,max}}$		Maximum DC operating voltage
$V_{\text{ESD,air}}$		Air discharge ESD capability
$V_{\text{ESD,contact}}$		Contact discharge ESD capability
V_{leak}	$V_{\text{RM}}, V_{\text{RWM}}, V_{\text{WM}}, V_{\text{DC}}$	(Reverse) voltage @ leakage current
- *)	I_{F}	Current @ forward voltage
- *)	$I_{\text{RM}}, I_{\text{RM,max}} @ V_{\text{RM}}$	(Reverse) current @ maximum reverse stand-off voltage, working voltage, operating voltage
- *)	V_{F}	Forward voltage

*) Not applicable due to bidirectional characteristics of CeraDiodes.

Multilayer varistors (MLVs)

High-speed series

SMD

Cautions and warnings

General

Some parts of this publication contain statements about the suitability of our ceramic transient voltage suppressor (CTVS) components (multilayer varistors (MLVs)), CeraDiodes, ESD/EMI filters, leaded transient voltage/ RFI suppressors (SHCV types)) for certain areas of application, including recommendations about incorporation/design-in of these products into customer applications. The statements are based on our knowledge of typical requirements often made of our CTVS devices in the particular areas. We nevertheless expressly point out that such statements cannot be regarded as binding statements about the suitability of our CTVS components for a particular customer application. As a rule, EPCOS is either unfamiliar with individual customer applications or less familiar with them than the customers themselves. For these reasons, it is always incumbent on the customer to check and decide whether the CTVS devices with the properties described in the product specification are suitable for use in a particular customer application.

- Do not use EPCOS CTVS components for purposes not identified in our specifications, application notes and data books.
- Ensure the suitability of a CTVS in particular by testing it for reliability during design-in. Always evaluate a CTVS component under worst-case conditions.
- Pay special attention to the reliability of CTVS devices intended for use in safety-critical applications (e.g. medical equipment, automotive, spacecraft, nuclear power plant).

Design notes

- Always connect a CTVS in parallel with the electronic circuit to be protected.
- Consider maximum rated power dissipation if a CTVS has insufficient time to cool down between a number of pulses occurring within a specified isolated time period. Ensure that electrical characteristics do not degrade.
- Consider derating at higher operating temperatures. Choose the highest voltage class compatible with derating at higher temperatures.
- Surge currents beyond specified values will puncture a CTVS. In extreme cases a CTVS will burst.
- If steep surge current edges are to be expected, make sure your design is as low-inductance as possible.
- In some cases the malfunctioning of passive electronic components or failure before the end of their service life cannot be completely ruled out in the current state of the art, even if they are operated as specified. In applications requiring a very high level of operational safety and especially when the malfunction or failure of a passive electronic component could endanger human life or health (e.g. in accident prevention, life-saving systems, or automotive battery line applications such as clamp 30), ensure by suitable design of the application or other measures (e.g. installation of protective circuitry or redundancy) that no injury or damage is sustained by third parties in the event of such a malfunction or failure. Only use CTVS components from the automotive series in safety-relevant applications.

Multilayer varistors (MLVs)

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- Specified values only apply to CTVS components that have not been subject to prior electrical, mechanical or thermal damage. The use of CTVS devices in line-to-ground applications is therefore not advisable, and it is only allowed together with safety countermeasures like thermal fuses.

Storage

- Only store CTVS in their original packaging. Do not open the package prior to processing.
- Storage conditions in original packaging: temperature -25 to $+45^{\circ}\text{C}$, relative humidity $\leq 75\%$ annual average, maximum 95% , dew precipitation is inadmissible.
- Do not store CTVS devices where they are exposed to heat or direct sunlight. Otherwise the packaging material may be deformed or CTVS may stick together, causing problems during mounting.
- Avoid contamination of the CTVS surface during storage, handling and processing.
- Avoid storing CTVS devices in harmful environments where they are exposed to corrosive gases for example (SO_x , Cl).
- Use CTVS as soon as possible after opening factory seals such as polyvinyl-sealed packages.
- Solder CTVS components after shipment from EPCOS within the time specified:
 - CTVS with Ni barrier termination, 12 months
 - CTVS with AgPt termination, 6 months
 - SHCV, 24 months

Handling

- Do not drop CTVS components and allow them to be chipped.
- Do not touch CTVS with your bare hands - gloves are recommended.
- Avoid contamination of the CTVS surface during handling.
- Washing processes may damage the product due to the possible static or cyclic mechanical loads (e.g. ultrasonic cleaning). They may cause cracks to develop on the product and its parts, which might lead to reduced reliability or lifetime.

Mounting

- When CTVS devices are encapsulated with sealing material or overmolded with plastic material, electrical characteristics might be degraded and the life time reduced.
- Make sure an electrode is not scratched before, during or after the mounting process.
- Make sure contacts and housings used for assembly with CTVS components are clean before mounting.
- The surface temperature of an operating CTVS can be higher. Ensure that adjacent components are placed at a sufficient distance from a CTVS to allow proper cooling.
- Avoid contamination of the CTVS surface during processing.

Multilayer varistors (MLVs)

High-speed series

SMD

Soldering

- Complete removal of flux is recommended to avoid surface contamination that can result in an instable and/or high leakage current.
- Use resin-type or non-activated flux.
- Bear in mind that insufficient preheating may cause ceramic cracks.
- Rapid cooling by dipping in solvent is not recommended, otherwise a component may crack.

Operation

- Use CTVS only within the specified operating temperature range.
- Use CTVS only within specified voltage and current ranges.
- Environmental conditions must not harm a CTVS. Only use them in normal atmospheric conditions. Reducing the atmosphere (e.g. hydrogen or nitrogen atmosphere) is prohibited.
- Prevent a CTVS from contacting liquids and solvents. Make sure that no water enters a CTVS (e.g. through plug terminals).
- Avoid dewing and condensation.
- EPCOS CTVS components are mainly designed for encased applications. Under all circumstances avoid exposure to:
 - direct sunlight
 - rain or condensation
 - steam, saline spray
 - corrosive gases
 - atmosphere with reduced oxygen content
- EPCOS CTVS devices are not suitable for switching applications or voltage stabilization where static power dissipation is required.

This listing does not claim to be complete, but merely reflects the experience of EPCOS AG.

Display of ordering codes for EPCOS products

The ordering code for one and the same EPCOS product can be represented differently in data sheets, data books, other publications, on the EPCOS website, or in order-related documents such as shipping notes, order confirmations and product labels. **The varying representations of the ordering codes are due to different processes employed and do not affect the specifications of the respective products.** Detailed information can be found on the Internet under www.epcos.com/orderingcodes

Important notes

The following applies to all products named in this publication:

1. Some parts of this publication contain **statements about the suitability of our products for certain areas of application**. These statements are based on our knowledge of typical requirements that are often placed on our products in the areas of application concerned. We nevertheless expressly point out **that such statements cannot be regarded as binding statements about the suitability of our products for a particular customer application**. As a rule, EPCOS is either unfamiliar with individual customer applications or less familiar with them than the customers themselves. For these reasons, it is always ultimately incumbent on the customer to check and decide whether an EPCOS product with the properties described in the product specification is suitable for use in a particular customer application.
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