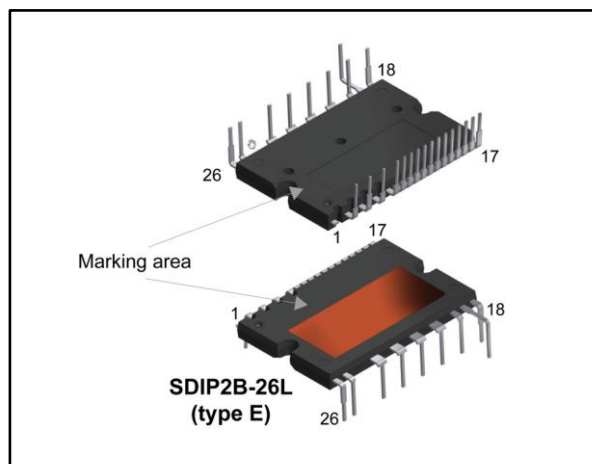


SLLIMM™ - 2nd series IPM, 3-phase inverter, 12 A, 600 V short-circuit rugged IGBT

Datasheet - preliminary data



Features

- IPM 12 A, 600 V 3-phase IGBT inverter bridge including 2 control ICs for gate driving and freewheeling diodes
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Internal bootstrap diode
- Undervoltage lockout of gate drivers
- Smart shutdown function
- Short-circuit protection
- Shutdown input/fault output
- Separate open emitter outputs
- Built-in temperature sensor
- Comparator for fault protection
- Short-circuit rugged TFS IGBTs
- Very fast, soft recovery diodes
- 85 kΩ NTC UL 1434 CA 4 recognized
- Fully isolated package
- Isolation rating of 1500 Vrms/min

Applications

- 3-phase inverters for motor drives
- Home appliances such as washing machines, refrigerators, air conditioners and sewing machines

Description

This second series of SLLIMM (small low-loss intelligent molded module) provides a compact, high performance AC motor drive in a simple, rugged design. It combines new ST proprietary control ICs (one LS and one HS driver) with an improved short-circuit rugged trench gate field-stop (TFS) IGBT, making it ideal for 3-phase inverter systems such as home appliances and air conditioners. SLLIMM™ is a trademark of STMicroelectronics.

Table 1: Device summary

Order code	Marking	Package	Packing
STGIB8CH60TS-E	GIB8CH60TS-E	SDIP2B-26L	Tube

Contents

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1 Internal schematic and pin description

Figure 1: Internal schematic diagram and pin configuration

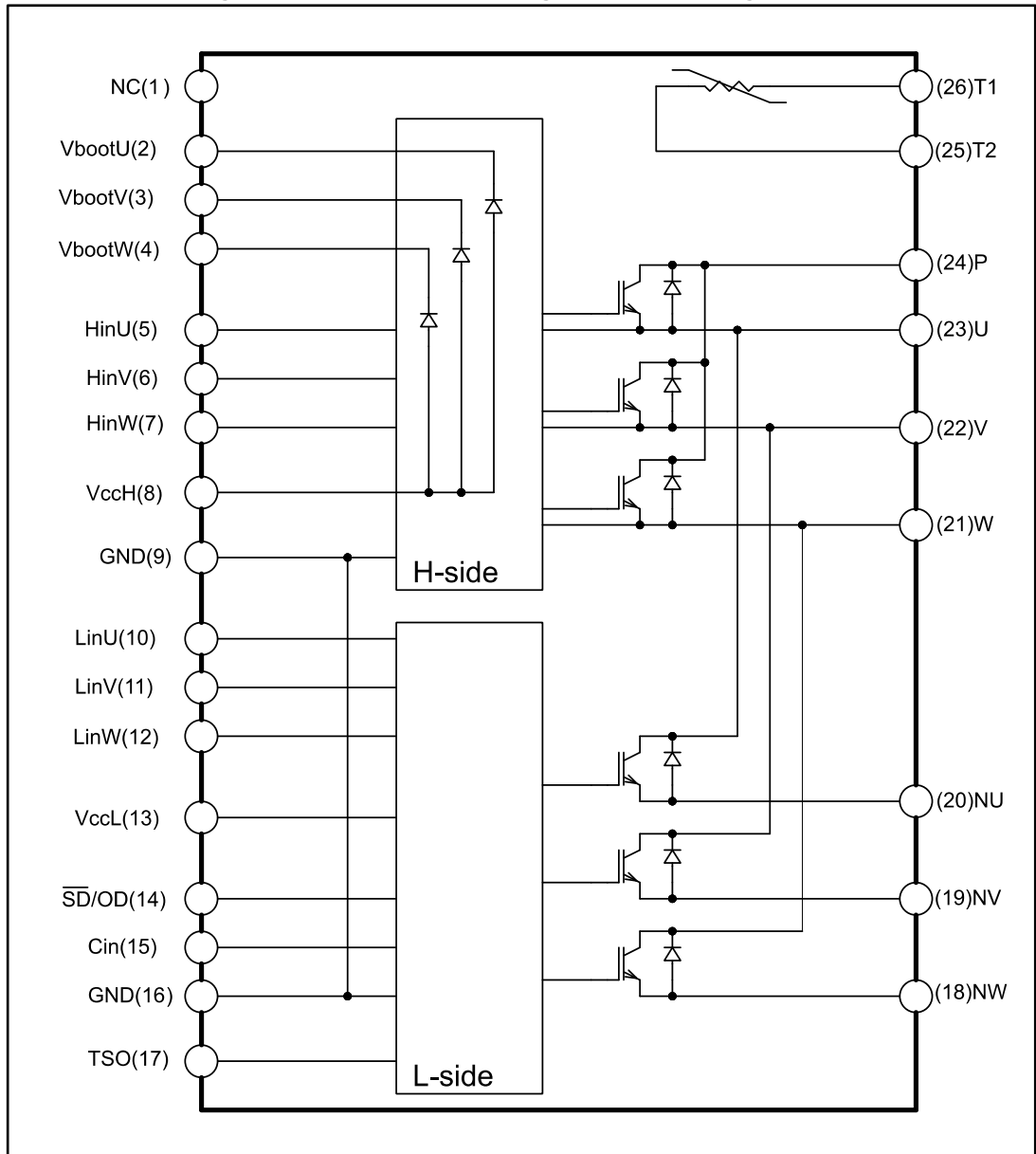


Table 2: Pin description

Pin	Symbol	Description
1	NC	
2	VBOOTu	Bootstrap voltage for U phase
3	VBOOTv	Bootstrap voltage for V phase
4	VBOOTw	Bootstrap voltage for W phase
5	HINu	High-side logic input for U phase
6	HINv	High-side logic input for V phase
7	HINw	High-side logic input for W phase
8	VCCH	High-side low voltage power supply
9	GND	Ground
10	LINu	Low-side logic input for U phase
11	LINv	Low-side logic input for V phase
12	LINw	Low-side logic input for W phase
13	VCCL	Low-side low voltage power supply
14	\overline{SD} / OD	Shutdown logic input (active low) / open-drain (comparator output)
15	CIN	Comparator input
16	GND	Ground
17	TSO	Temperature sensor output
18	NW	Negative DC input for W phase
19	NV	Negative DC input for V phase
20	NU	Negative DC input for U phase
21	W	W phase output
22	V	V phase output
23	U	U phase output
24	P	Positive DC input
25	T2	NTC thermistor terminal 2
26	T1	NTC thermistor terminal 1

2 Absolute maximum ratings

Table 3: Absolute maximum ratings ($T_J = 25\text{ °C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{PN}	Supply voltage between P -N _U , -N _V , -N _W	450	V
$V_{PN(surge)}$	Supply voltage surge between P -N _U , -N _V , -N _W	500	V
V_{CES}	Collector-emitter voltage each IGBT	600	V
$\pm I_C$	Continuous collector current each IGBT ($T_C = 25\text{ °C}$)	12	A
	Continuous collector current each IGBT ($T_C = 80\text{ °C}$)	8	
$\pm I_{CP}$	Peak collector current each IGBT (less than 1ms)	24	A
P_{TOT}	Total dissipation at $T_C=25\text{ °C}$ each IGBT	50	W
t_{scw}	Short circuit withstand time, $V_{CE} = 300V$, $T_J = 125\text{ °C}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN} = 0\text{ to }5\text{ V}$	5	μs

Table 4: Control parts

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage between $V_{CCH-GND}$, $V_{CCL-GND}$	-0.3	20	V
V_{BOOT}	Bootstrap voltage	-0.3	619	V
V_{OUT}	Output voltage between U, V, W and GND	$V_{BOOT} - 21$	$V_{BOOT} + 0.3$	V
V_{CIN}	Comparator input voltage	-0.3	20	V
V_{IN}	Logic input voltage applied between HIN _x , LIN _x and GND	-0.3	15	V
$V_{\overline{SD/OD}}$	Open drain voltage	-0.3	7	V
$I_{\overline{SD/OD}}$	Open drain sink current		10	mA
V_{TSO}	Temperature sensor output voltage	-0.3	5.5	V
I_{TSO}	Temperature sensor output current		7	mA

Table 5: Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage, $t = 60\text{ sec.}$)	1500	V _{rms}
T_J	Power chips operating junction temperature	-40 to 175	$^{\circ}\text{C}$
T_C	Module case operation temperature	-40 to 125	$^{\circ}\text{C}$

Table 6: Thermal data

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Thermal resistance junction-case single IGBT	3	$^{\circ}\text{C/W}$
	Thermal resistance junction-case single diode	6	

3 Electrical characteristics

($T_j = 25^\circ\text{C}$ unless otherwise noted).

3.1 Inverter part

Table 7: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector-cut off current	$V_{CE} = 600\text{ V}$, $V_{CC} = V_{boot} = 15\text{ V}$	-		100	μA
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0\text{ to }5\text{ V}$, $I_C = 8\text{ A}$	-	1.68	2.18	V
		$V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0\text{ to }5\text{ V}$, $I_C = 12\text{ A}$	-	1.91		
V_F	Diode forward voltage	$V_{IN}^{(1)} = 0$, $I_C = 8\text{ A}$	-	1.55	2.1	V
		$V_{IN}^{(1)} = 0$, $I_C = 12\text{ A}$	-	1.7		V

Notes:

⁽¹⁾Applied between HINx, LINx and GND for x = U, V, W.

Table 8: Inductive load switching time and energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{on}^{(1)}$	Turn-on time	$V_{DD} = 300\text{ V}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(2)} = 0\text{ to }5\text{ V}$, $I_C = 8\text{ A}$	-	280	-	ns
$t_{c(on)}^{(1)}$	Cross-over time on		-	142	-	
$t_{off}^{(1)}$	Turn-off time		-	400	-	
$t_{c(off)}^{(1)}$	Cross-over time off		-	85	-	
t_{rr}	Reverse recovery time		-	215	-	
E_{on}	Turn-on switching energy		-	201	-	
E_{off}	Turn-off switching energy	-	102	-		
E_{rr}	Reverse recovery energy	-	8.1	-		
$t_{on}^{(1)}$	Turn-on time	$V_{DD} = 300\text{ V}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(2)} = 0\text{ to }5\text{ V}$, $I_C = 12\text{ A}$	-	300	-	ns
$t_{c(on)}^{(1)}$	Cross-over time on		-	175	-	
$t_{off}^{(1)}$	Turn-off time		-	380	-	
$t_{c(off)}^{(1)}$	Cross-over time off		-	85	-	
t_{rr}	Reverse recovery time		-	220	-	
E_{on}	Turn-on switching energy		-	340	-	
E_{off}	Turn-off switching energy	-	160	-		
E_{rr}	Reverse recovery energy	-	10.2	-		

Notes:

⁽¹⁾ t_{on} and t_{off} include the propagation delay time of the internal drive. $t_{c(on)}$ and $t_{c(off)}$ are the switching time of the IGBT itself under the internally given gate driving condition.

⁽²⁾Applied between HINx, LINx and GND for x = U, V, W.

Figure 2: Switching time test circuit

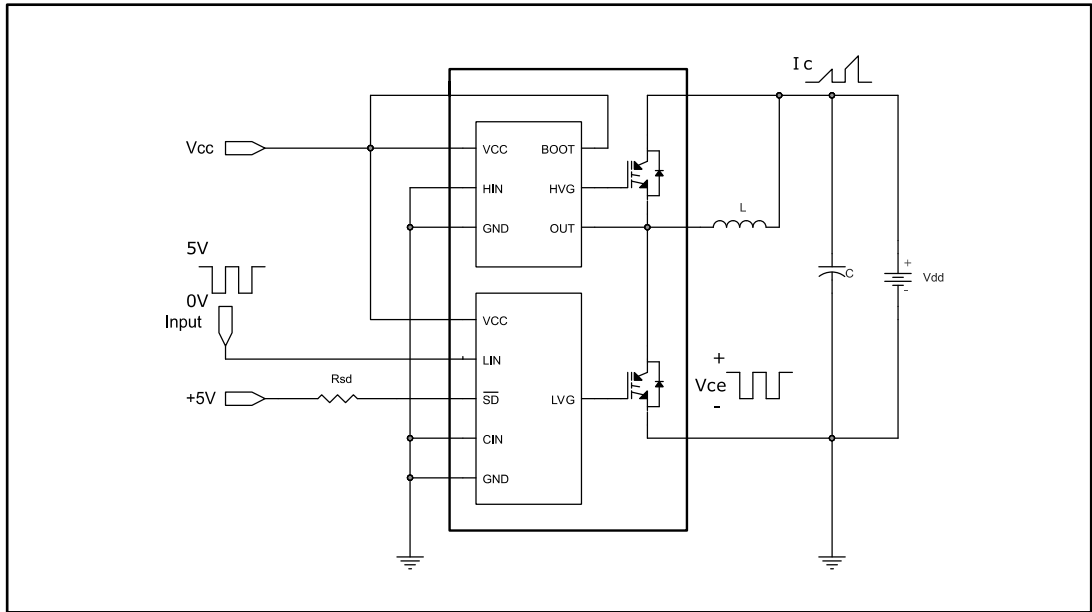
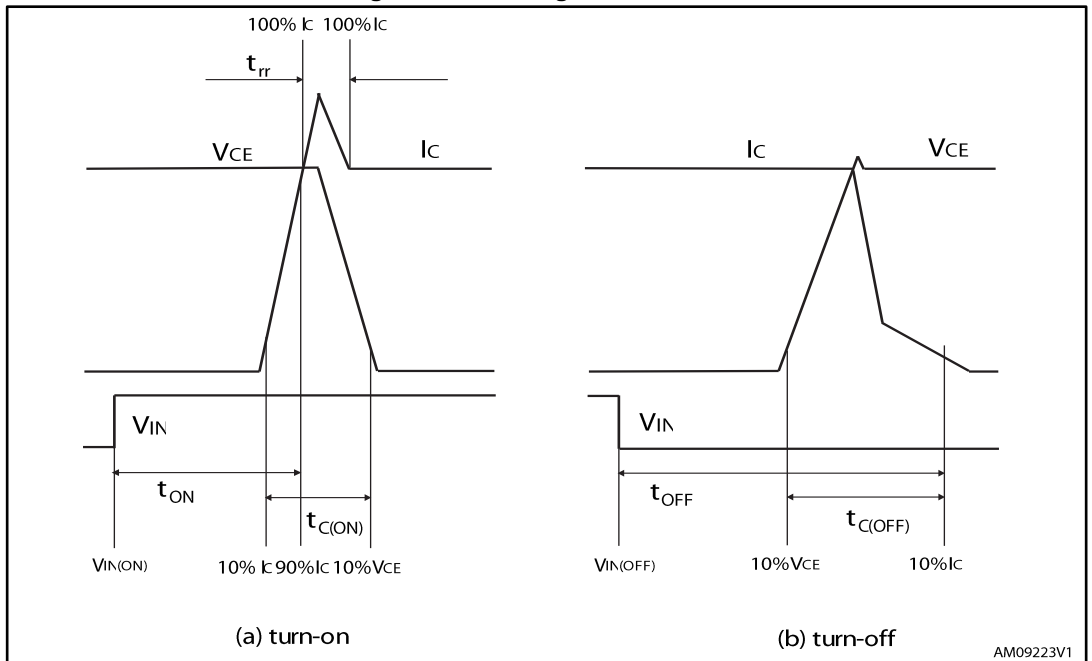


Figure 3: Switching time definition



3.2 Control / protection part

Table 9: High and low side drivers

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{il}	Low logic level voltage				0.8	V
V_{ih}	High logic level voltage		2			V
I_{INh}	IN logic "1" input bias current	$IN_x = 15\text{ V}$	80	150	200	μA
I_{INl}	IN logic "0" input bias current	$IN_x = 0\text{ V}$			1	μA
High side						
V_{CC_hys}	V_{CC} UV hysteresis		1.2	1.4	1.7	V
$V_{CCH_th(on)}$	V_{CCH} UV turn-on threshold		11	11.5	12	V
$V_{CCH_th(off)}$	V_{CCH} UV turn-off threshold		9.6	10.1	10.6	V
V_{BS_hys}	V_{BS} UV hysteresis		0.5	1	1.6	V
$V_{BS_th(on)}$	V_{BS} UV turn-on threshold		10.1	11	11.9	V
$V_{BS_th(off)}$	V_{BS} UV turn-off threshold		9.1	10	10.9	V
I_{QBSU}	Under voltage V_{BS} quiescent current	$V_{BS} = 9\text{ V}$, $HIN_x^{(1)} = 5\text{ V}$		55	75	μA
I_{QBS}	V_{BS} quiescent current	$V_{CC} = 15\text{ V}$, $HIN_x^{(1)} = 5\text{ V}$		125	170	μA
I_{qccu}	Undervoltage quiescent supply current	$V_{CC} = 9\text{ V}$, $HIN_x^{(1)} = 0$		190	250	μA
I_{qcc}	Quiescent current	$V_{CC} = 15\text{ V}$, $HIN_x^{(1)} = 0$		560	730	μA
$R_{DS(on)}$	BS driver ON resistance			150		Ω
Low side						
V_{CC_hys}	V_{CC} UV hysteresis		1.1	1.4	1.6	V
$V_{CCL_th(on)}$	V_{CCL} UV turn-on threshold		10.4	11.6	12.4	V
$V_{CCL_th(off)}$	V_{CCL} UV turn-off threshold		9.0	10.3	11	V
I_{qccu}	Undervoltage quiescent supply current	$V_{CC} = 10\text{ V}$, \overline{SD} pulled to 5 V through $R_{SD} = 10\text{ k}\Omega$, $C_{IN} = LIN_x^{(1)} = 0$		600	800	μA
I_{qcc}	Quiescent current	$V_{CC} = 15\text{ V}$, $\overline{SD} = 5\text{ V}$, $C_{IN} = LIN_x^{(1)} = 0$		700	900	μA
V_{SSD}	Smart \overline{SD} unlatch threshold		0.5	0.6	0.75	V
I_{SDh}	\overline{SD} logic "1" input bias current	$\overline{SD} = 5\text{ V}$	25	50	70	μA
I_{SDl}	\overline{SD} logic "0" input bias current	$\overline{SD} = 0\text{ V}$			1	μA

Notes:

⁽¹⁾Applied between HIN_x , LIN_x and GND for $x = U, V, W$.

Table 10: Temperature sensor output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{T_{SO}}$	Temperature sensor output voltage	$T_j = 25\text{ }^\circ\text{C}$	0.974	1.16	1.345	V
$I_{T_{SO_SNK}}$	Temperature sensor sink current capability			0.1		mA
$I_{T_{SO_SRC}}$	Temperature sensor source current capability		4			mA

Table 11: Sense comparator ($V_{CC} = 15\text{ V}$, unless otherwise is specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{CIN}	C_{IN} input bias current	$V_{CIN} = 1\text{ V}$	-0.2		0.2	μA
V_{ref}	Internal reference voltage		460	510	560	mV
V_{OD}	Open drain low level output voltage	$I_{od} = 5\text{ mA}$			500	mV
t_{CIN_SD}	C_{IN} comparator delay to \overline{SD}	\overline{SD} pulled to 5 V through $R_{SD} = 10\text{ k}\Omega$; measured applying a voltage step 0-1 V to Pin C_{IN} 50 % C_{IN} to 90 % \overline{SD}	240	320	410	ns
SR_{SD}	\overline{SD} fall slew rate	\overline{SD} pulled to 5 V through $R_{SD} = 10\text{ k}\Omega$; $C_L = 1\text{ nF}$ through \overline{SD} and ground; 90% \overline{SD} to 10% \overline{SD}		25		V/ μs

“Please keep in mind that comparator remains enabled even if V_{CC} is in UVLO condition but higher than 4 V”.

4 Fault management

The device integrates an open-drain output connected to the \overline{SD} pin. As soon as a fault occurs, the open-drain is activated and LVGx outputs are forced low. Two types of fault can be pointed out:

- Overcurrent (OC) sensed by the internal comparator (see more detail in [Section 1: "Internal schematic and pin description"](#));
- Undervoltage on supply voltage (V_{CC});

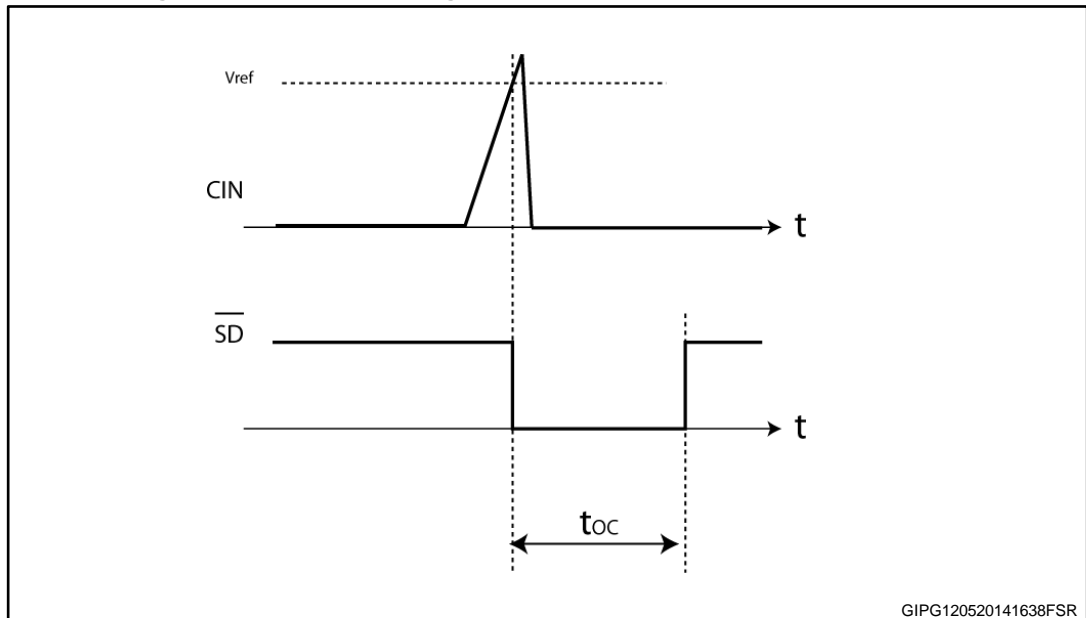
Each fault enables the SD open drain for a specified time, as described in the following table.

Table 12: Fault timing

Symbol	Parameter	Event time	SD open-drain enable time result
OC	Overcurrent event	$\leq 20 \mu s$	20 μs
		$\geq 20 \mu s$	OC time
UVLO	Undervoltage lockout event	$\leq 50 \mu s$	50 μs
		$\geq 50 \mu s$ until the V_{CC_LS} exceed the V_{CC_LS} UV turn ON threshold	UVLO time

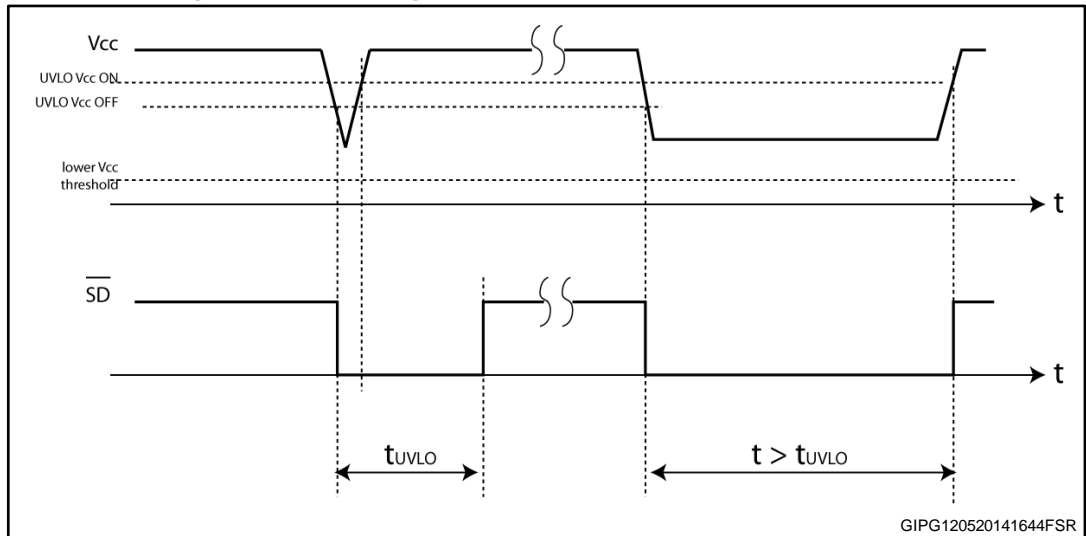
Actually, the device remains in a fault condition (\overline{SD} at low logic level and LVGx outputs disabled) for a time also depending on RC network connected to the \overline{SD} pin. The network generates a time contribute, which is added to the internal value.

Figure 4: Overcurrent timing (without contribution of RC network on \overline{SD})



GIPG120520141638FSR

Figure 5: UVLO timing (without contribution of RC network on \overline{SD})



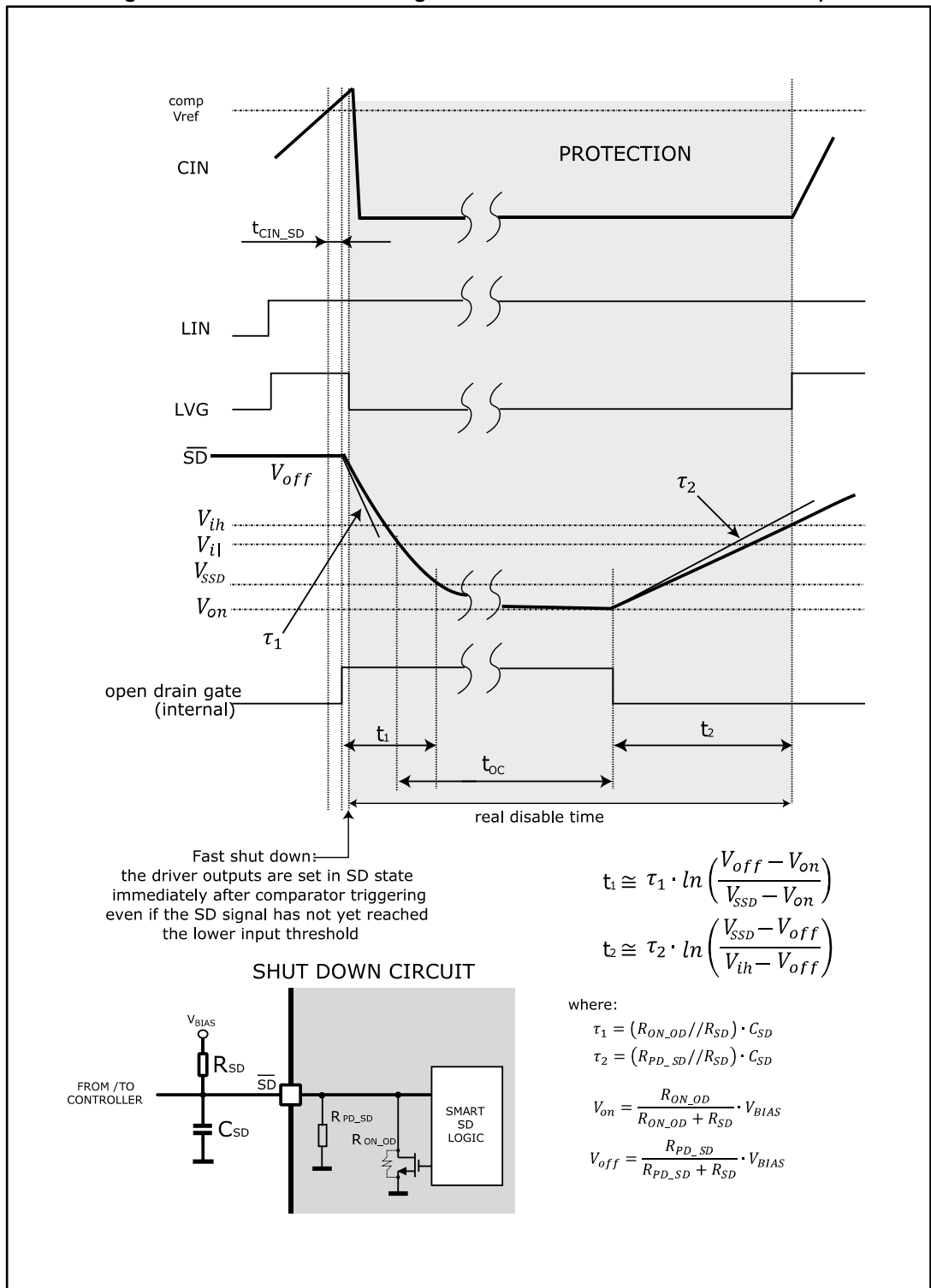
4.1 TSO output

The device integrates a temperature sensor. A voltage proportional to the die temperature is available on the TSO pin. When this function is not used, the pin can be left floating.

4.2 Smart shutdown function

The device integrates a comparator committed to the fault sensing function. The comparator input can be connected to an external shunt resistor in order to implement a simple overcurrent detection function. The output signal of the comparator is fed to an integrated MOSFET with the open drain output available on \overline{SD} input. When the comparator triggers, the device is set to shutdown state and its outputs are all set to low level.

Figure 6: Smart shutdown timing waveforms in case of overcurrent event)



Note: $R_{ON_OD} = V_{OD} / 5 \text{ mA}$ see Table 11: "Sense comparator ($V_{CC} = 15 \text{ V}$, unless otherwise is specified)"; $R_{PD_SD} (\text{typ}) = 5 \text{ V} / I_{SDh}$.

In common overcurrent protection architectures, the comparator output is usually connected to the \overline{SD} input and an RC network is connected to this \overline{SD} line in order to provide a mono-stable circuit which implements a protection time that follows the fault condition. Differently from the common fault detection systems, the device Smart shutdown architecture allows to immediately turn-off the outputs gate driver in case of fault, by minimizing the propagation delay between the fault detection event and the actual outputs switch-off. In fact the time delay between the fault and the outputs turn off is no more dependent on the RC value of the external network connected to the pin. In the smart shutdown circuitry, the fault signal has a preferential path which directly switches off the outputs after the comparator triggering. At the same time the internal logic turns on the open drain output and holds it on until the \overline{SD} voltage goes below the V_{SSD} threshold and t_{oc} time is elapsed. The driver outputs restart following the input pins as soon as the voltage at the \overline{SD} pin reaches the higher threshold of the \overline{SD} logic input. The Smart shutdown system provides the possibility to increase the time constant of the external RC network (that is the disable time after the fault event) up to very large values without increasing the delay time of the protection.

6 Guidelines

1. Input signals HIN and LIN are active-high logic. A 100 k Ω (typ.) pull-down resistor is built in for each input pin. To prevent input signal oscillation, the wiring of each input should be as short as possible and the use of RC filters (R1, C1) on each input signal is recommended. The filters should be implemented with a time constant of about 100 ns and placed as close as possible to the IPM input pins.
2. The use of a bypass capacitor C_{VCC} (aluminum or tantalum) can help reduce the transient circuit demand on the power supply. Also, to reduce high frequency switching noise distributed on the power lines, placing a decoupling capacitor C_2 (100 to 220 nF, with low ESR and low ESL) as close as possible to each V_{CC} pin and in parallel with the bypass capacitor is recommended.
3. The use of RC filter (RSF, CSF) for preventing protection circuit malfunction is recommended. The time constant (RSF x CSF) should be set to 1 μ s and the filter must be placed as close as possible to the CIN pin.
4. The is an input/output pin (open drain type if used as output). It is recommended that it be pulled up to a power supply (i.e., MCU bias at 3.3/5 V) by a resistor value capable of keeping the lod no higher than 5 mA ($V_{OD} \leq 500$ mV when the open drain MOSFET is ON). The filter on \overline{SD} should be sized to obtain a desired restart time after a fault event and placed as close as possible to the \overline{SD} pin.
5. A decoupling capacitor CTSO between 1 nF and 10 nF can be used to increase the noise immunity of the TSO thermal sensor; a similar decoupling capacitor COT (between 10 nF and 100 nF) can be implemented if the NTC thermistor is available and used. In both cases, their effectiveness is improved if the capacitors are placed close to the MCU.
6. The decoupling capacitor C3 (100 to 220 nF with low ESR and low ESL) in parallel with each C_{boot} is useful to filter high frequency disturbances. Both C_{boot} and C3 (if present) should be placed as close as possible to the U,V,W and V_{boot} pins. Bootstrap negative electrodes should be connected to U,V,W terminals directly and separated from the main output wires.
7. To prevent overvoltage on the V_{CC} pin, a Zener diode (Dz1) can be used. Similarly on the V_{boot} pin, a Zener diode (Dz2) can be placed in parallel with each C_{boot} .
8. The use of the decoupling capacitor C_4 (100 to 220 nF, with low ESR and low ESL) in parallel with the electrolytic capacitor C_{vdc} is useful to prevent surge destruction. Both capacitors C_4 and C_{vdc} should be placed as close as possible to the IPM (C_4 has priority over C_{vdc}).
9. By integrating an application-specific type HVIC inside the module, direct coupling to the MCU terminals without an opto-coupler is possible.
10. Low inductance shunt resistors should be used for phase leg current sensing
11. In order to avoid malfunctions, the wiring between N pins, the shunt resistor and PWR_GND should be as short as possible.
12. The connection of SGN_GND to PWR_GND at only one point (close to the shunt resistor terminal) can help to reduce the impact of power ground fluctuation.

These guidelines are useful for application design to ensure the specifications of the device. For further details, please refer to the relevant application note.

Table 13: Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V _{PN}	Supply voltage	Applied between P-Nu, N _v , N _w		300	400	V
V _{CC}	Control supply voltage	Applied between V _{CC} -GND	13.5	15	18	V
V _{BS}	High side bias voltage	Applied between V _{BOOTi} -OUT _i for i = U, V, W	13		18	V
t _{dead}	Blanking time to prevent Arm-short	For each input signal	1.0			μs
f _{PWM}	PWM input signal	-40 °C < T _C < 100 °C -40 °C < T _j < 125 °C			20	kHz
T _C	Case operation temperature				100	°C

7 NTC thermistor

Table 14: NTC thermistor

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R ₂₅	Resistance	T = 25 °C		85		kΩ
R ₁₂₅	Resistance	T = 125 °C		2.6		kΩ
B	B-constant	T = 25 °C to 100 °C		4092		K
T	Operating temperature range		-40		125	°C

Figure 8: NTC resistance vs. temperature

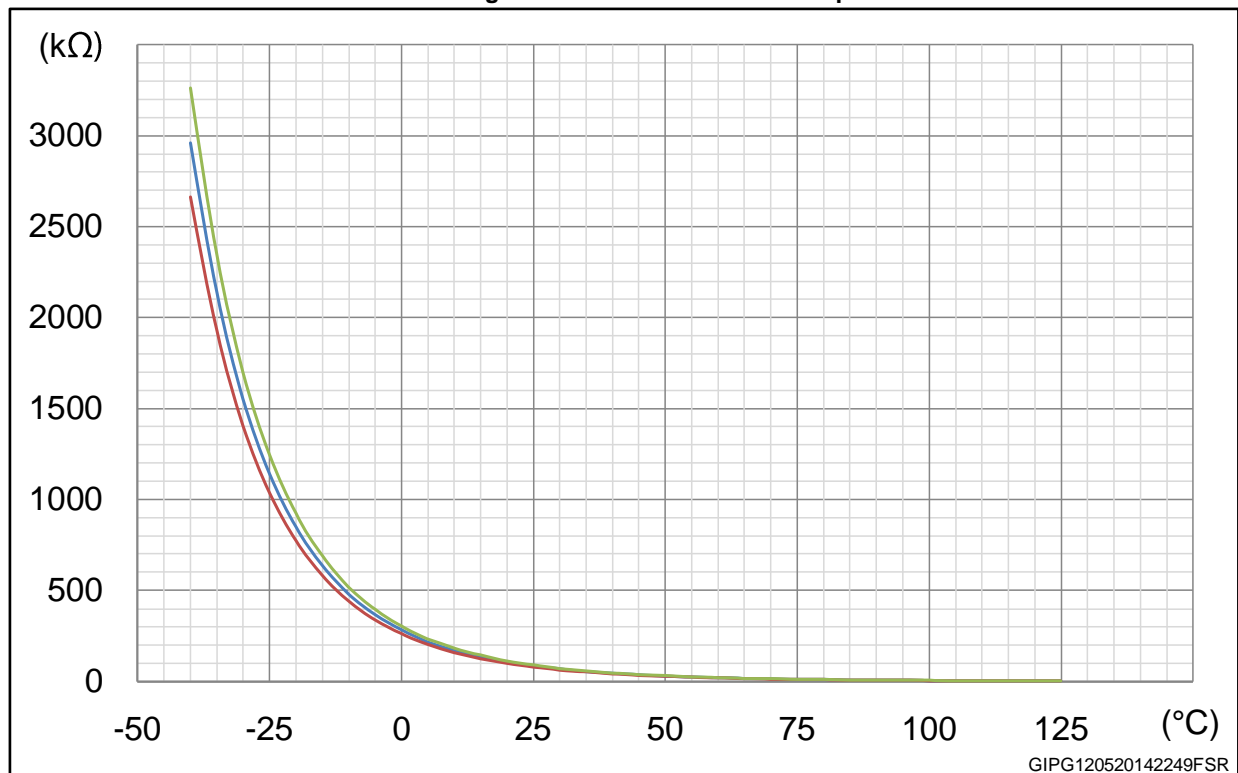
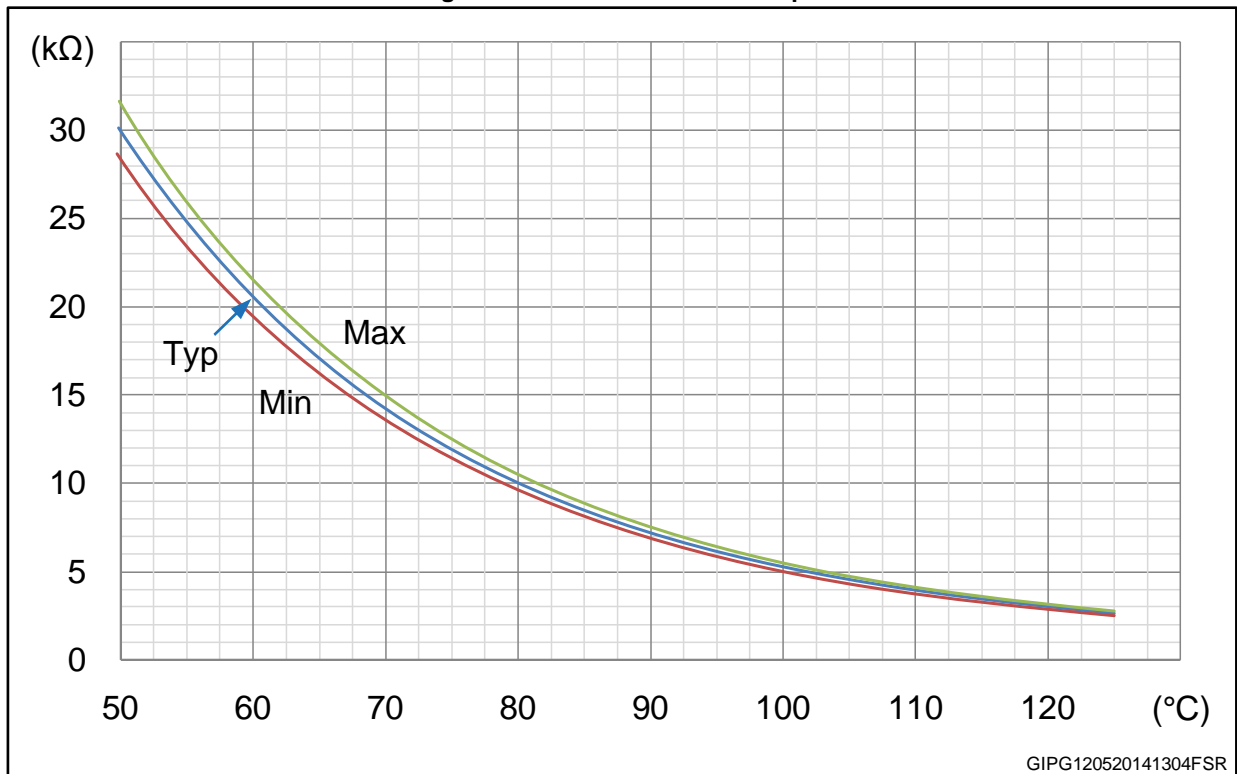


Figure 9: NTC resistance vs. temperature - zoom



8 Electrical characteristics (curves)

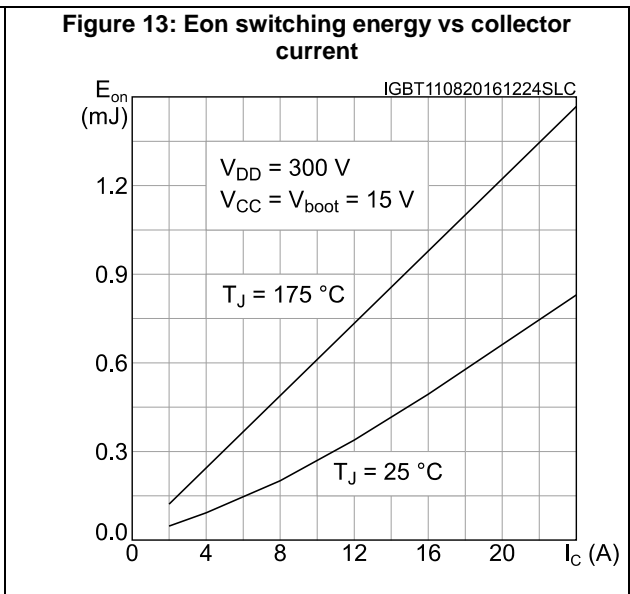
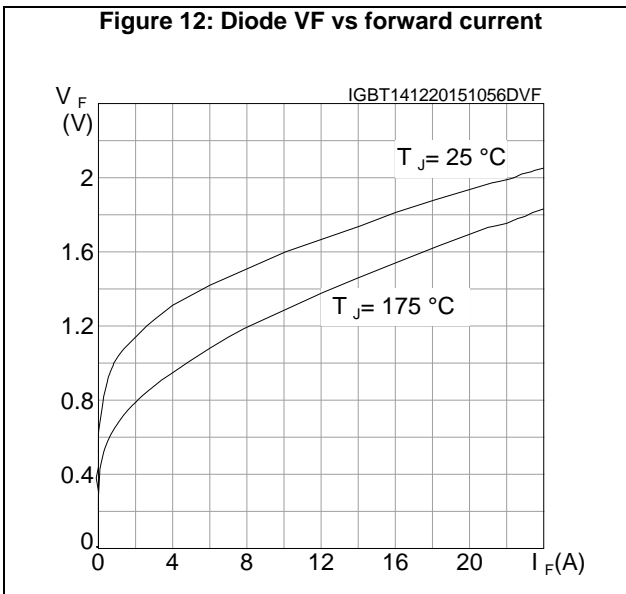
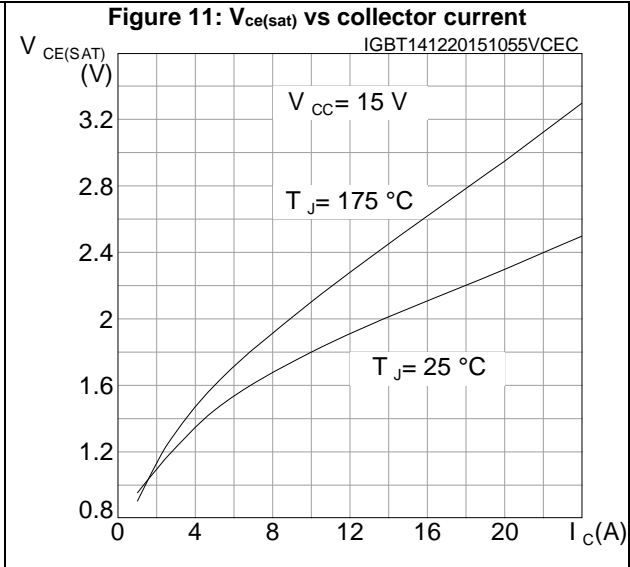
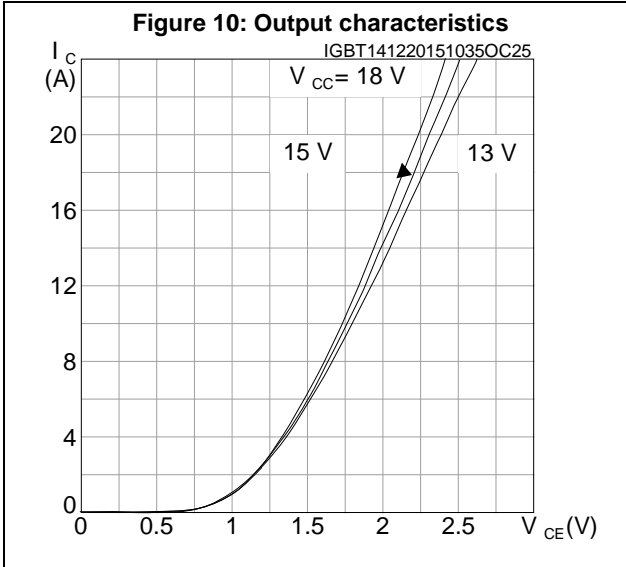


Figure 14: E_{off} switching energy vs collector current

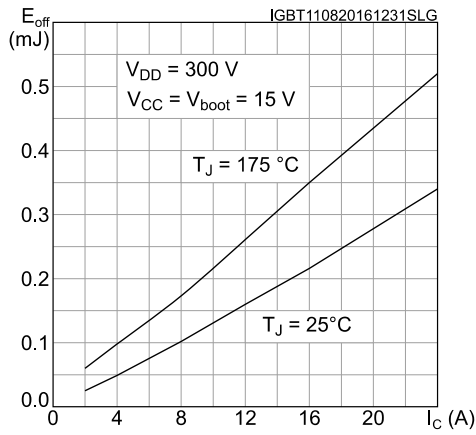


Figure 15: V_{TSO} output characteristics vs LVIC temperature

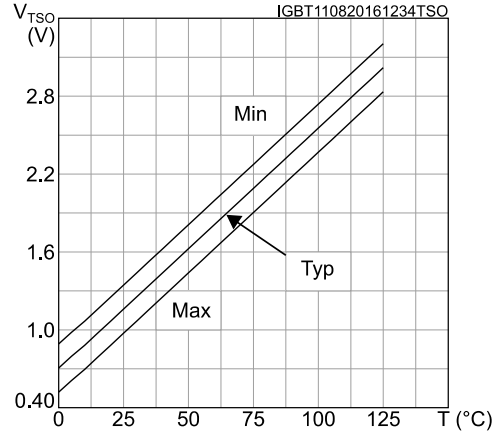
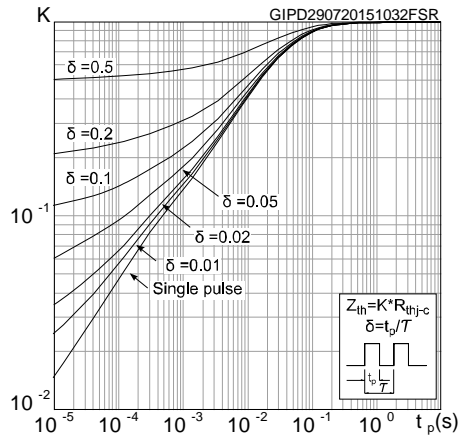


Figure 16: Thermal impedance for SDIP2B-26L IGBT



9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

9.1 SDIP2B-26L type E

Figure 17: SDIP2B-26L type E package outline

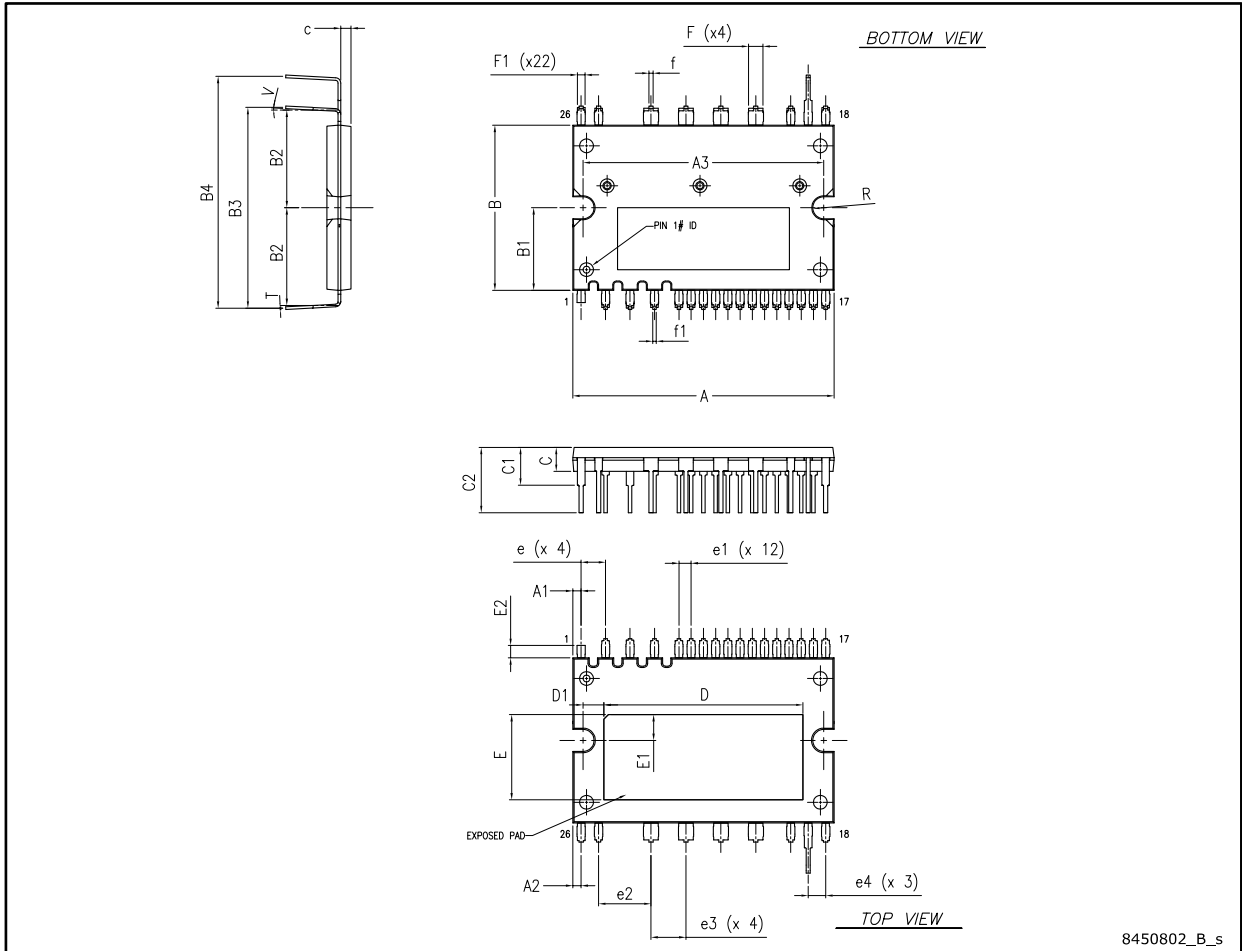


Table 15: SDIP2B-26L type E package mechanical data (dimensions are in mm)

Ref.	Dimensions
A	38.00 ± 0.50
A1	1.22 ± 0.25
A2	1.22 ± 0.25
A3	35.00 ± 0.30
c	1.50 ± 0.05
B	24.00 ± 0.50
B1	12.00
B2	14.40 ± 0.50
B3	29.20 ± 0.50
B4	33.70 ± 0.50
C	3.50 ± 0.20
C1	5.50 ± 0.50
C2	9.50 ± 0.50
e	3.556 ± 0.200
e1	1.778 ± 0.200
e2	7.62 ± 0.20
e3	5.08 ± 0.20
e4	2.54 ± 0.20
D	28.95 ± 0.50
D1	3.025 ± 0.300
E	12.40 ± 0.50
E1	3.75 ± 0.30
E2	1.80
f	0.60 ± 0.15
f1	0.50 ± 0.15
F	2.10 ± 0.15
F1	1.10 ± 0.15
R	1.60 ± 0.20
T	0.400 ± 0.025
V	0° / 5°

10 Revision history

Table 16: Document revision history

Date	Revision	Changes
12-Oct-2016	1	First release.

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