

## N-channel 900 V, 1.90 $\Omega$ typ., 4 A MDmesh™ K5 Power MOSFET in a TO-220FP package

Datasheet - production data

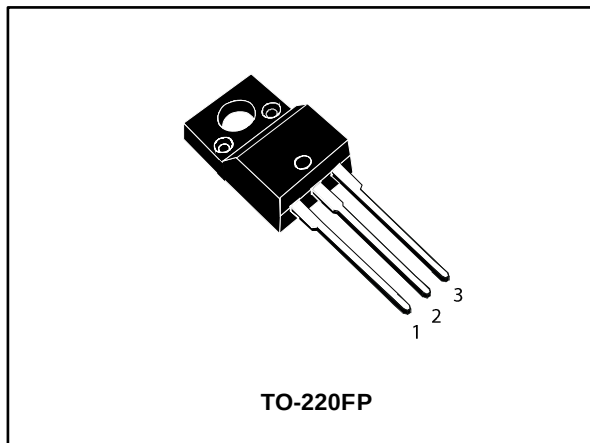
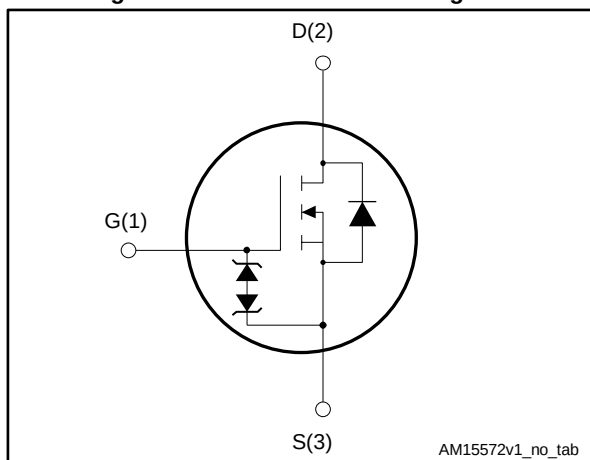


Figure 1: Internal schematic diagram



### Features

| Order code | V <sub>DS</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> |
|------------|-----------------|--------------------------|----------------|
| STF4N90K5  | 900 V           | 2.10 $\Omega$            | 4 A            |

- Industry's lowest R<sub>DS(on)</sub> X area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

| Order code | Marking | Package  | Packing |
|------------|---------|----------|---------|
| STF4N90K5  | 4N90K5  | TO-220FP | Tube    |

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## Contents

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol                 | Parameter                                                                                                                               | Value              | Unit               |
|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|--------------------|--------------------|
| $V_{GS}$               | Gate-source voltage                                                                                                                     | $\pm 30$           | V                  |
| $I_D$                  | Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$                                                                        | 4 <sup>(1)</sup>   | A                  |
| $I_D$                  | Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$                                                                       | 2.5 <sup>(1)</sup> | A                  |
| $I_D^{(2)}$            | Drain current (pulsed)                                                                                                                  | 16                 | A                  |
| $P_{TOT}$              | Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$                                                                                 | 20                 | W                  |
| $dv/dt$ <sup>(3)</sup> | Peak diode recovery voltage slope                                                                                                       | 4.5                | V/ns               |
| $dv/dt$ <sup>(4)</sup> | MOSFET $dv/dt$ ruggedness                                                                                                               | 50                 |                    |
| $V_{ISO}$              | Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t = 1\text{ s}$ ; $T_C = 25\text{ }^{\circ}\text{C}$ ) | 2500               | V                  |
| $T_j$                  | Operating junction temperature range                                                                                                    | - 55 to 150        | $^{\circ}\text{C}$ |
| $T_{stg}$              | Storage temperature range                                                                                                               |                    |                    |

**Notes:**<sup>(1)</sup>Limited by package<sup>(2)</sup>Pulse width limited by safe operating area<sup>(3)</sup> $I_{SD} \leq 4\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ;  $V_{DS}\text{ peak} < V_{(BR)DSS}$ ,  $V_{DD} = 450\text{ V}$ .<sup>(4)</sup> $V_{DS} \leq 720\text{ V}$ 

Table 3: Thermal data

| Symbol         | Parameter                           | Value | Unit                        |
|----------------|-------------------------------------|-------|-----------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case    | 6.25  | $^{\circ}\text{C}/\text{W}$ |
| $R_{thj-amb}$  | Thermal resistance junction-ambient | 62.5  | $^{\circ}\text{C}/\text{W}$ |

Table 4: Avalanche characteristics

| Symbol   | Parameter                                                                                                              | Value | Unit |
|----------|------------------------------------------------------------------------------------------------------------------------|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )                                   | 1     | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 160   | mJ   |

## 2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

Table 5: On/off-state

| Symbol        | Parameter                         | Test conditions                                                                              | Min. | Typ. | Max.     | Unit          |
|---------------|-----------------------------------|----------------------------------------------------------------------------------------------|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$                                                  | 900  |      |          | V             |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 900\text{ V}$                                              |      |      | 1        | $\mu\text{A}$ |
|               |                                   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 900\text{ V}$<br>$T_C = 125\text{ }^{\circ}\text{C}^{(1)}$ |      |      | 50       | $\mu\text{A}$ |
| $I_{GSS}$     | Gate body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$                                           |      |      | $\pm 10$ | $\mu\text{A}$ |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DD} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$                                           | 3    | 4    | 5        | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 1.5\text{ A}$                                                |      | 1.90 | 2.10     | $\Omega$      |

**Notes:**

<sup>(1)</sup> Defined by design, not subject to production test.

Table 6: Dynamic

| Symbol            | Parameter                             | Test conditions                                                                                                                                     | Min. | Typ. | Max. | Unit     |
|-------------------|---------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|----------|
| $C_{iss}$         | Input capacitance                     | $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ ,<br>$V_{GS} = 0\text{ V}$                                                                             | -    | 173  | -    | pF       |
| $C_{oss}$         | Output capacitance                    |                                                                                                                                                     | -    | 17.9 | -    | pF       |
| $C_{rss}$         | Reverse transfer capacitance          |                                                                                                                                                     | -    | 1    | -    | pF       |
| $C_{o(tr)}^{(1)}$ | Equivalent capacitance time related   | $V_{DS} = 0\text{ to }720\text{ V}$ ,<br>$V_{GS} = 0\text{ V}$                                                                                      | -    | 29   | -    | pF       |
| $C_{o(er)}^{(2)}$ | Equivalent capacitance energy related |                                                                                                                                                     | -    | 11   | -    | pF       |
| $R_g$             | Intrinsic gate resistance             | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$                                                                                                             | -    | 15.5 | -    | $\Omega$ |
| $Q_g$             | Total gate charge                     | $V_{DD} = 720\text{ V}$ , $I_D = 3\text{ A}$<br>$V_{GS} = 10\text{ V}$<br>(see <a href="#">Figure 15: "Test circuit for gate charge behavior"</a> ) | -    | 5.3  | -    | nC       |
| $Q_{gs}$          | Gate-source charge                    |                                                                                                                                                     | -    | 1.45 | -    | nC       |
| $Q_{gd}$          | Gate-drain charge                     |                                                                                                                                                     | -    | 2.8  | -    | nC       |

**Notes:**

<sup>(1)</sup> Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

<sup>(2)</sup> Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

Table 7: Switching times

| Symbol       | Parameter           | Test conditions                                                                                                                                                                                                                                   | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 450\text{ V}$ , $I_D = 1.50\text{ A}$ ,<br>$R_G = 4.7\ \Omega$ ; $V_{GS} = 10\text{ V}$<br>(see <a href="#">Figure 14: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 19: "Switching time waveform"</a> ) | -    | 10.5 | -    | ns   |
| $t_r$        | Rise time           |                                                                                                                                                                                                                                                   | -    | 11.8 | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time |                                                                                                                                                                                                                                                   | -    | 26.4 | -    | ns   |
| $t_f$        | Fall time           |                                                                                                                                                                                                                                                   | -    | 25.5 | -    | ns   |

Table 8: Source-drain diode

| Symbol          | Parameter                     | Test conditions                                                                                                                                                                                                                      | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                                                                                                                      | -    |      | 4    | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                                                                                                                      | -    |      | 16   | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 3\text{ A}$ , $V_{GS} = 0\text{ V}$                                                                                                                                                                                        | -    |      | 1.5  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 3\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$<br>(see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> )                                        | -    | 289  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                                      | -    | 1.56 |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                                      | -    | 10.8 |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 3\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$<br>(see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> ) | -    | 494  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                                      | -    | 2.45 |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                                      | -    | 9.9  |      | A             |

**Notes:**

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

Table 9: Gate-source Zener diode

| Symbol        | Parameter                     | Test conditions                                 | Min. | Typ. | Max. | Unit |
|---------------|-------------------------------|-------------------------------------------------|------|------|------|------|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS} = \pm 1\text{ mA}$ , $I_D = 0\text{ A}$ | 30   | -    | -    | V    |

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

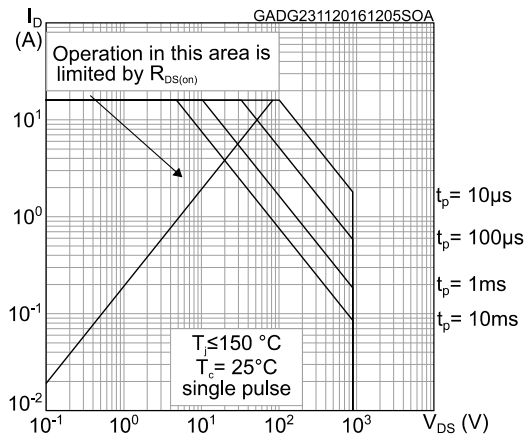


Figure 3: Thermal impedance

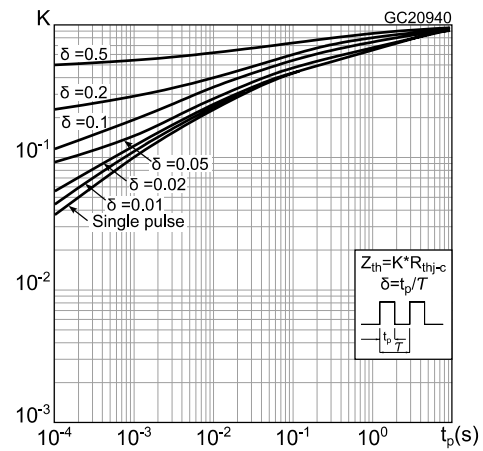


Figure 4: Output characteristics

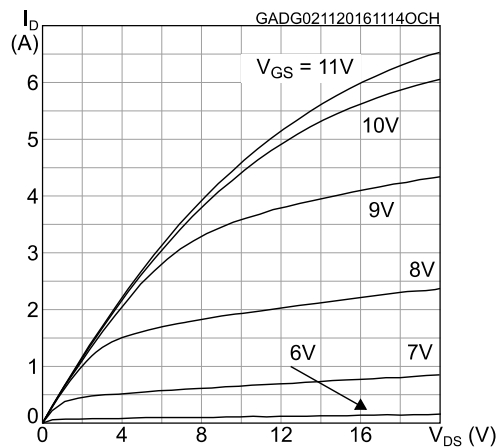


Figure 5: Transfer characteristics

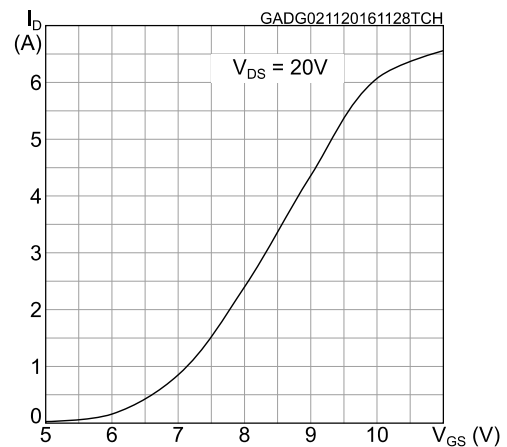


Figure 6: Gate charge vs gate-source voltage

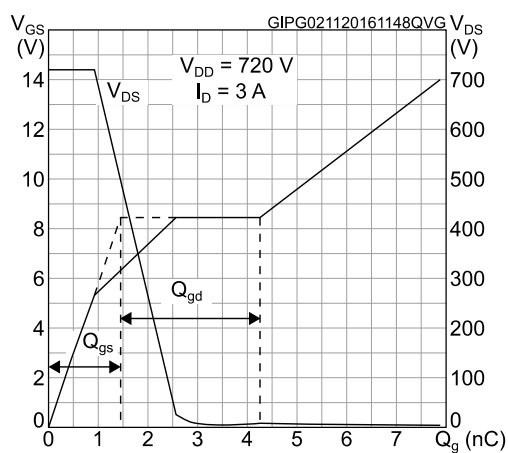


Figure 7: Static drain-source on-resistance

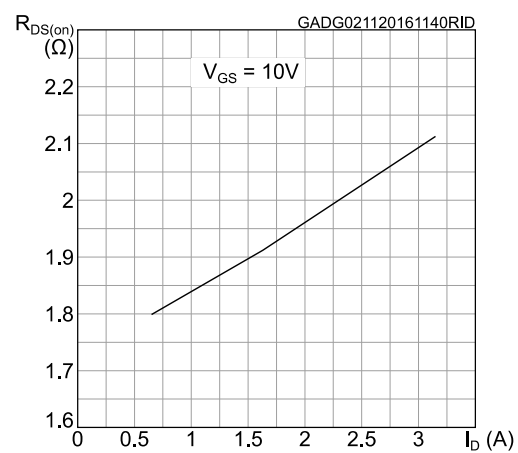


Figure 8: Capacitance variations

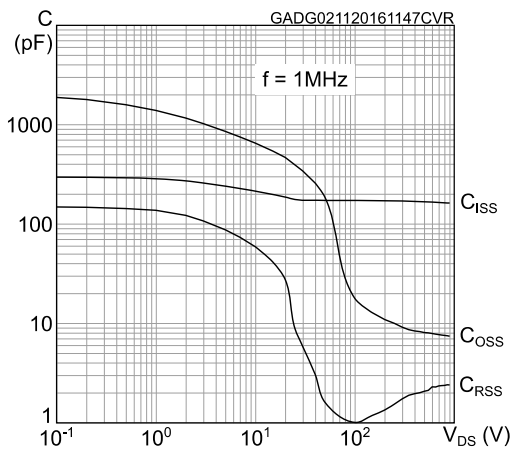


Figure 9: Normalized gate threshold voltage vs temperature

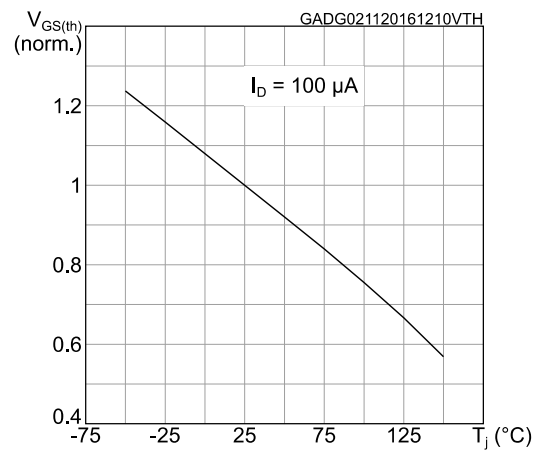


Figure 10: Normalized on-resistance vs temperature

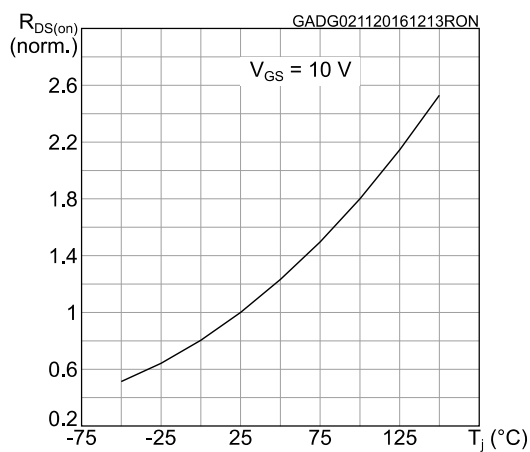


Figure 11: Normalized V(BR)DSS vs temperature

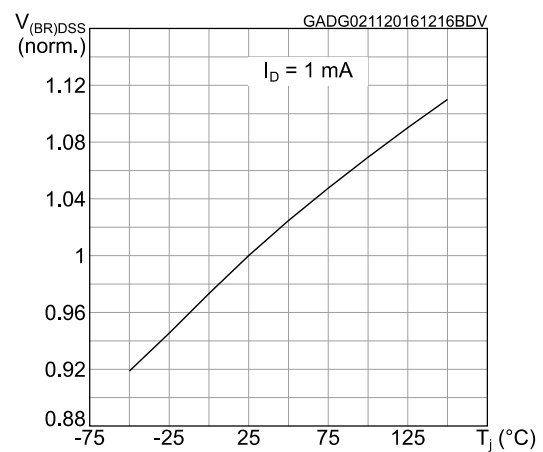


Figure 12: Maximum avalanche energy vs starting T\_J

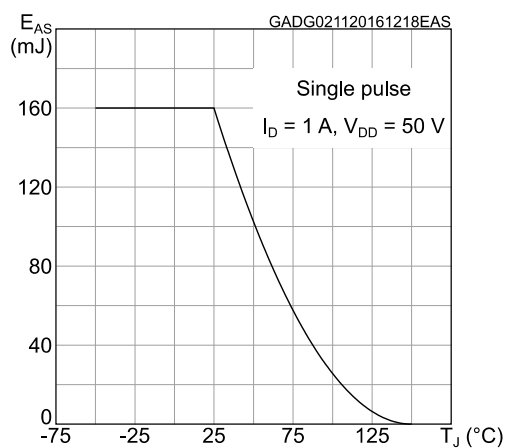
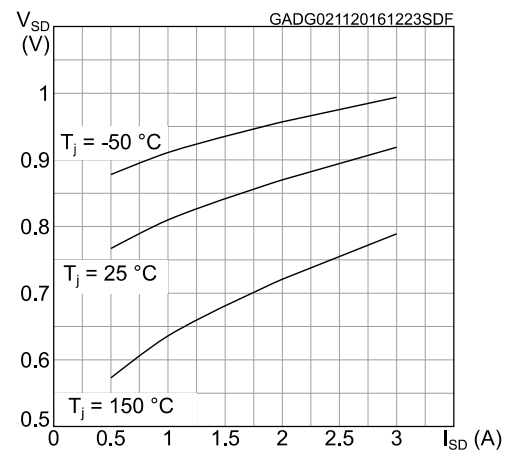
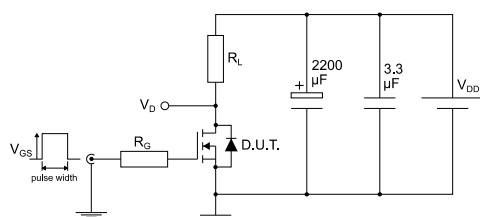


Figure 13: Source-drain diode forward characteristics



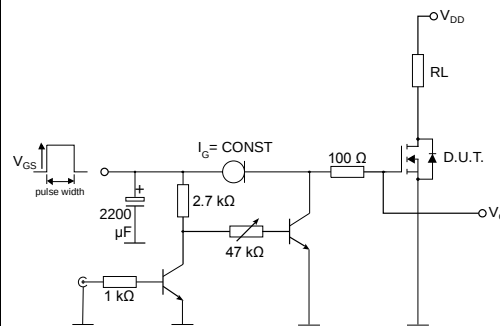
### 3 Test circuits

**Figure 14: Test circuit for resistive load switching times**



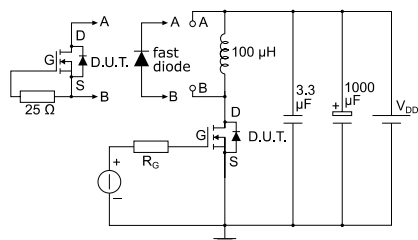
AM01468v1

**Figure 15: Test circuit for gate charge behavior**



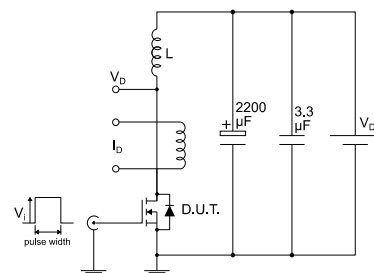
AM01469v10

**Figure 16: Test circuit for inductive load switching and diode recovery times**



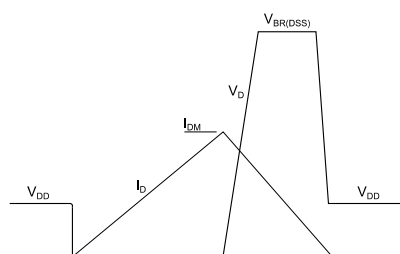
AM01470v1

**Figure 17: Unclamped inductive load test circuit**



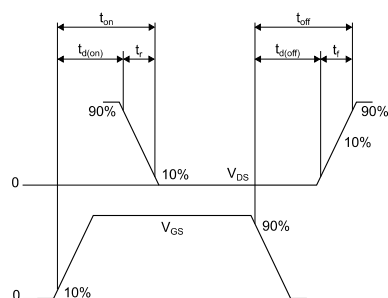
AM01471v1

**Figure 18: Unclamped inductive waveform**



AM01472v1

**Figure 19: Switching time waveform**



AM01473v1

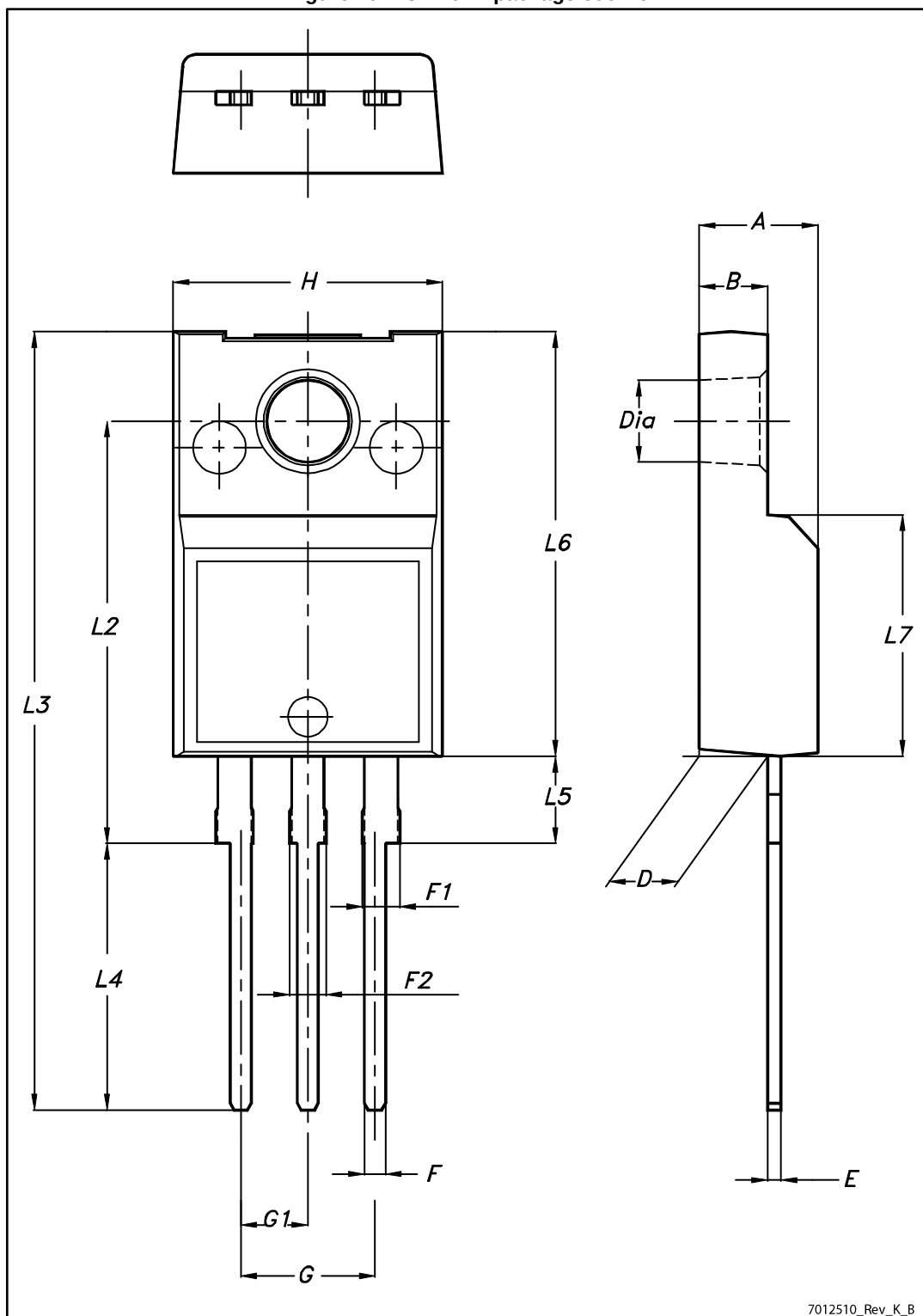


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **[www.st.com](http://www.st.com)**. ECOPACK® is an ST trademark.

## 4.1 TO-220FP package information

Figure 20: TO-220FP package outline



7012510\_Rev\_K\_B

Table 10: TO-220FP package mechanical data

| Dim. | mm   |      |      |
|------|------|------|------|
|      | Min. | Typ. | Max. |
| A    | 4.4  |      | 4.6  |
| B    | 2.5  |      | 2.7  |
| D    | 2.5  |      | 2.75 |
| E    | 0.45 |      | 0.7  |
| F    | 0.75 |      | 1    |
| F1   | 1.15 |      | 1.70 |
| F2   | 1.15 |      | 1.70 |
| G    | 4.95 |      | 5.2  |
| G1   | 2.4  |      | 2.7  |
| H    | 10   |      | 10.4 |
| L2   |      | 16   |      |
| L3   | 28.6 |      | 30.6 |
| L4   | 9.8  |      | 10.6 |
| L5   | 2.9  |      | 3.6  |
| L6   | 15.9 |      | 16.4 |
| L7   | 9    |      | 9.3  |
| Dia  | 3    |      | 3.2  |

## 5 Revision history

Table 11: Document revision history

| Date        | Revision | Changes                                                                 |
|-------------|----------|-------------------------------------------------------------------------|
| 02-Nov-2016 | 1        | First release.                                                          |
| 23-Nov-2016 | 2        | Updated <i>Figure 2: "Safe operating area"</i> .<br>Minor text changes. |

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