

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

OptiMOS™

OptiMOS™ Power-Transistor, 300 V
IPP410N30N

Data Sheet

Rev. 2.0
Final

1 Description

Features

- N-channel, normal level
- Fast Diode with reduced Q_{rr}
- Optimized for hard commutation ruggedness
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC¹⁾ for target application
- Halogen-free according to IEC61249-2-21

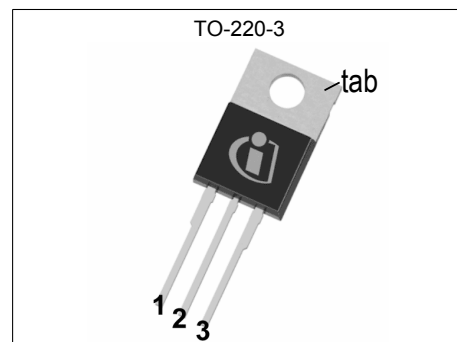
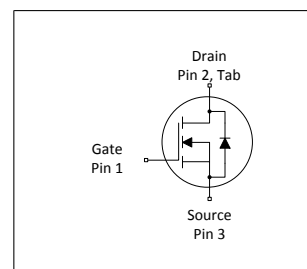


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	300	V
$R_{DS(on),max}$	41	mΩ
I_D	44	A



Type / Ordering Code	Package	Marking	Related Links
IPP410N30N	PG-TO220-3	410N30N	-

¹⁾ J-STD20 and JESD22

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2 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	44 34	A	$T_C=25\text{ °C}$ $T_C=100\text{ °C}$
Pulsed drain current ¹⁾	$I_{D,pulse}$	-	-	176	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	E_{AS}	-	-	240	mJ	$I_D=22\text{ A}$, $R_{GS}=50\text{ }\Omega$
Reverse diode peak dv/dt	dv/dt	-	-	60	kV/ μ s	$I_D=44\text{ A}$, $V_{DS}=150\text{ V}$, $di/dt=1000\text{ A}/\mu\text{s}$, $T_{j,max}=175\text{ °C}$
Gate source voltage	V_{GS}	-20	-	20	V	-
Diode hard commutation breakdown current ²⁾	P_{tot}	-	-	300	W	$T_C=25\text{ °C}$
Operating and storage temperature	T_j , T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case ³⁾	R_{thJC}	-	0.3	0.5	K/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62	K/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁴⁾	R_{thJA}	-	-	40	K/W	-

¹⁾ See figure 3

²⁾ Diode pulse current is defined by thermal and/or package limits

³⁾ Defined by design. Not subject to production test.

⁴⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μ m thick) copper area for drain connection. PCB is vertical in still air.

4 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	300	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2	3	4	V	$V_{DS}=V_{GS}$, $I_D=270\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	1 10	10 300	μA	$V_{DS}=240\text{ V}$, $V_{GS}=0\text{ V}$, $T_J=25\text{ }^\circ\text{C}$ $V_{DS}=240\text{ V}$, $V_{GS}=0\text{ V}$, $T_J=125\text{ }^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	1	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	36	41	m Ω	$V_{GS}=10\text{ V}$, $I_D=44\text{ A}$
Gate resistance ¹⁾	R_G	-	2.4	3.6	Ω	-
Transconductance	g_{fs}	52	103	-	S	$ V_{DS} >2 I_D /R_{DS(on)max}$, $I_D=44\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	5400	7180	pF	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	281	374	pF	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	6	13	pF	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	16	-	ns	$V_{DD}=100\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=22\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	9	-	ns	$V_{DD}=100\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=22\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	43	-	ns	$V_{DD}=100\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=22\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	9	-	ns	$V_{DD}=100\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=22\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	24	-	nC	$V_{DD}=100\text{ V}$, $I_D=44\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	7	-	nC	$V_{DD}=100\text{ V}$, $I_D=44\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	15	-	nC	$V_{DD}=100\text{ V}$, $I_D=44\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	65	87	nC	$V_{DD}=100\text{ V}$, $I_D=44\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.4	-	V	$V_{DD}=100\text{ V}$, $I_D=44\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	131	-	nC	$V_{DD}=100\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	44	A	$T_C=25\text{ °C}$
Diode pulse current ¹⁾	$I_{S,pulse}$	-	-	176	A	$T_C=25\text{ °C}$
Diode hard commutation current ²⁾	$I_{S,hard}$	-	-	44	A	$T_C=25\text{ °C}$, $di_F/dt=1000\text{ A/}\mu\text{s}$
Diode forward voltage	V_{SD}	-	0.9	1.2	V	$V_{GS}=0\text{ V}$, $I_F=44\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time ³⁾	t_{rr}	-	152	304	ns	$V_R=100\text{ V}$, $I_F=32.2\text{ A}$, $di_F/dt=100\text{ A/}\mu\text{s}$
Reverse recovery charge ³⁾	Q_{rr}	-	844	1689	nC	$V_R=100\text{ V}$, $I_F=32.2\text{ A}$, $di_F/dt=100\text{ A/}\mu\text{s}$

¹⁾ Diode pulse current is defined by thermal and/or package limits

²⁾ Maximum allowed hard-commutated current through diode at $di/dt=1000\text{ A/}\mu\text{s}$
³⁾ Defined by design. Not subject to production test.

5 Electrical characteristics diagrams

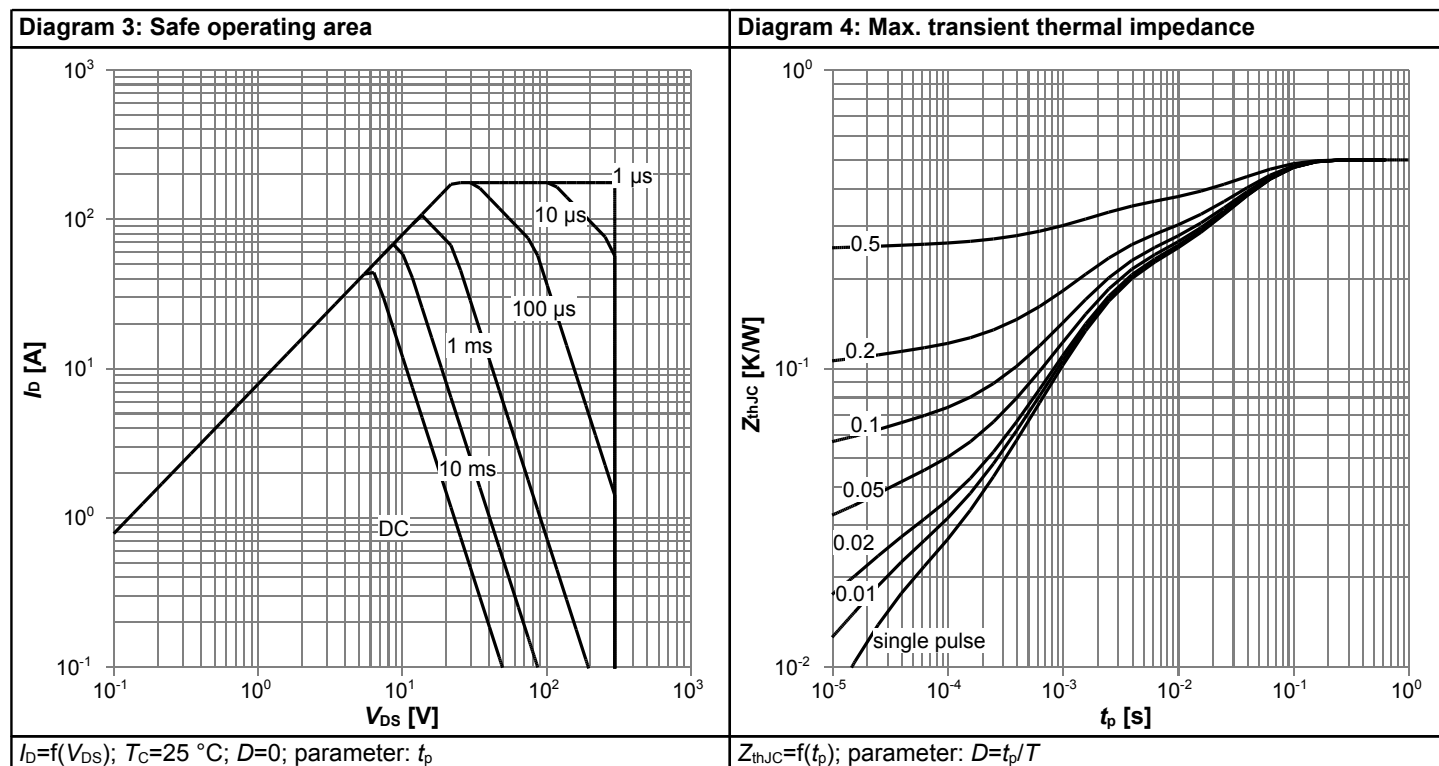
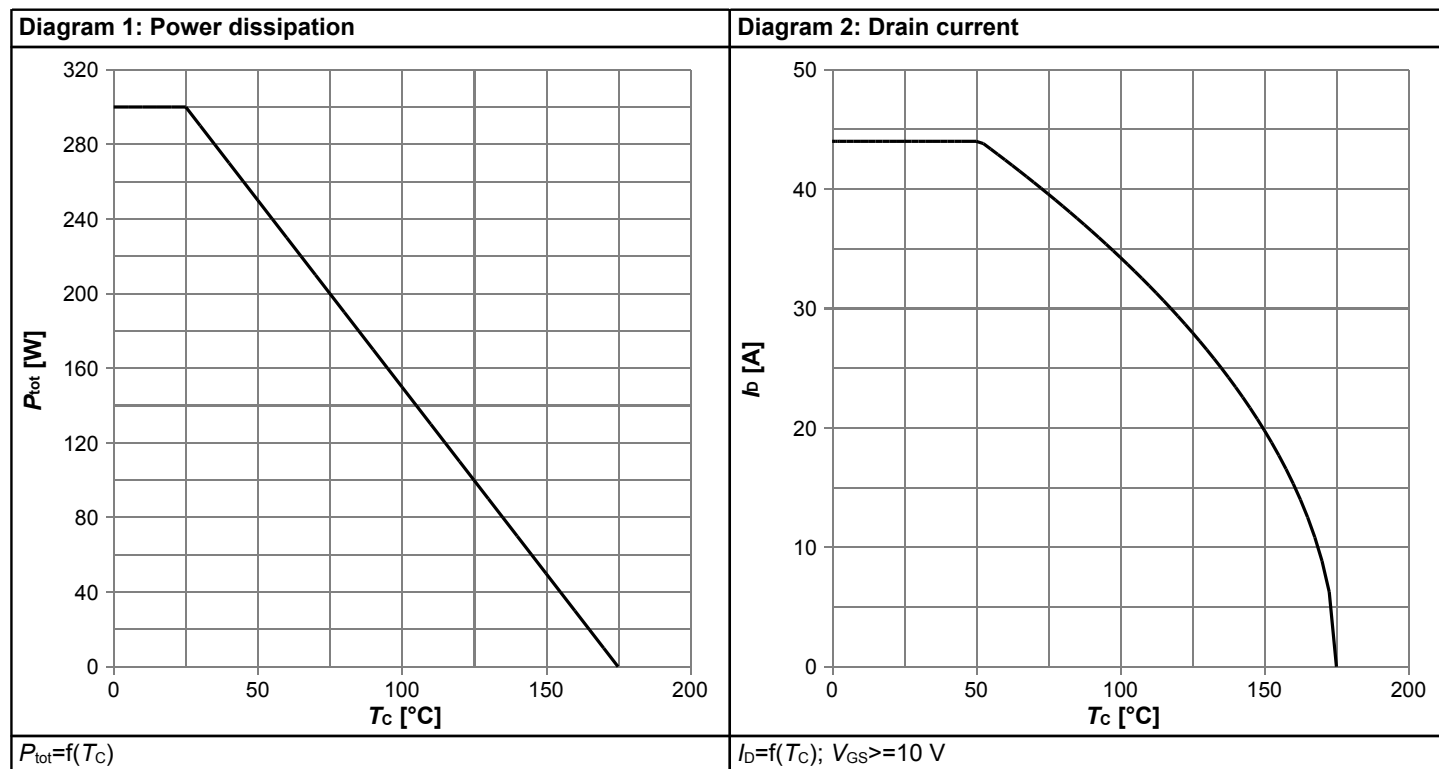


Diagram 5: Typ. output characteristics

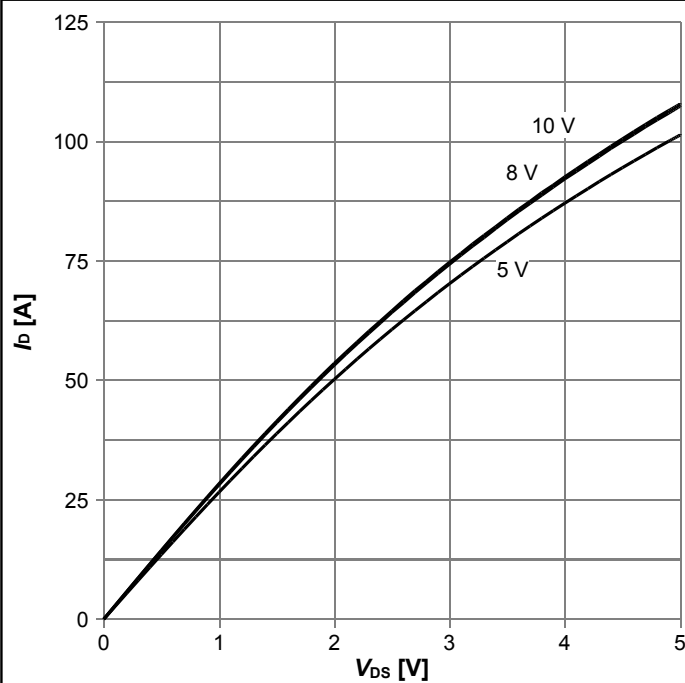

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. drain-source on resistance

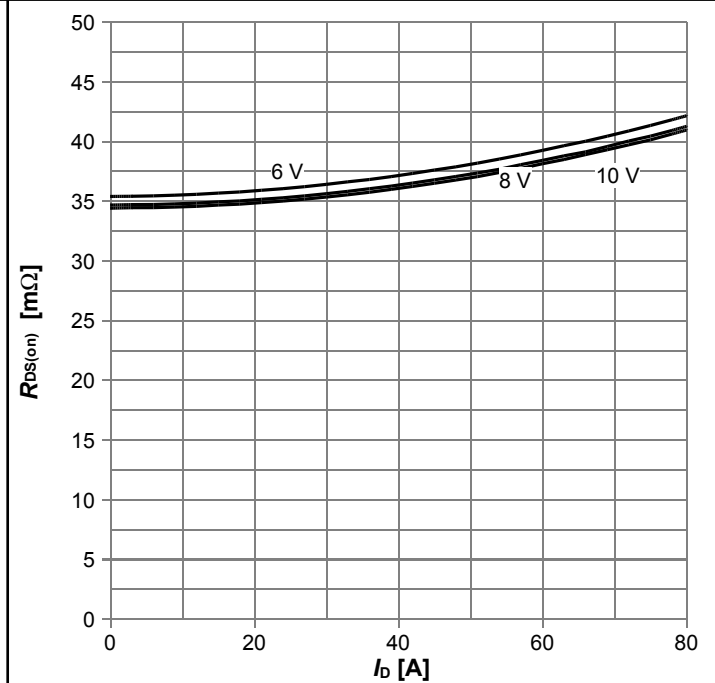

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. transfer characteristics

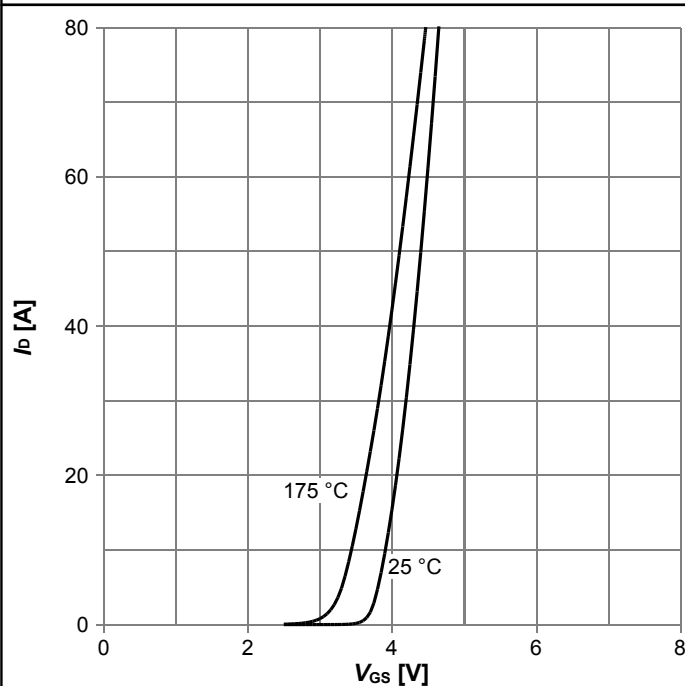

 $I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)\text{max}}; \text{parameter: } T_j$

Diagram 8: Typ. forward transconductance

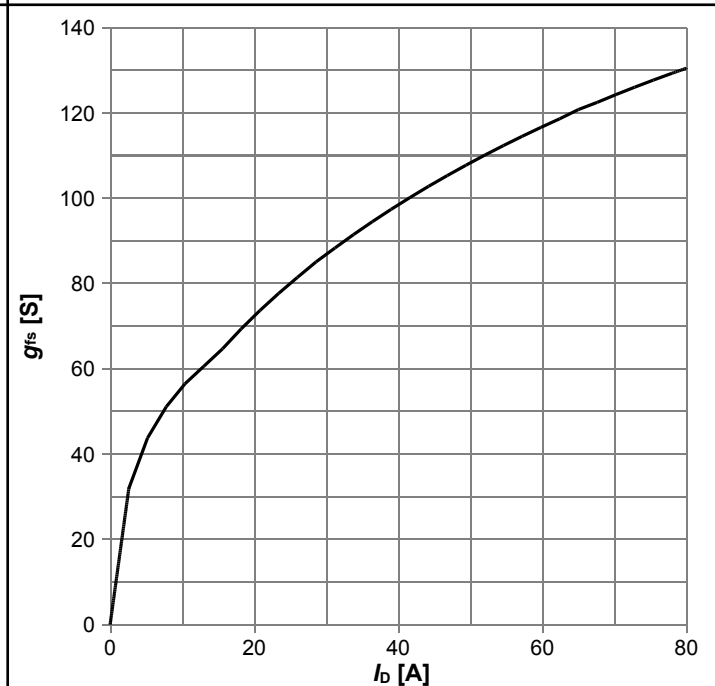
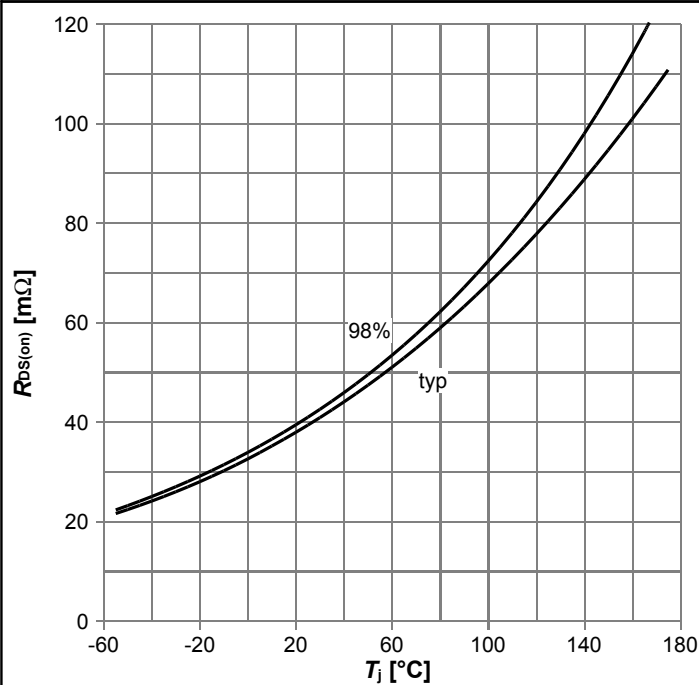
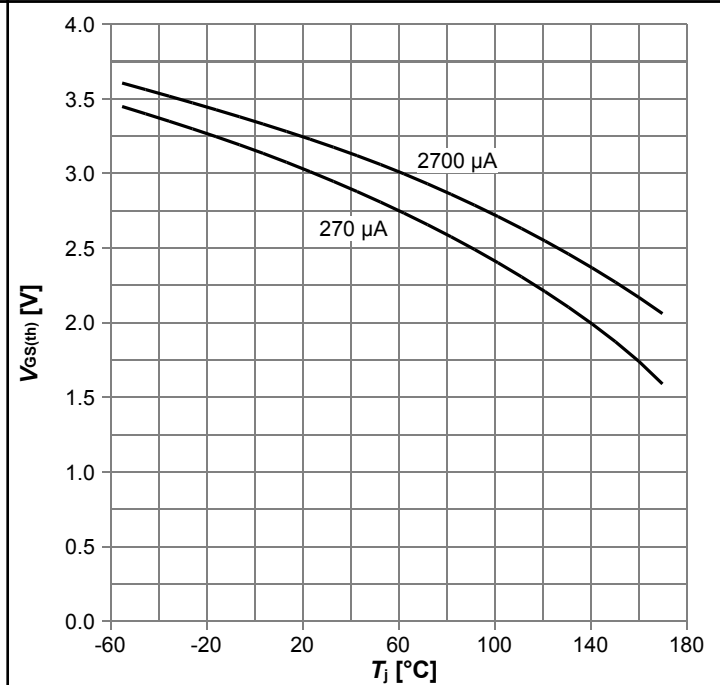

 $g_{fs} = f(I_D); T_j = 25^\circ\text{C}$

Diagram 9: Drain-source on-state resistance



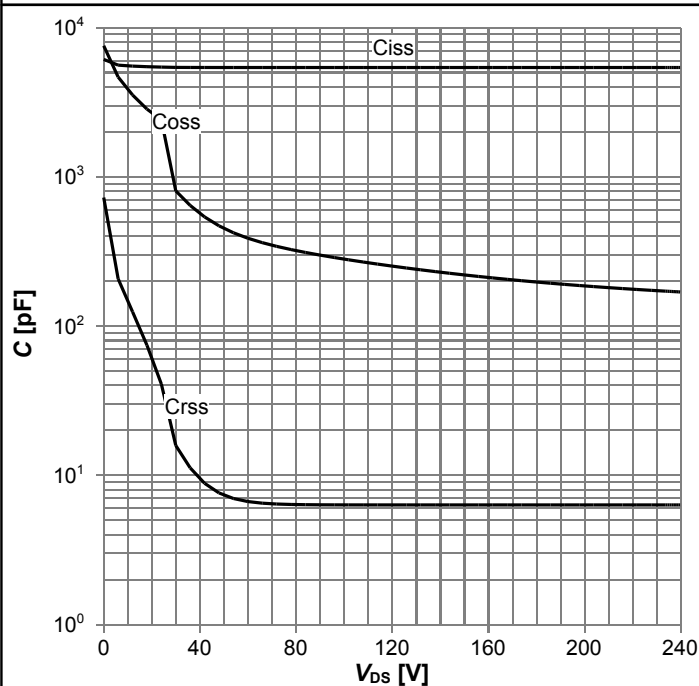
$$R_{DS(on)} = f(T_j); I_D = 44 \text{ A}; V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



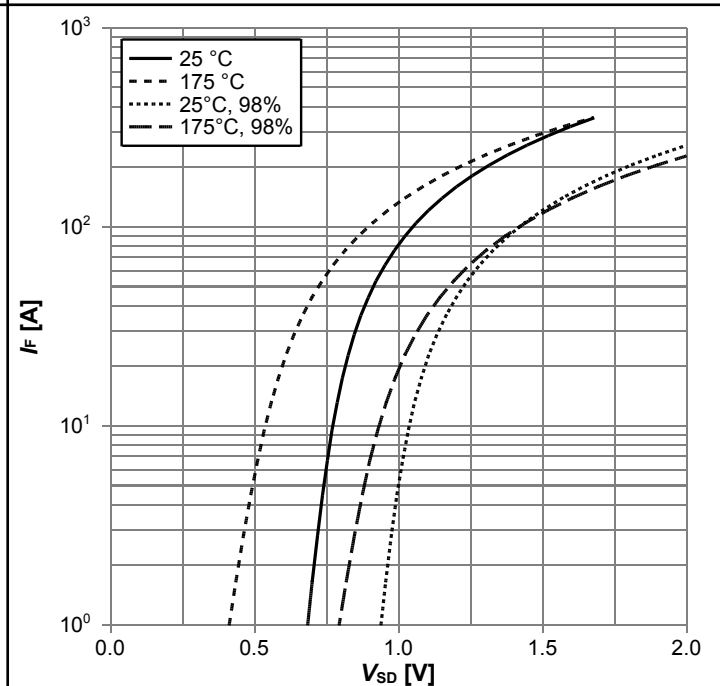
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; \text{parameter: } I_D$$

Diagram 11: Typ. capacitances



$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Forward characteristics of reverse diode



$$I_F = f(V_{SD}); \text{parameter: } T_j$$

Diagram 13: Avalanche characteristics

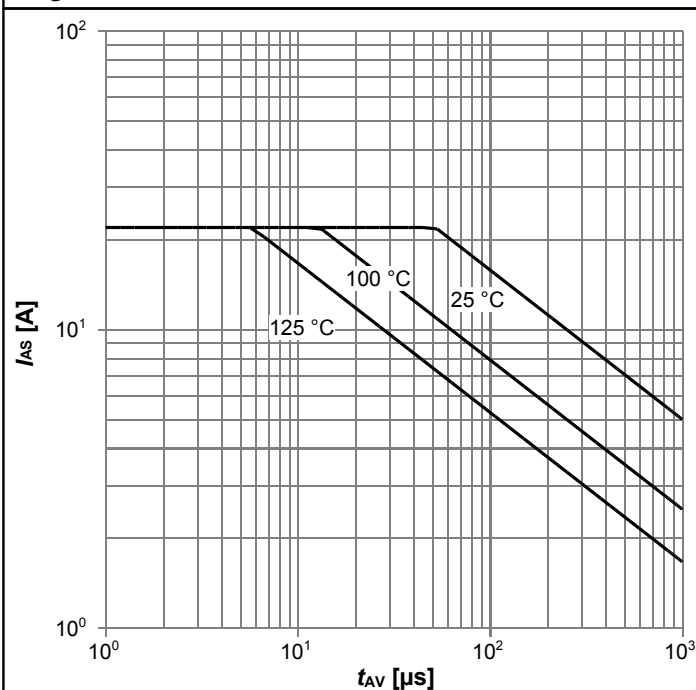

 $I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega; \text{parameter: } T_{j(\text{start})}$

Diagram 14: Typ. gate charge

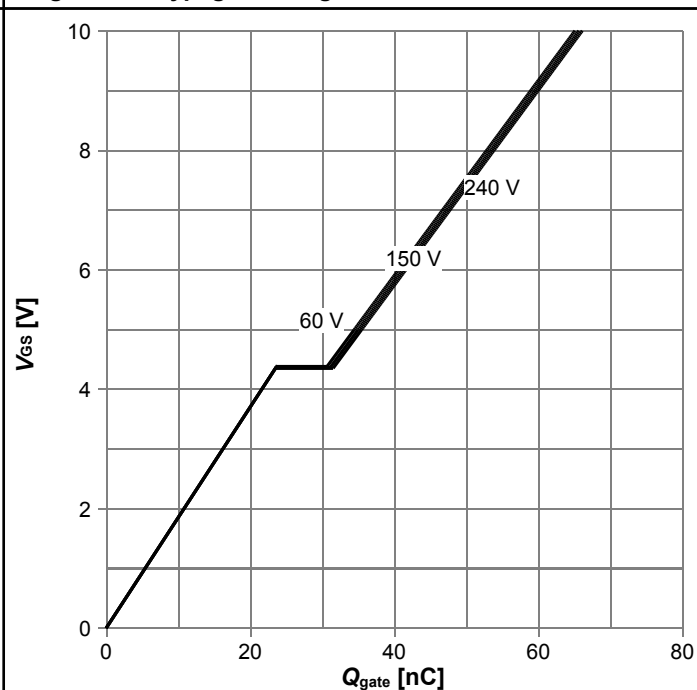
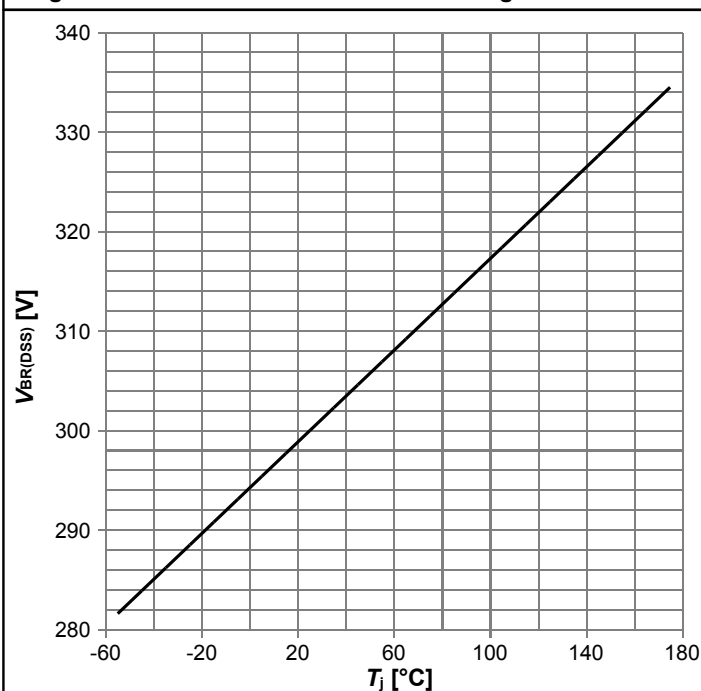
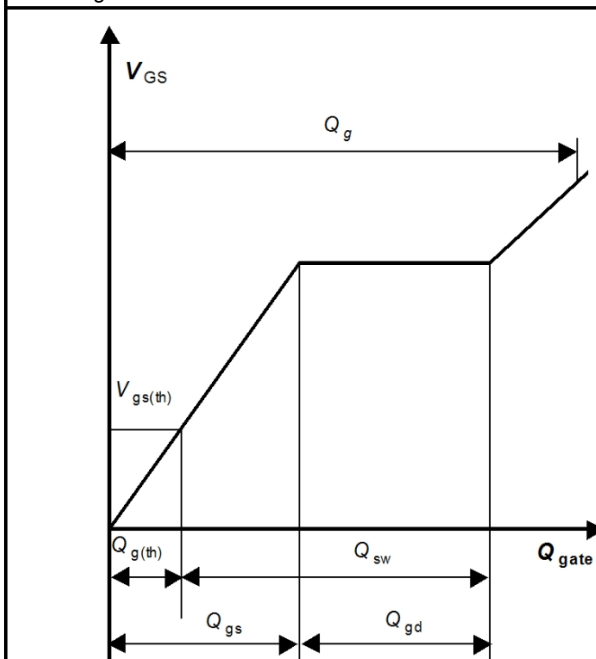

 $V_{GS}=f(Q_{\text{gate}}); I_D=44\ \text{A pulsed}; \text{parameter: } V_{DD}$

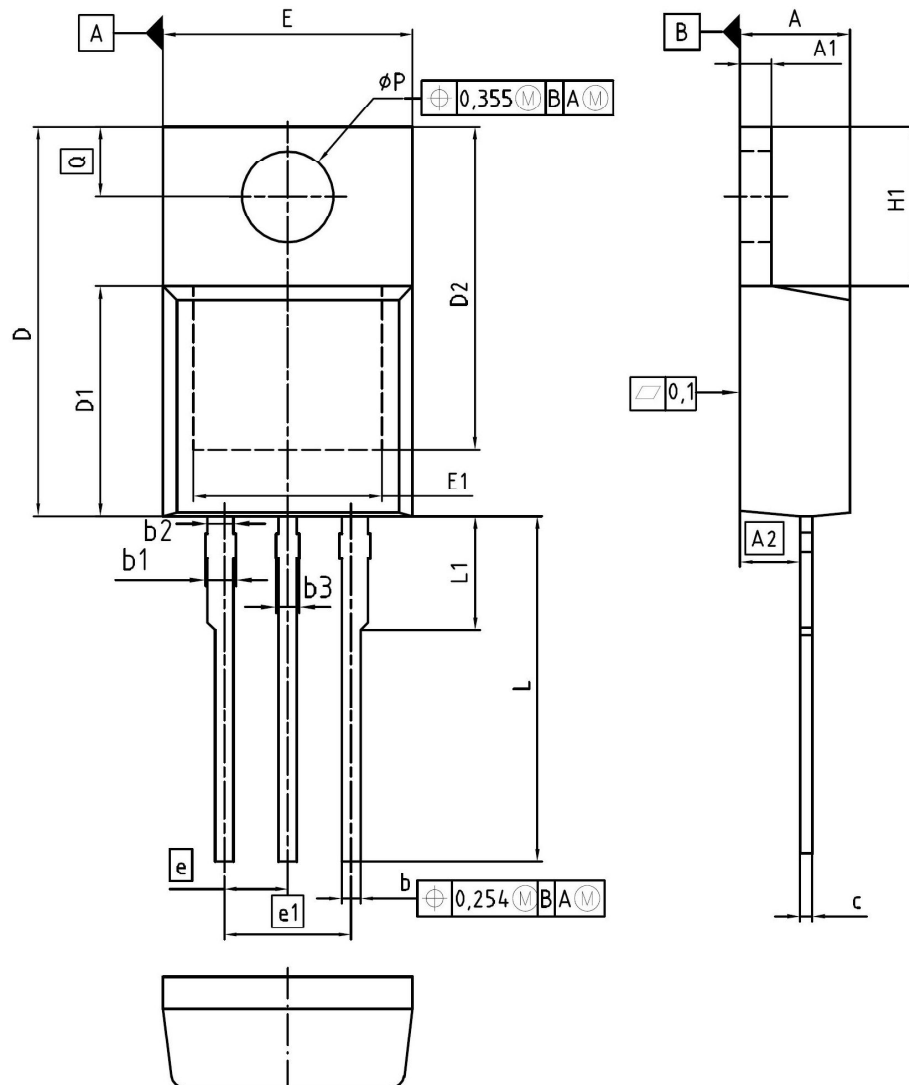
Diagram 15: Drain-source breakdown voltage


 $V_{BR(DSS)}=f(T_J); I_D=1\ \text{mA}$

Gate charge waveforms



6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
ØP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

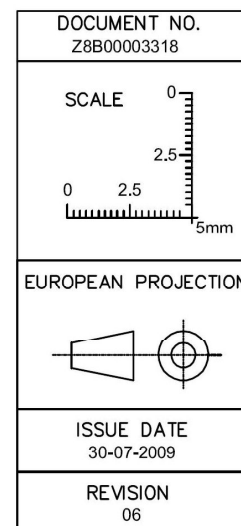


Figure 1 Outline PG-TO220-3, dimensions in mm/inches

Revision History

IPP410N30N

Revision: 2014-12-27, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-12-27	Release of final version

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