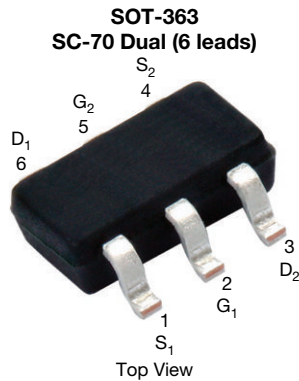


Dual N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A)	Q _g (nC) TYP.
60	1.4 at V _{GS} = 10 V	0.37	0.47
	3 at V _{GS} = 4.5 V	0.25	



Marking Code: PD

Ordering Information:

Si1926DL-T1-E3 (Lead (Pb)-free)

Si1926DL-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

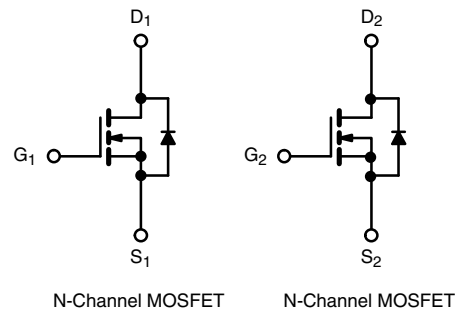
- TrenchFET® power MOSFET
- 100 % R_g tested
- ESD protected: 1800 V
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



**RoHS
COMPLIANT**
HALOGEN
FREE
Available

APPLICATIONS

- Low power load switch



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	60	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	0.37
		T _C = 70 °C	0.30
		T _A = 25 °C	0.34 ^{b, c}
		T _A = 70 °C	0.27 ^{b, c}
Pulsed Drain Current	I _{DM}	0.65	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	0.25 ^{b, c}
Maximum Power Dissipation	P _D	T _C = 25 °C	0.51
		T _C = 70 °C	0.33
		T _A = 25 °C	0.30 ^{b, c}
		T _A = 70 °C	0.20 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient ^{b, d}	R _{thJA}	360	415	°C/W
Maximum Junction-to-Foot (Drain)	R _{thJF}	300	350	

Notes

- Based on T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- Maximum under steady state conditions is 400 °C/W.



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	60	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	56.7	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-	-3	-	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1	-	2.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 10\text{ V}$	-	-	± 150	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 60\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 85\text{ }^\circ\text{C}$	-	-	10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 10\text{ V}$, $V_{GS} = 4.5\text{ V}$	0.50	-	-	A
		$V_{DS} \geq 7.5\text{ V}$, $V_{GS} = 10\text{ V}$	0.65	-	-	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 0.34\text{ A}$	-	-	1.4	Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 0.23\text{ A}$	-	-	3	
Forward Transconductance	g_{fs}	$V_{DS} = 30\text{ V}$, $I_D = 0.2\text{ A}$	-	159	-	ms
Dynamic ^b						
Input Capacitance	C_{iss}	$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	-	18.5	-	μF
Output Capacitance	C_{oss}		-	7.5	-	
Reverse Transfer Capacitance	C_{rss}		-	4.2	-	
Total Gate Charge	Q_g	$V_{DS} = 30\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 0.34\text{ A}$	-	0.9	1.4	nC
		$V_{DS} = 30\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 0.34\text{ A}$	-	0.5	0.75	
Gate-Source Charge	Q_{gs}		-	0.2	-	
Gate-Drain Charge	Q_{gd}		-	0.15	-	
Gate Resistance	R_g	$f = 1\text{ MHz}$	-	160	240	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}$, $R_L = 100\text{ }\Omega$, $I_D \equiv 0.3\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$	-	6.5	10	ns
Rise Time	t_r		-	12	18	
Turn-Off Delay Time	$t_{d(off)}$		-	13	22	
Fall Time	t_f		-	14	21	
Drain-Source Body Diode Characteristics						
Continuous Sorce-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	-	-	0.43	A
Pulse Diode Forward Current ^a	I_{SM}		-	-	0.65	
Body Diode Voltage	V_{SD}	$I_S = 0.3\text{ A}$	-	0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 0.6\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	16.5	25	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	13	20	nC
Reverse Recovery Fall Time	t_a		-	13.5	-	ns
Reverse Recovery Rise Time	t_b		-	3	-	

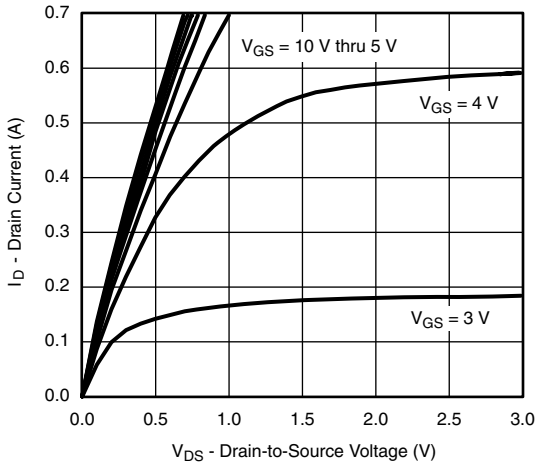
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

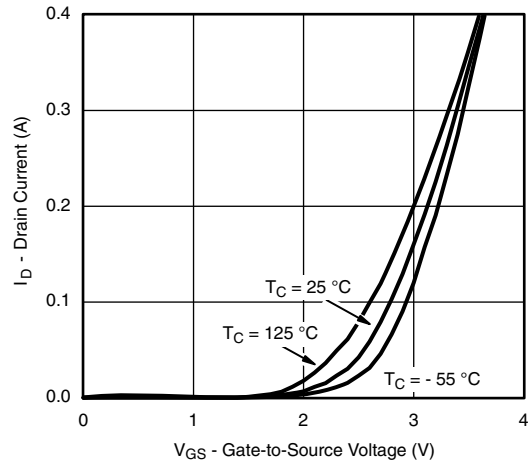
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



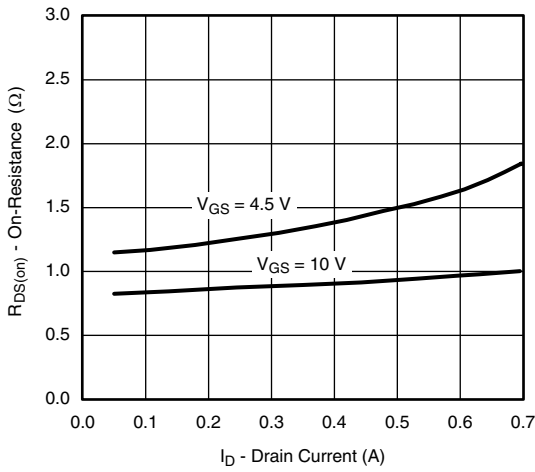
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



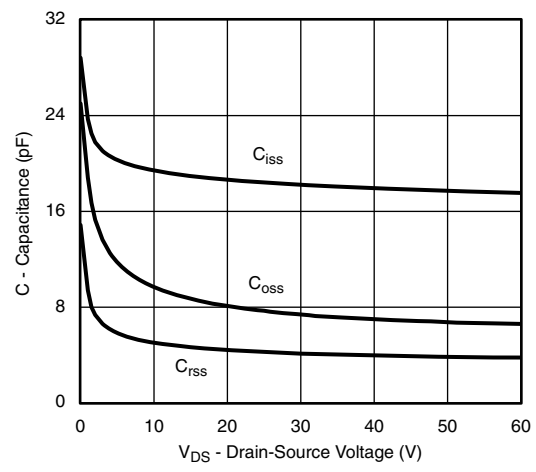
Output Characteristics



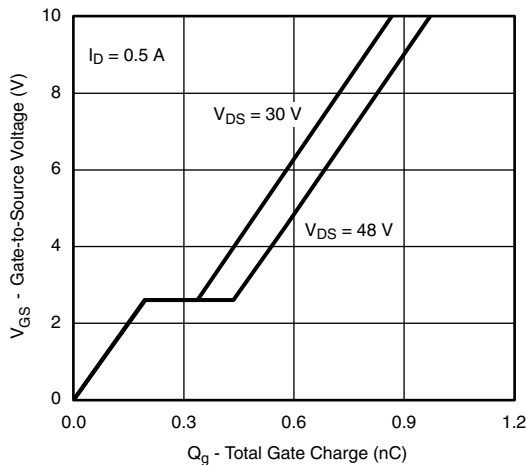
Transfer Characteristics Curves vs. Temperature



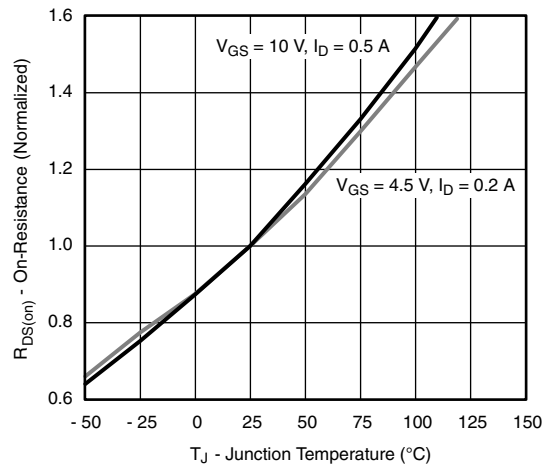
On-Resistance vs. Drain Current



Capacitance



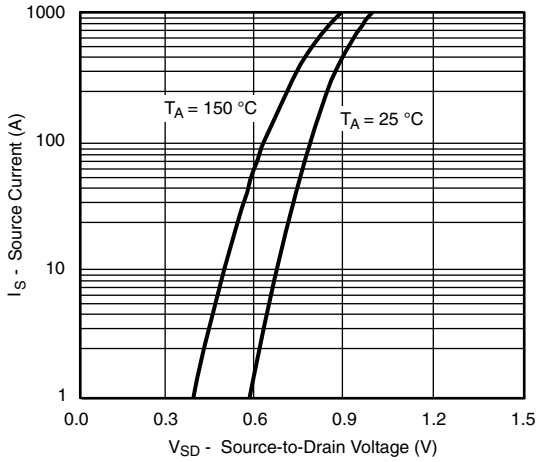
Gate Charge



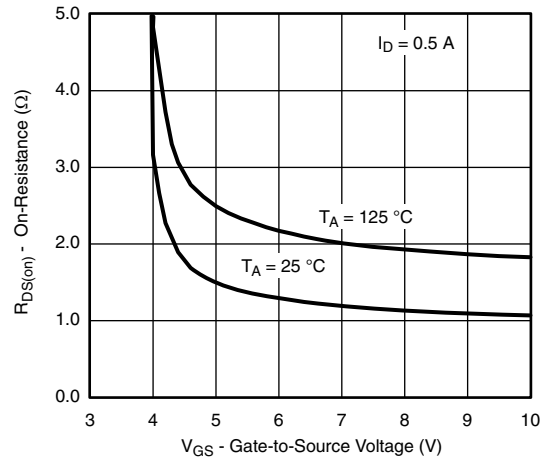
On-Resistance vs. Junction Temperature



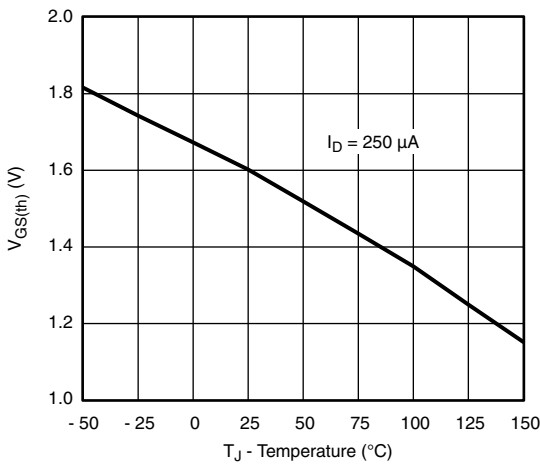
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



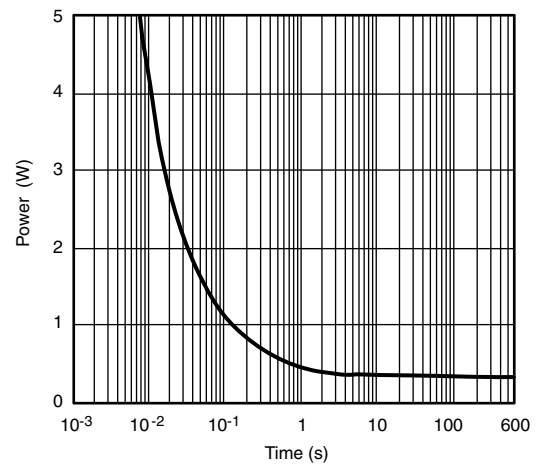
Source-Drain Diode Forward Voltage



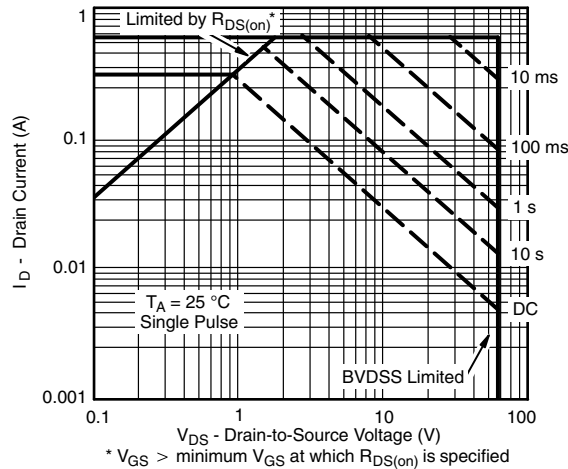
R_{DS(on)} vs. V_{GS} vs. Temperature



Threshold Voltage



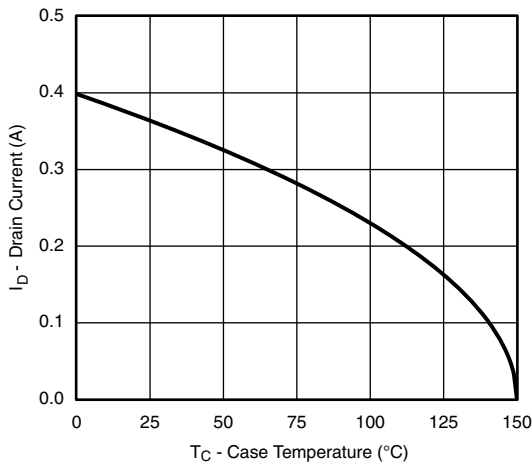
Single Pulse Power



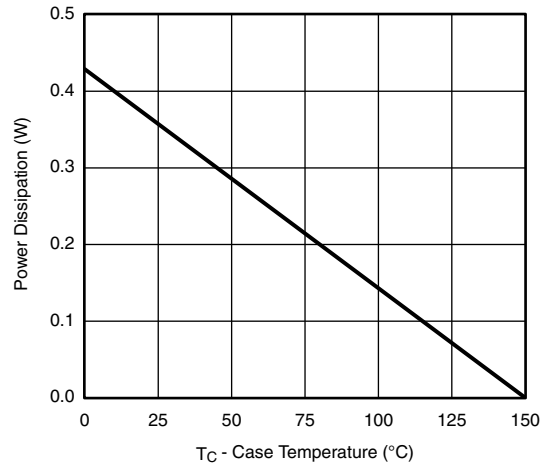
Safe Operating Area



TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Current Derating ^a



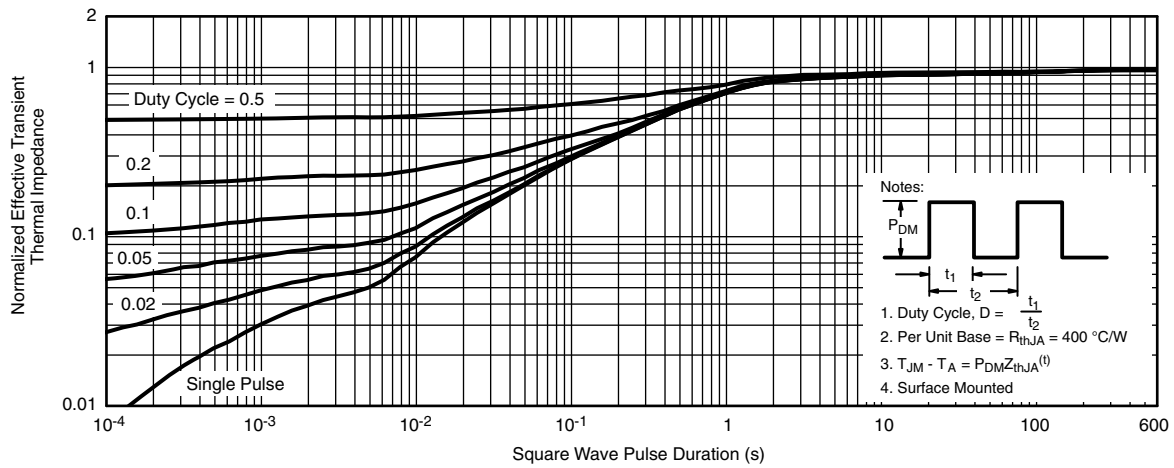
Power Derating

Note

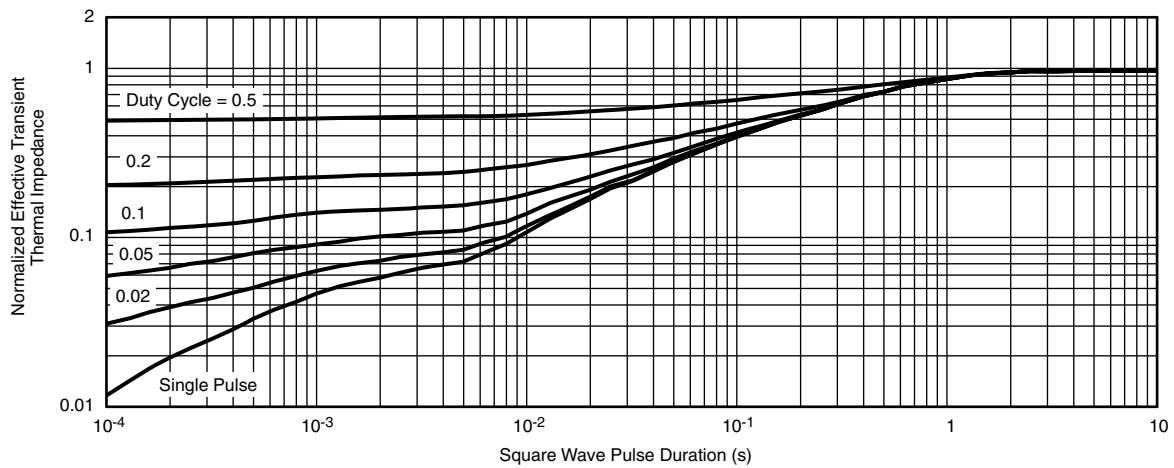
- a. The power dissipation P_D is based on $T_{J(max.)} = 150\text{ }^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

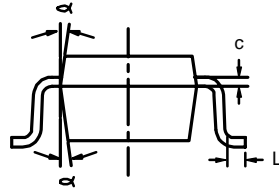
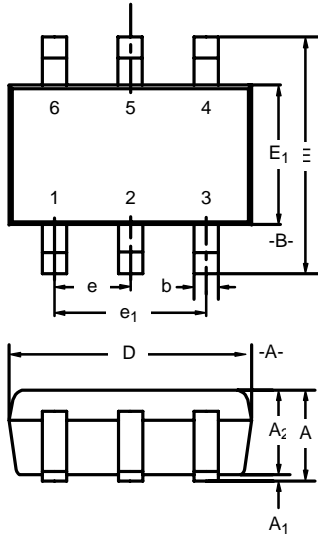


Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73684.

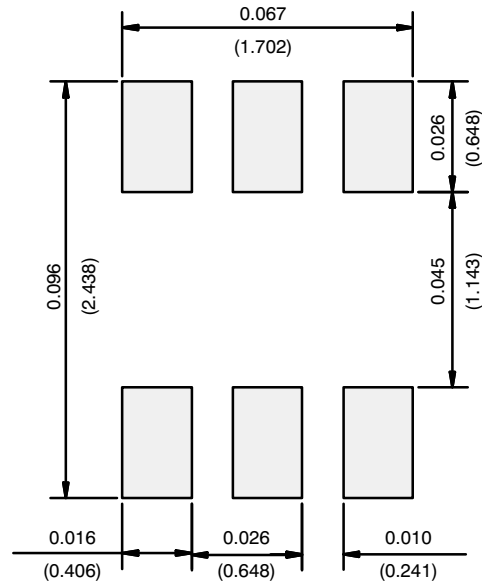


SC-70: 6-LEADS



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	-	1.10	0.035	-	0.043
A ₁	-	-	0.10	-	-	0.004
A ₂	0.80	-	1.00	0.031	-	0.039
b	0.15	-	0.30	0.006	-	0.012
c	0.10	-	0.25	0.004	-	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E ₁	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e ₁	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		
ECN: S-03946—Rev. B, 09-Jul-01						
DWG: 5550						

RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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