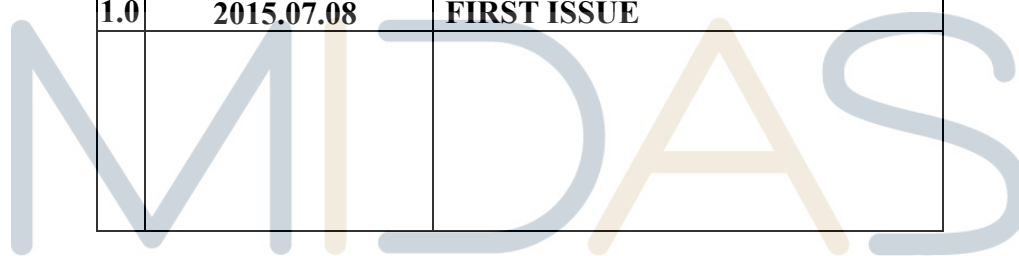


Specification		
Part Number:	MCT024N0CW240320PMLIPS	
Version:	1	
Date:	08/07/2015	
Revision		
1.0	2015.07.08	FIRST ISSUE



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Display Size	2.4"
Resolution	240 x 320
VGA Size	QVGA
Orientation	Portrait
Appearance	RGB
Logic Voltage	3.3V
Interface	Parallel
Brightness	450 cd/m ²
Touchscreen	Capacitive
Module Size W x H x D	48.72 x 70.26 x 3.88 mm
Operating Temperature	-20°C ~ +70°C
Pin Out	45 – Way



Contents

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General Description

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 2.4'TFT-LCD contains 240*320 pixels, and can display up to 65K/262K colors.

* Features

- Low Input Voltage: 3.3V (TYP)
- Display Colors of TFT LCD: 65K/262K colors
- TFT Interface: 8/9/16/18BIT 8080 MCU interface
3/4-wire serial interface;
16/18BIT RGB.
- CTP Interface: I2C

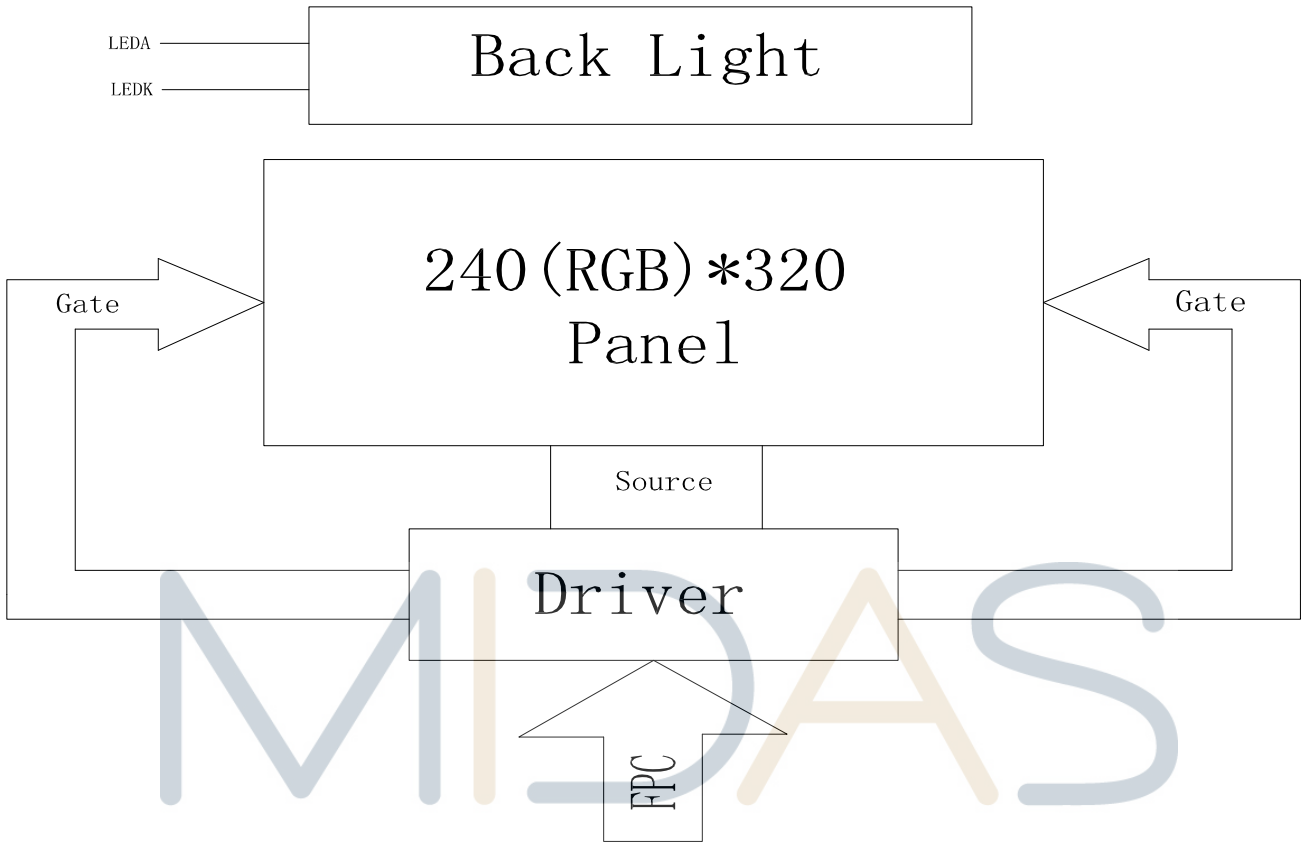
General Information Items	Specification	Unit	Note
	Main Panel		
TFT Display area(AA)	36.72(H)* 48.96 (V) (2.4inch)	mm	-
CTP View area	37.72(H)* 49.96 (V)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	240(RGB)*320	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.153(H)*0.153(V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	ST7789V	-	-
CTP Driver IC	FT6236	-	-
Touch mode	Single point and Gestures	-	-
Display mode	Transmissive/Normally Black	-	-
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		48.72		mm	-
	Vertical(V)		70.26		mm	-
	Depth(D)		3.88		mm	-

Weight		TBD		g	-
--------	--	-----	--	---	---

1. Block Diagram



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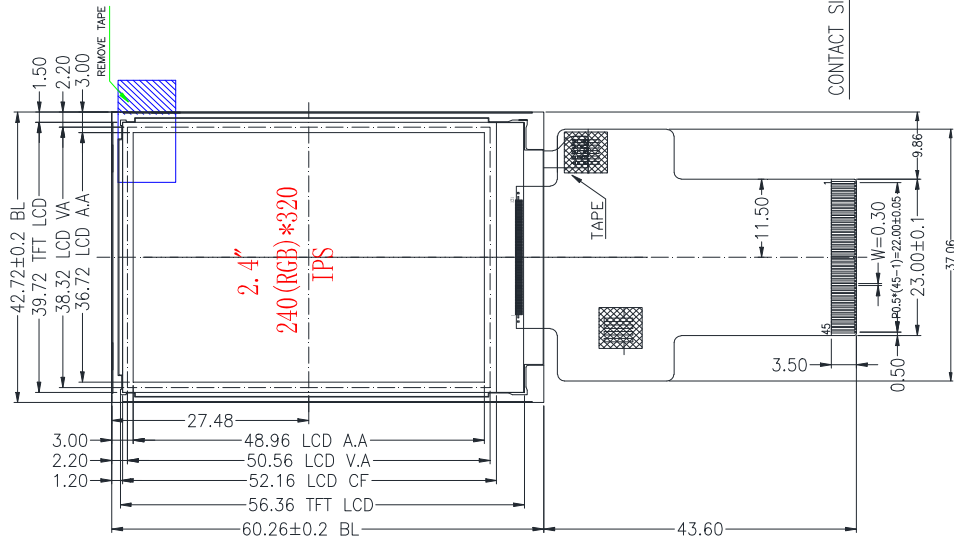


2. Outline dimension

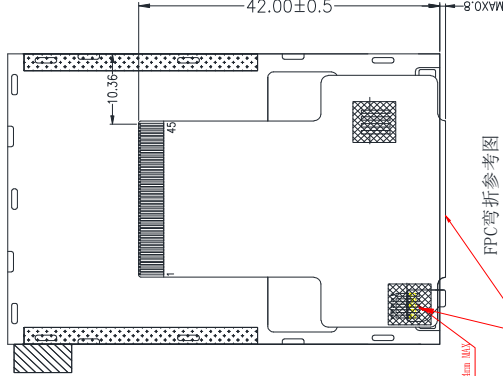
2.1 LCM

注：上机壳开窗小于LCD/CF 0.3mm以上，
LCD VA为镜片开窗参考尺寸。

2.1±0.1(不包括双面胶)

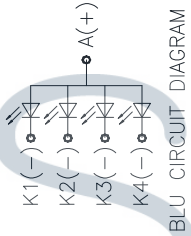


Pin Name	NO.
GND	1
VCI	2
VCI	3
IM2	4
IM2	5
IM0	6
RESET	7
CS	8
WR(SPI-CLK)	9
WR(SPI-AS)	10
RD	11
VSYNC	12
HSYNC	13
ENABLE	14
DOTCLK	15
SDA	16
SCL	17
DB0	18
DB1	19
DB2	20
DB3	21
DB4	22
DB5	23
DB6	24
DB7	25
DB8	26
DB9	27
DB10	28
DB11	29
DB12	30
DB13	31
DB14	32
DB15	33
DB16	34
DB17	35
SDO	36
LEDA	37
LEDA	38
LEDA	39
LEDA	40
YUNCI	41
YUNCI	42
XUNCI	43
YUNCI	44
GND	45



DB Pin in use	Interface type
DB7-DB0	DB1 Tyla 8-bit interface
DB15-DB0	DB1 Tyla 16-bit interface
DB8-DB0	DB1 Tyla 16-bit interface
DB17-DB0	DB1 Tyla 16-bit interface
SDA SCL CS	S-Data 8 BIT data serial interface
SDA SCL CS KS	S-Data 8 BIT data serial interface

NOTE:
1. If not use PIN, fix to the GND, 10VCC or NC.
2. If use RGB mode must select serial interface

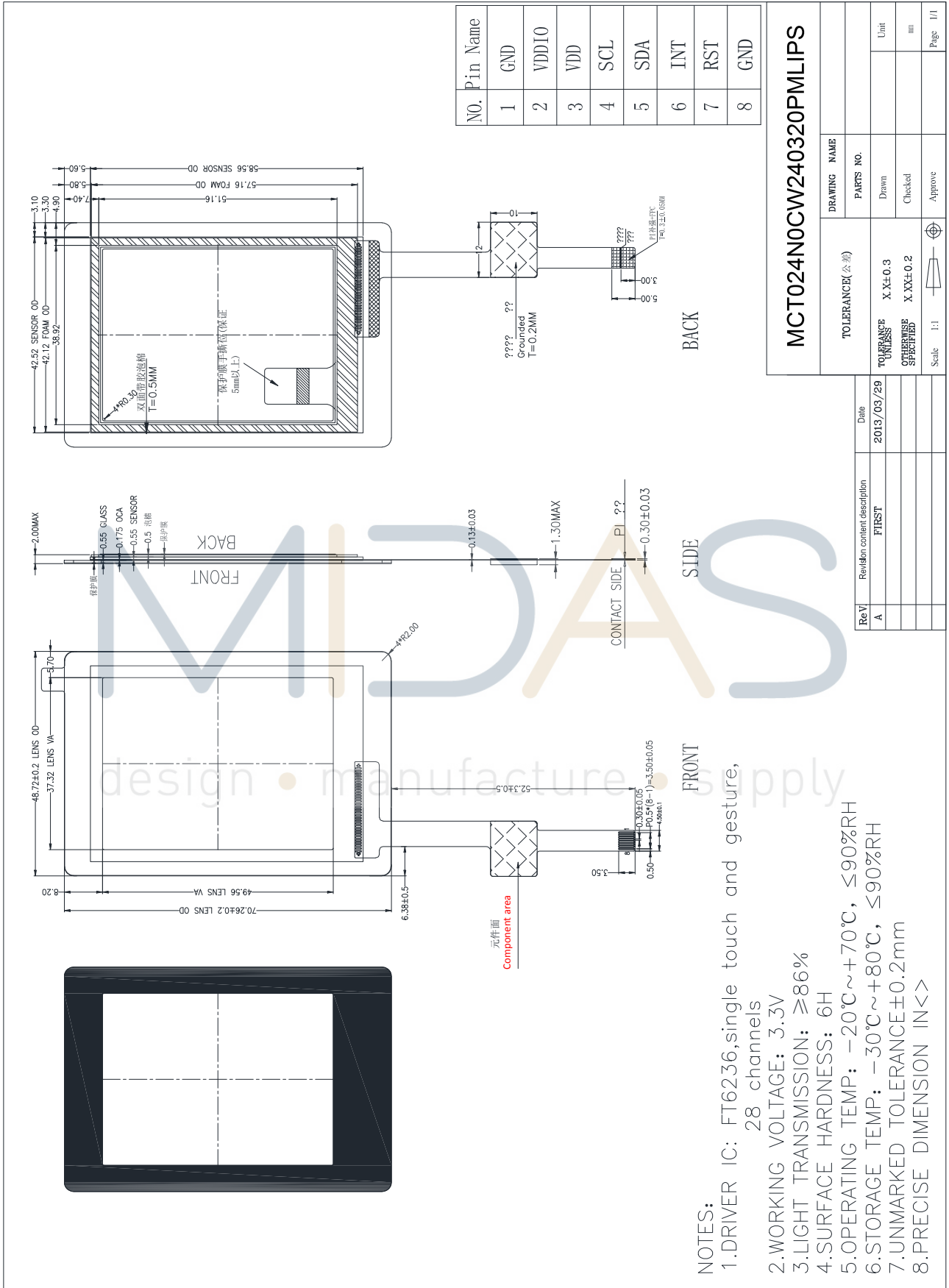


MCT024N0CW240320PMLIPS	
TOLERANCE(公差)	PARTS NO.
UNIT	Drawn
QUANTITY	Checked
SPECIFIED	Approve
Scale 1:1	Page 1/1

Rev	Revision content description	Date
A	FIRST	2014/06/24

- NOTES:
1. DISPLAY TYPE: 2.4", TFT-LCD, 65K/262K COLORS
 2. DISPLAY MODE: IPS NORMALLY BLACK
 3. VIEWING DIRECTION: ALL
 4. DRIVER IC: ST7789V (COG)
 5. VCI: 3.3V
 6. OPERATING TEMP: -20°C TO 70°C
STORAGE TEMP: -30°C TO 80°C
 7. BACK LIGHT: LED WHITE, 4 LED, 80mA, 3.2±0.3V
 8. RoHS COMPLIANT.

2.2 CTP



2.3 LCM+CTP

NO.	TFT Pin Name
1	GND
2	VCI
3	VCI
4	IN2
5	IN1
6	IND
7	RESET
8	CS
9	BL (S1+~2+)
10	VSPHWS2
11	RD
12	VSYNC
13	HSYNC
14	ENABLE
15	DOTCLK
16	SDA
17	SDB
18	DB01
19	DB02
20	DB03
21	DB04
22	DB05
23	DB06
24	DB07
25	DB08
26	DB09
27	DB10
28	DB11
29	DB12
30	DB13
31	DB14
32	DB15
33	DB16
34	DB17
35	S00
36	LEDA
37	LEDA1
38	LEDA2
39	LEDA3
40	LEDA4
41	XRND1
42	XRND2
43	XRND3
44	XRND4
45	GND

NO.	CTP Pin Name
1	GND
2	VDD
3	VDD
4	SCL
5	SDA
6	RST
7	RST
8	GND

MCT024N0CW240320PMLIPS

TOLEFRANCE(公差)

PARTS NO. Drawn
Checked
Approve

TOLERANCE UNLESS OTHERWISE SPECIFIED X.X±0.3
X.XX±0.2

Scale 1:1

Revision content description

Rev	Revision description	Date
A	FIRST	2019/05/29

BLU CIRCUIT DIAGRAM

Pin	Pin in use	Interface type
0	0	DB1 Pin 0 interface
0	0	DB7~DB0
0	1	DB1 Pin 1 interface
0	1	DB15~DB0
0	1	DB7~DB0
0	1	DB1 Pin 0 interface
0	1	DB1 Pin 0 interface
0	1	DB1 Pin 0 interface
1	0	4 wire 8 BIT data serial interface
1	0	SIM SCL CS RS
1	1	5 wire 8 BIT data serial interface
1	1	SIM SCL CS RS

NOTE:
 1. If not use PIN, fix to the GND, I0VCC or NC.
 2. If use RGB mode must select serial interface

NOTES:

- DISPLAY TYPE: 2.4", TFT-LCD, 65K/262K COLORS
- DISPLAY MODE: IPS NORMALLY BLACK
- VIEWING DIRECTION: ALL
- TFT DRIVER IC: ST1789V (COG)
- CTP DRIVER IC: FT6236
- VCI: 3.3V(TFT)
- VDD: 3.3V(CTP)
- CTP SURFACE HARDNESS: 6H
- OPERATING TEMP: -20°C TO 70°C
- STORAGE TEMP: -30°C TO 80°C
- TFT BACK LIGHT: LED WHITE, 4 LED, 80mA, 3.2±0.3V
- RoHS COMPLIANT.

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3. Input terminal Pin Assignment

3.1 TFT

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	VCI	Supply voltage(3.3V).	P
3	VCI	Supply voltage(3.3V).	P
4	IM2	MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface. Fix this pin at VCI and GND.	I
5	IM1		I
6	IM0		I
7	RESET	This signal will reset the device and must be applied to properly initialize the chip.	I
8	CS	Chip select input pin ("Low" enable). fix this pin at VCI or GND when not in use.	I
9	DC(SCL)	This pin is used to select "Data or Command" in the parallel interface. When D/CX = '1', data is selected. When D/CX = '0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. fix this pin at VCI or GND when not in use.	I
10	WR(SPI-RS)	The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VCI or GND when not in use.	I
11	RD	Serves as a read signal and MCU read data at the rising edge. fix this pin at VCI or GND when not in use.	I
12	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
13	HSYNC	Line synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
14	ENABLE	Data enable signal for RGB interface operation.	I

		fix this pin at VCI or GND when not in use.	
15	DOTCLK	Dot clock signal for RGB interface operation. Fix this pin at VCI or GND when not in use.	I
16	SDA	Serial input signal. The data is latched on the rising edge of the SCL signal. fix this pin at VCI or GND when not in use.	I
17-34	DB0-DB17	18-bit parallel bi-directional data bus for MCU system and RGB interface mode . Fix to GND level when not in use	I/O
35	SDO	SPI interface output pin. -The data is output on the falling edge of the SCL signal. -If not used, let this pin open.	O
36	LEDA	Anode pin of backlight	P
37	LEDK1	Cathode pin OF backlight	P
38	LEDK2	Cathode pin OF backlight	P
39	LEDK3	Cathode pin OF backlight	P
40	LEDK4	Cathode pin OF backlight	P
41	XR	Touch panel Right Glass Terminal	A/D
42	YD	Touch panel Bottom Film Terminal	A/D
43	XL	Touch panel LIFT Glass Terminal	A/D
44	YU	Touch panel Top Film Terminal	A/D
45	GND	Ground.	P



3.2 CTP

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	VDDIO	I/O power supply voltage.	P
3	VDD	Supply voltage.	P
4	SCL	I2C clock input.	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host.	I
7	RST	External Reset, Low is active.	I
8	GND	Ground.	P



4. LCD Optical Characteristics

4.1 Optical specification

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (with Polarizer)	T (%)	Normal viewing angle	—	4.65	—	%	Measuring with Polarizer · Reference Only
Transmittance (without Polarizer)	T (%)		—	14.6	—	%	
Contrast	CR		640	800	—	—	(1)(2)
Response time	Rising		T_R	—	16	21	msec
	Falling	T_F	—	19	24		
Color gamut	(%)	$\Theta=0$ Normal viewing angle	—	70	—	%	C-light
Color chromaticity (CIE1931)	White	W_x	0.290	0.310	0.330	—	(1)(4) CF glass
		W_y	0.316	0.336	0.356		
	Red	R_x	0.627	0.647	0.667	—	
		R_y	0.297	0.317	0.337		
	Green	G_x	0.255	0.275	0.295	—	
		G_y	0.562	0.582	0.602		
	Blue	B_x	0.120	0.140	0.160	—	
		B_y	0.068	0.088	0.108		
Viewing angle	Hor.	Θ_L	CR>10	—	80	—	(1)(4) Measuring with Polarizer · Reference Only
		Θ_R		—	80		
	Ver.	Θ_U		—	80		
		Θ_D		—	80		
Optima View Direction	Free						(5)

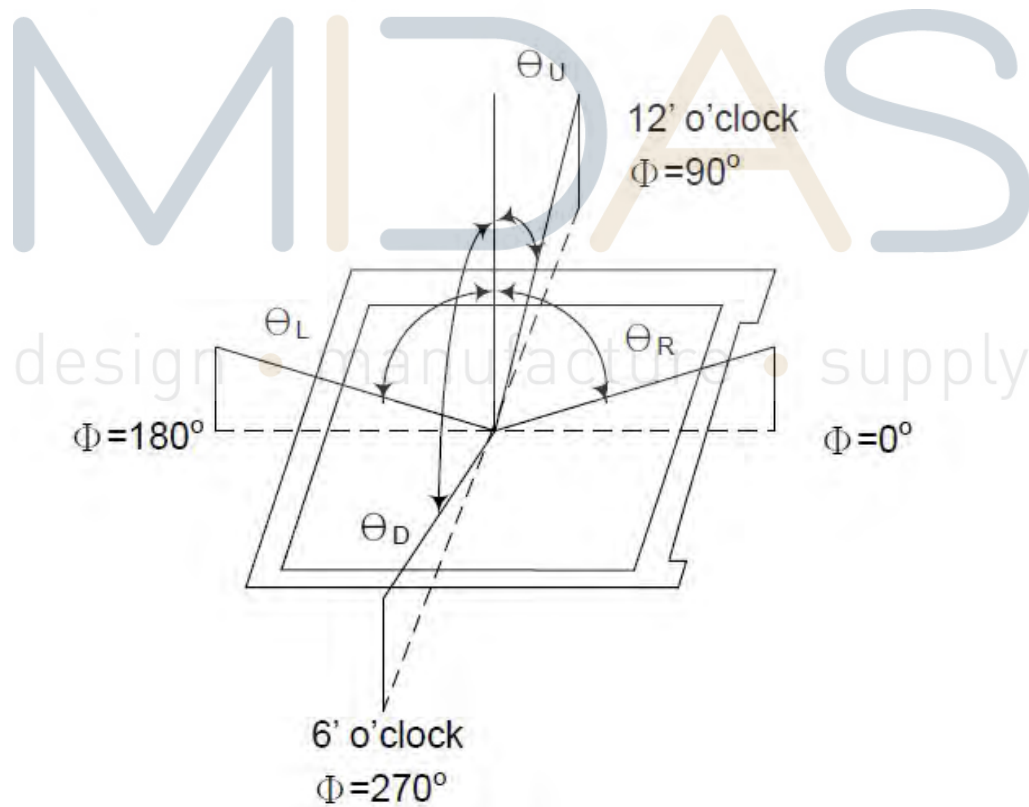
4.2 Measuring Condition

- Measuring surrounding: dark room
- Ambient temperature: $25\pm 2^{\circ}\text{C}$
- 15min. warm-up time.

4.3 Measuring Equipment

Chromaticity and BM-5A for other optical characteristics.

Note (1) Definition of Viewing Angle:



Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

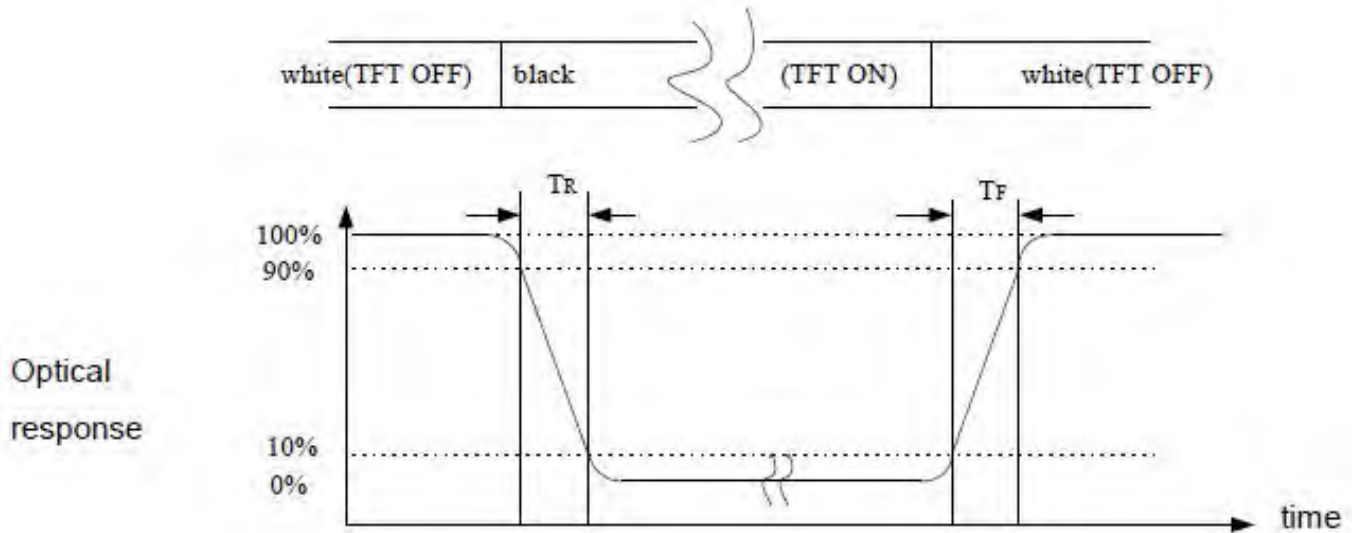
$$\text{CR} = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

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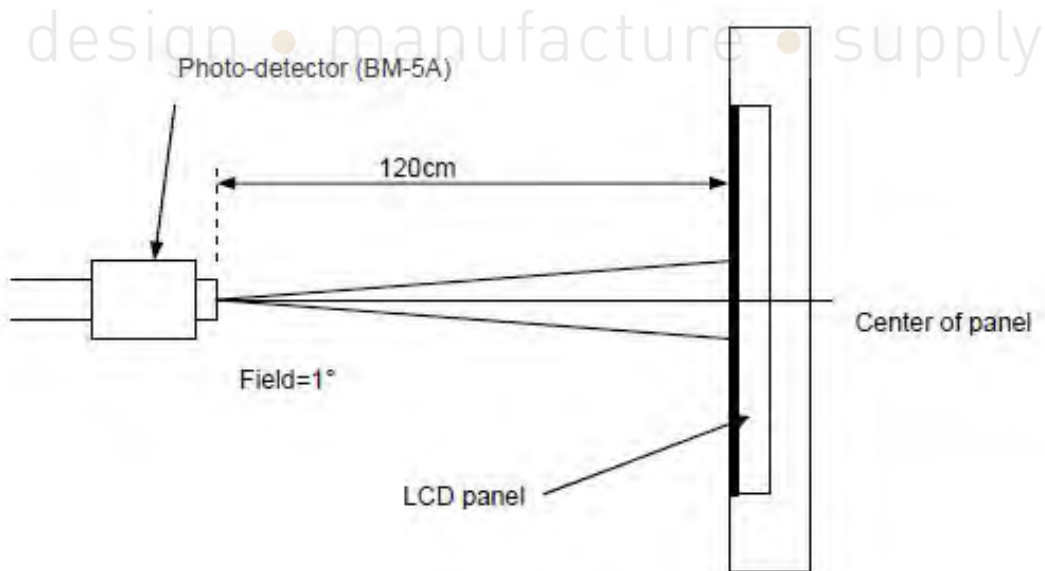
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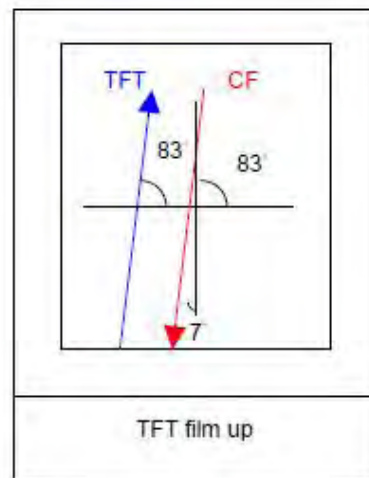
Note (3) Definition of Response Time : Sum of T_R and T_F



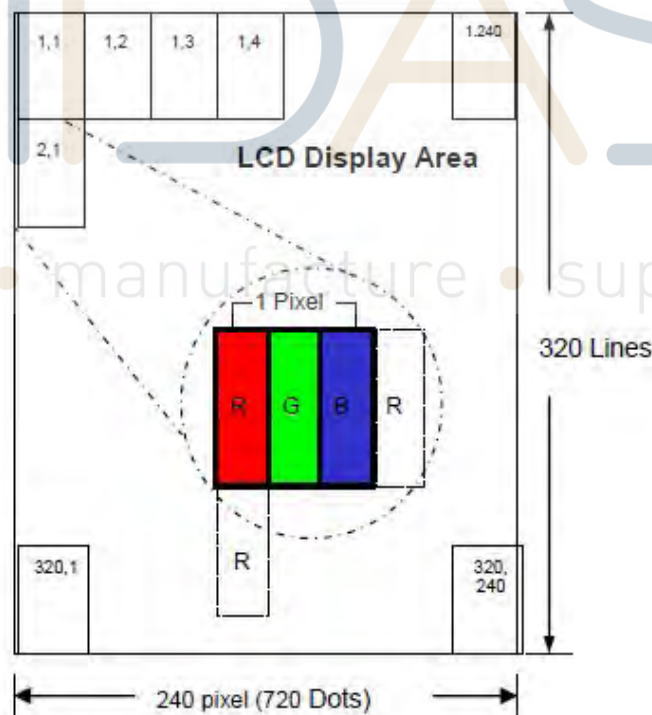
Note (4) Definition of optical measurement setup



Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.



5.0 Pixel Format



5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	-0.3	4.6	V
Digital interface supply Voltage	VDDIO	-0.3	4.6	V
Operating temperature	T _{OP}	-20	+70	°C
Storage temperature	T _{ST}	-30	+80	°C

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	2.4	3.3	4.2	V	
Digital interface supply Voltage	VDDIO	1.65	3.3	4.2	V	
Normal mode Current consumption	IDD	--	8	--	mA	
Level input voltage	V _{IH}	0.7V _{DDIO}		V _{DDIO}	V	
	V _{IL}	GND		0.3V _{DDIO}	V	
Level output voltage	V _{OH}	0.8V _{DDIO}		V _{DDIO}	V	
	V _{OL}	GND		0.2V _{DDIO}	V	

5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 4 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I _F	60	80	--	mA	
Forward Voltage	V _F	--	3.2	--	V	
LCM Luminance	L _V	450		--	cd/m ²	I _F =80mA

LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	

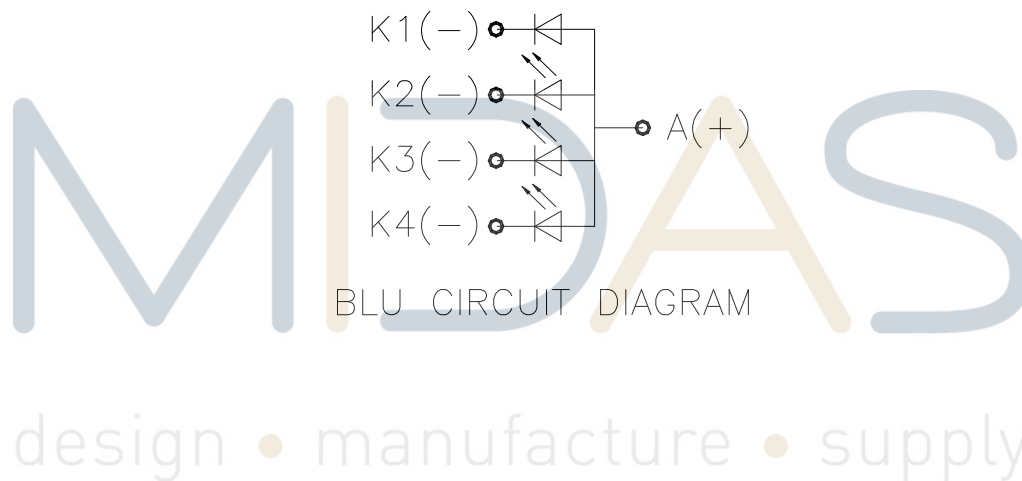
Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition:

$T_a=25\pm 3\text{ }^\circ\text{C}$, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The "LED life time" is defined as the module brightness decrease to 50% original brightness at

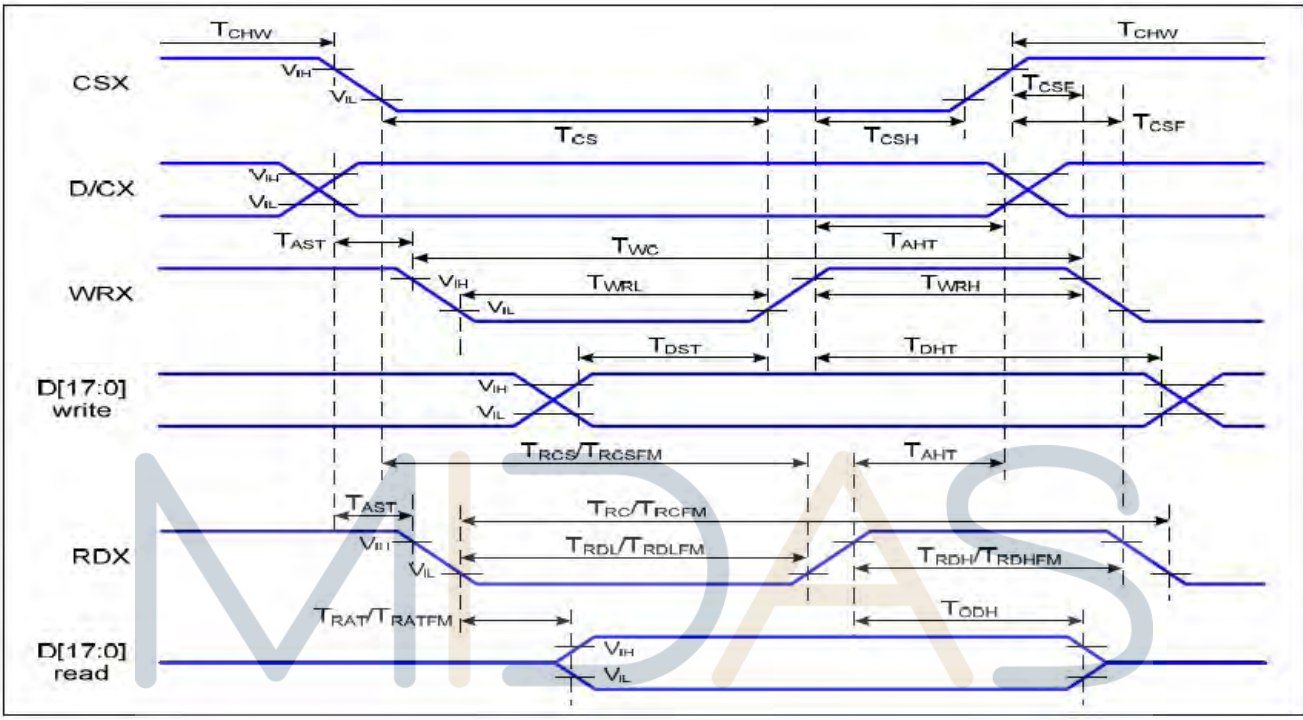
$T_a=25\text{ }^\circ\text{C}$ and $IL=80\text{mA}$. The LED lifetime could be decreased if operating IL is larger than 80mA. The

constant current driving method is suggested.



6. TFT AC Characteristic

6.1 8080 Series MCU Parallel Interface Timing Characteristics: 18/16/9/8-bit Bus



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VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta= -30 to 70 °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T _{AST}	Address setup time	0		ns	-
	T _{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T _{CHW}	Chip select "H" pulse width	0		ns	-
	T _{CS}	Chip select setup time (Write)	15		ns	
	T _{RCS}	Chip select setup time (Read ID)	45		ns	
	T _{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T _{CSF}	Chip select wait time (Write/Read)	10		ns	
	T _{CSH}	Chip select hold time	10		ns	
WRX	T _{WC}	Write cycle	66		ns	
	T _{WRH}	Control pulse "H" duration	15		ns	
	T _{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T _{RC}	Read cycle (ID)	160		ns	When read ID data
	T _{RDH}	Control pulse "H" duration (ID)	90		ns	
	T _{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T _{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T _{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T _{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T _{DST}	Data setup time	10		ns	For CL=30pF

	T _{DHT}	Data hold time	10		ns
	T _{RAT}	Read access time (ID)		40	ns
	T _{RATFM}	Read access time (FM)		340	ns
	T _{ODH}	Output disable time	20	80	ns





Figure 2 Rising and Falling Timing for I/O Signal

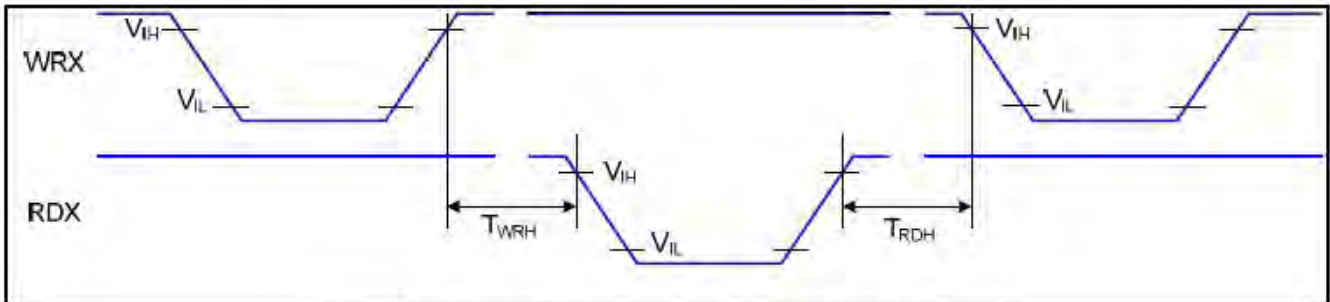
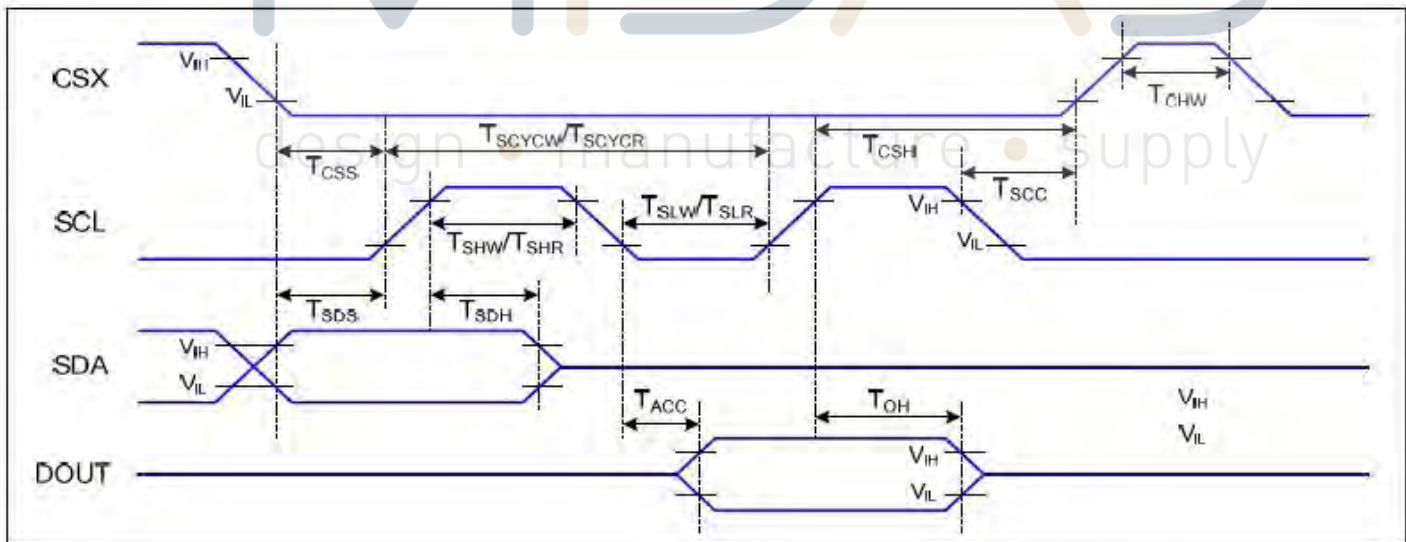


Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (T_r , T_f) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

6.2 Display Serial Interface Timing Characteristics (3-line SPI system)

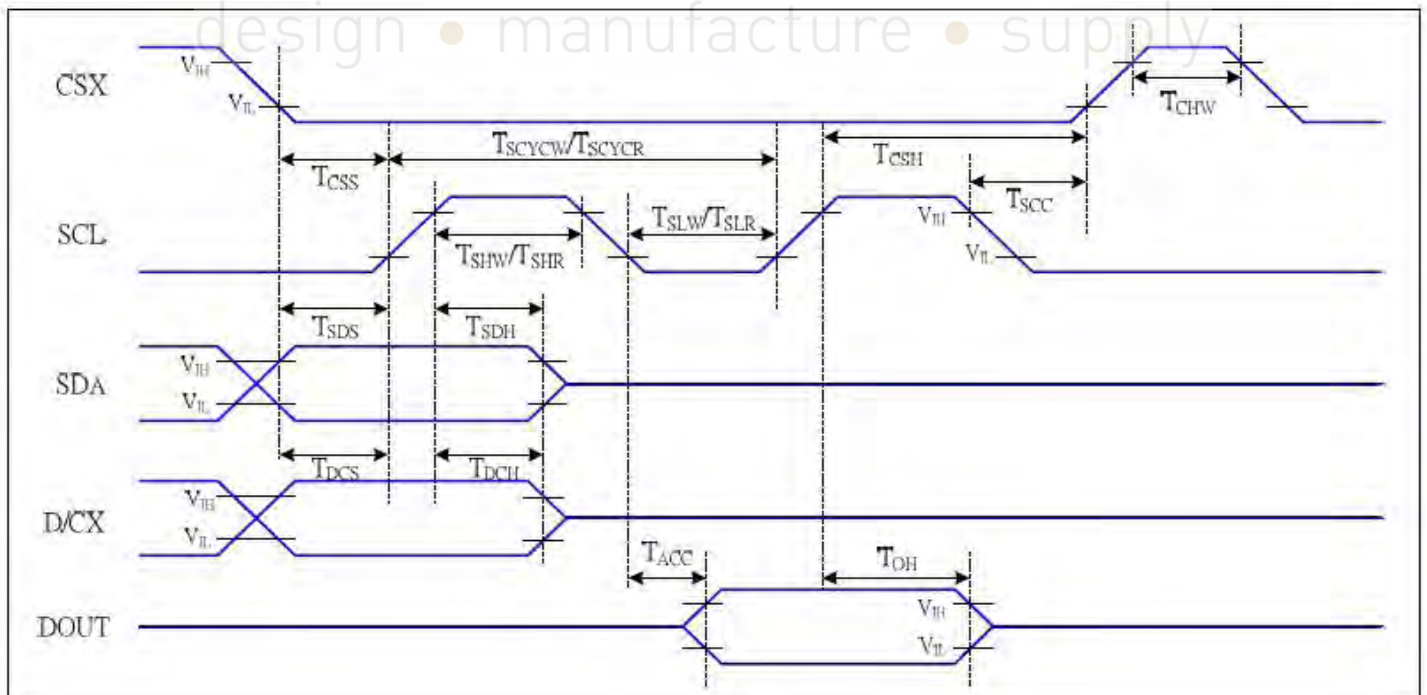


VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

6

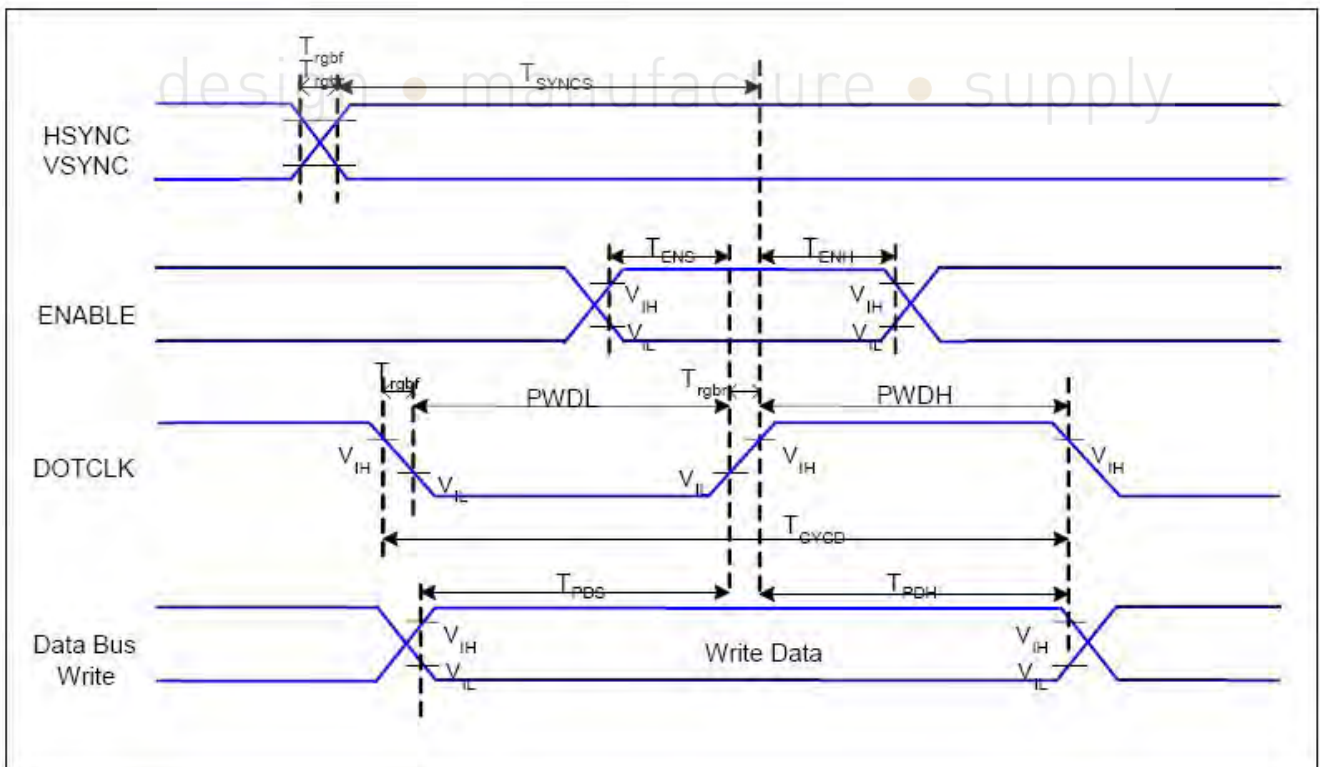
3 Display Serial Interface Timing Characteristics (4-line SPI system)



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 °C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

6.4 Parallel RGB Interface Timing Characteristics



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 °C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T _{SYNCS}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T _{ENS}	Enable Setup Time	25	-	ns	
	T _{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T _{CYCD}	DOTCLK Cycle Time	120	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	20	ns	
DB	T _{PDS}	PD Data Setup Time	50	-	ns	
	T _{PDH}	PD Data Hold Time	50	-	ns	

Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	320	-	Line
Vertical Front Porch	VFP		3	4	-	Line



Setting Example: To set frame frequency to 70Hz:

Internal Clock

Internal Oscillation Clock: 615KHz

DIV[1:0] = 2'b0 (x 1/1)

RTN[4:0] = 5'h1b (27 clocks)

FP = 7'h2 (2 lines), BP = 7'h2 (2 lines), NL = 6'h27 (320 lines)

Frame Rate → 70.30Hz

DOTCLK

HSYNC = 10 CLK

HBP = 20 CLK

HFP = 10 CLK

70Hz x (2 + 320 + 2) lines x (10 + 20 + 240 + 10) clocks = 6.35MHz

DOTCLK frequency = 6.35MHz

6.35 MHz / 615KHz = 10.32 □ Set PCDIV so that PCLK is divided by 10.

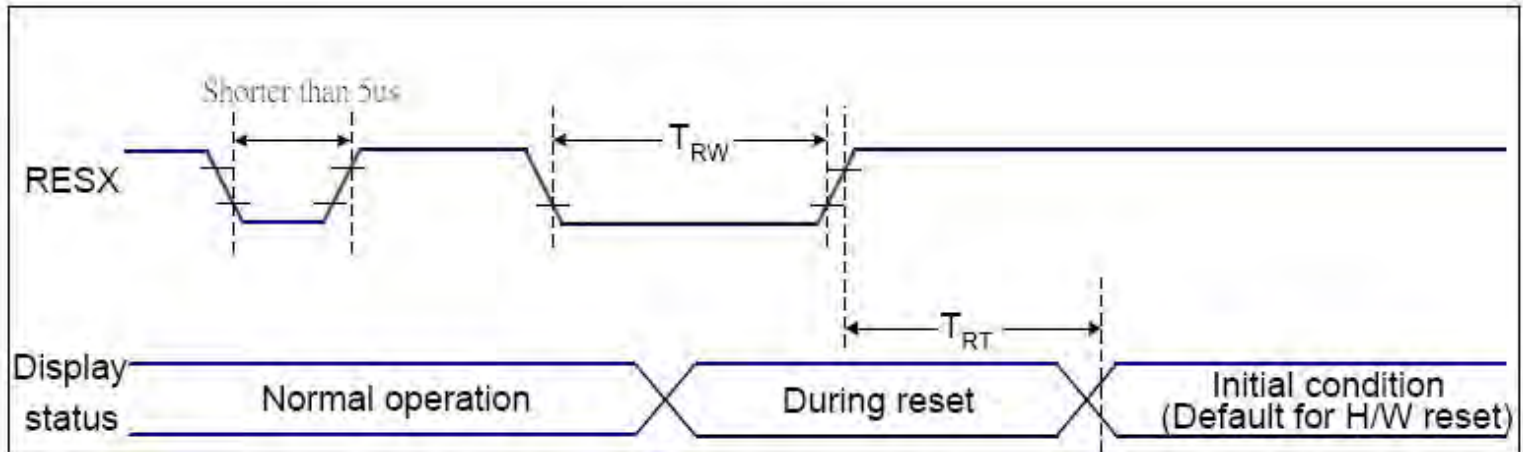
external fosc = 6.35 MHz / 10 = 635KHz

PCDIV = [6.35MHz / 635KHz) / 2] - 1 = 4

PCDIV[5:0] = 6'h04 (10 DOTCLK)

6.5 Reset Timing Characteristics





VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, $T_a=-30 \sim 70$ °C

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
-			120 (Note 1, 6, 7)	ms	

Notes:

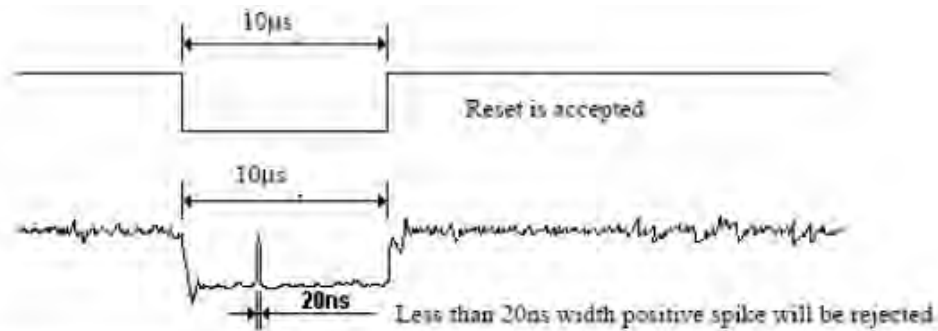
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.



7. CTP Specification

7.1 Electrical Characteristics

7.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	-0.3	3.6	V	1
I/O Digital Voltage	VDDIO	1.8	3.6	V	1
Operating temperature	T _{OP}	-20	+70	°C	-
Storage temperature	T _{ST}	-30	+80	°C	-

NOTES:

1. If used beyond the absolute maximum ratings, FT6236 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

7.1.2 DC Electrical Characteristics (T_a=25°C)



Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Digital supply voltage	VDD		2.8	3.3	3.6	V	
I/O Digital supply voltage	VDDIO		1.8	3.3	3.6	V	
Normal operation mode Current consumption	I_{opr}	VDD=2.8V Ta=25°C MCLK= 17.5Mhz	-	4	-	mA	
Monitor mode Current consumption	I_{mon}		-	1.5	-	mA	
Sleep mode Current consumption	I_{slp}		-	50	-	uA	
Level input voltage	V_{IH}		0.7V _{DDIO}	-	V _{DDIO}	V	
	V_{IL}		-0.3	-	0.3V _{DDIO}	V	
Level output voltage	V_{OH}	$I_{OH}=-0.1mA$	0.7V _{DDIO}	-	-	V	
	V_{OL}	$I_{OH}=0.1mA$	-	-	0.3V _{DDIO}	V	

7.2 AC Characteristics

Table 4-1 AC Characteristics of Oscillators

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
OSC clock 1	fosc1	VDDA= 2.8V; Ta=25°C	34.65	35	35.35	MHz	

Table 4-2 AC Characteristics of sensor

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
Sensor acceptable clock	ftx	VDDA= 2.8V; Ta=25°C	0	100	300	KHz	
Sensor output rise time	T _{txr}	VDDA= 2.8V; Ta=25°C	-	100	-	nS	
Sensor output fall time	T _{txf}	VDDA= 2.8V; Ta=25°C	-	80	-	nS	
Sensor input voltage	Trxi	VDDA= 2.8V; Ta=25°C	-	5	-	V	

7.2.1 I2C Interface

The I2C is always configured in the Slave mode. The data transfer format is shown in Figure4-1:

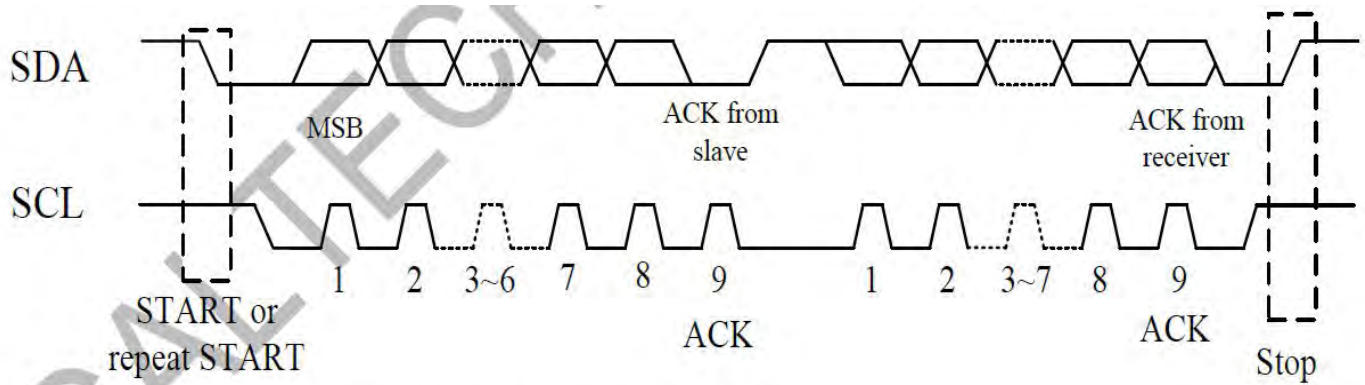


Figure 4-1 I2C Serial Data Transfer Format

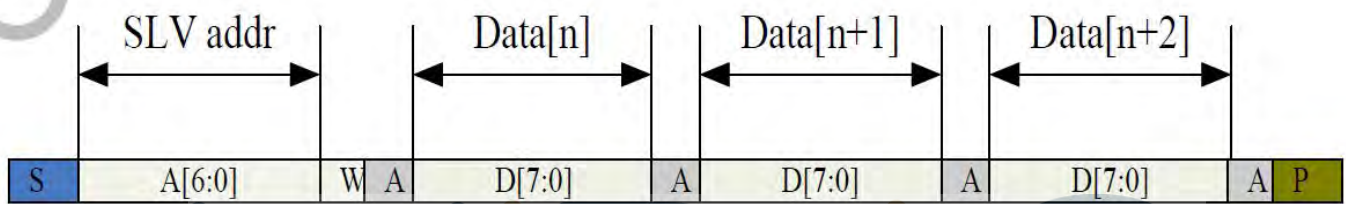


Figure 4-2 I2C master write, slave read

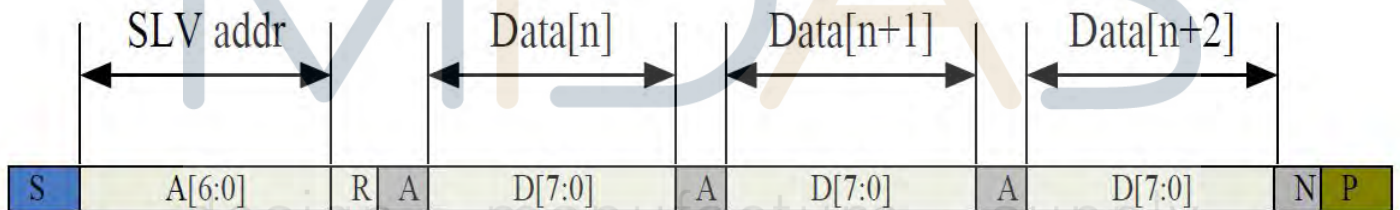


Figure 4-3 I2C master read, slave write

Table4-3 lists the meanings of the mnemonics used in the above figures.

Table 4-3 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0' for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table4-4.

Table 4-4 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	10	400	KHz
Bus free time between a STOP and START condition	4.7	\	us
Hold time (repeated) START condition	4.0	\	us
Data setup time	250	\	ns
Setup time for a repeated START condition	4.7	\	us
Setup Time for STOP condition	4.0	\	us

MIDAS

8. LCD Module Out-Going Quality Level

8.1 VISUAL & FUNCTION INSPECTION STANDARD

8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

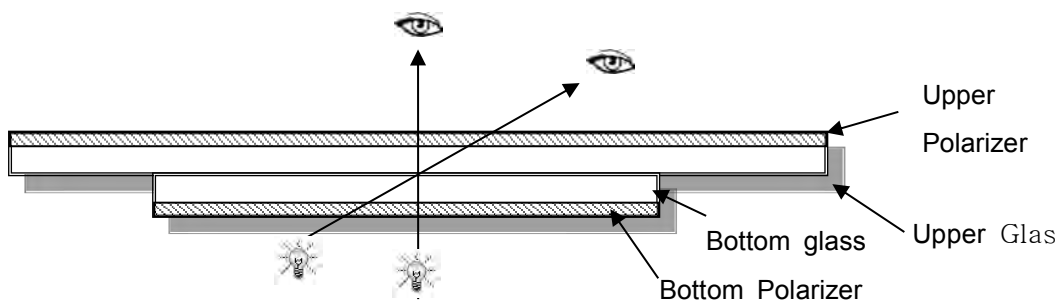
Temperature : $25\pm 5^{\circ}\text{C}$

Humidity : $65\%\pm 10\%\text{RH}$

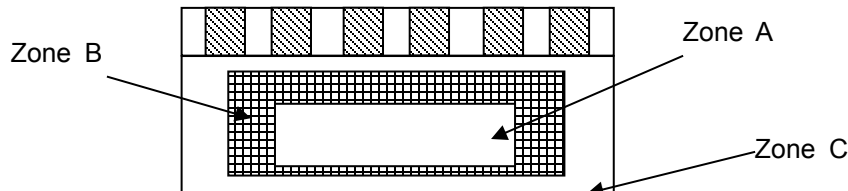
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



8.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

8.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

Major defect	Minor defect
0.65	1.5

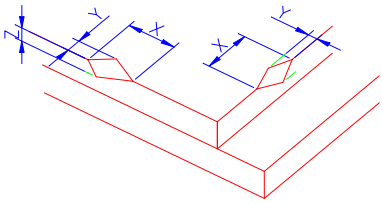
LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	

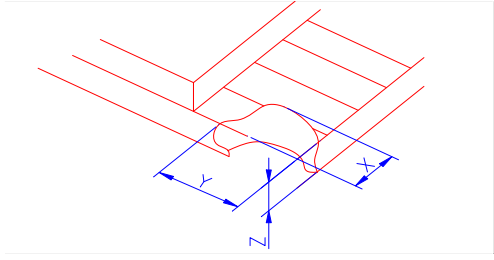
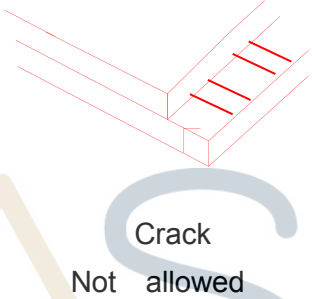
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

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8.1.4 Criteria (Visual)

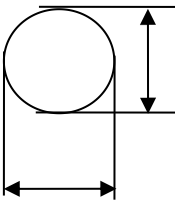
Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken	(1) The edge of LCD broken	 <table border="1" data-bbox="868 1608 1442 1756"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤3.0mm</td> <td><Inner border line of the seal</td> <td>≤T</td> </tr> </tbody> </table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
X	Y	Z						
≤3.0mm	<Inner border line of the seal	≤T						
NOTE: X: Length Y: Width								



<p>Z: Height L: Length of I TO, T: Height of L CD</p>	<p>(2)LCD corner broken</p>	 <table border="1" data-bbox="932 548 1377 647"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td>≤3.0mm</td> <td>≤L</td> <td>≤T</td> </tr> </table>	X	Y	Z	≤3.0mm	≤L	≤T
X	Y	Z						
≤3.0mm	≤L	≤T						
	<p>(3) LCD crack</p>	 <p>Crack Not allowed</p>						

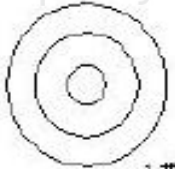
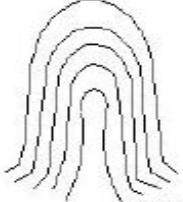
Number	Items	Criteria (mm)
--------	-------	---------------



2.0	<p>Spot defect</p>  <p>$\Phi = (X+Y)/2$</p>	<p>① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain)</p> <table border="1" data-bbox="446 302 1316 660"> <thead> <tr> <th rowspan="2">Zone Size (mm)</th> <th colspan="3">Accept</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.10$</td> <td colspan="3">Ignore</td> </tr> <tr> <td>$0.10 < \Phi \leq 0.20$</td> <td colspan="3">3(distance $\geq 10\text{mm}$)</td> </tr> <tr> <td>$0.20 < \Phi \leq 0.25$</td> <td colspan="3">2</td> </tr> <tr> <td>$\Phi > 0.25$</td> <td colspan="3">0</td> </tr> </tbody> </table> <p>② Dim spot (LCD/TP/Polarizer dim dot, light leakage, dark spot)</p> <table border="1" data-bbox="446 705 1316 1075"> <thead> <tr> <th rowspan="2">Zone Size (mm)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.1$</td> <td colspan="3">Ignore</td> </tr> <tr> <td>$0.10 < \Phi \leq 0.20$</td> <td colspan="3">3(distance $\geq 10\text{mm}$)</td> </tr> <tr> <td>$0.20 < \Phi \leq 0.30$</td> <td colspan="3">2</td> </tr> <tr> <td>$\Phi > 0.30$</td> <td colspan="3">0</td> </tr> </tbody> </table> <p>③ Polarizer accidented spot</p> <table border="1" data-bbox="446 1120 1316 1400"> <thead> <tr> <th rowspan="2">Zone Size (mm)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.2$</td> <td colspan="3">Ignore</td> </tr> <tr> <td>$0.3 < \Phi \leq 0.5$</td> <td colspan="3">2(distance $\geq 10\text{mm}$)</td> </tr> <tr> <td>$\Phi > 0.5$</td> <td colspan="3">0</td> </tr> </tbody> </table>	Zone Size (mm)	Accept			A	B	C	$\Phi \leq 0.10$	Ignore			$0.10 < \Phi \leq 0.20$	3(distance $\geq 10\text{mm}$)			$0.20 < \Phi \leq 0.25$	2			$\Phi > 0.25$	0			Zone Size (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.1$	Ignore			$0.10 < \Phi \leq 0.20$	3(distance $\geq 10\text{mm}$)			$0.20 < \Phi \leq 0.30$	2			$\Phi > 0.30$	0			Zone Size (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.2$	Ignore			$0.3 < \Phi \leq 0.5$	2(distance $\geq 10\text{mm}$)			$\Phi > 0.5$	0		
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$\Phi > 0.5$	0																																																																		
	<p>Line defect (LCD/TP /Polarizer black/white line, scratch, stain)</p>	<table border="1" data-bbox="446 1467 1316 1825"> <thead> <tr> <th rowspan="2">Width(mm)</th> <th rowspan="2">Length(mm)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.03$</td> <td>Ignor</td> <td colspan="3">Ignore</td> </tr> <tr> <td>$0.03 < W \leq 0.05$</td> <td>$L \leq 3.0$</td> <td colspan="3">$N \leq 2$</td> </tr> <tr> <td>$0.05 < W \leq 0.08$</td> <td>$L \leq 2.0$</td> <td colspan="3">$N \leq 2$</td> </tr> <tr> <td>$0.08 < W$</td> <td colspan="4">Define as spot defect</td> </tr> </tbody> </table>	Width(mm)	Length(mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.03$	Ignor	Ignore			$0.03 < W \leq 0.05$	$L \leq 3.0$	$N \leq 2$			$0.05 < W \leq 0.08$	$L \leq 2.0$	$N \leq 2$			$0.08 < W$	Define as spot defect																																								
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$0.08 < W$	Define as spot defect																																																																		



3.0	Polarizer Bubble	<table border="1"> <tr> <th rowspan="2">Zone Size (mm)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> <tr> <td>$\Phi \leq 0.2$</td> <td colspan="3">Ignore</td> </tr> <tr> <td>$0.2 < \Phi \leq 0.4$</td> <td colspan="3">3 (distance ≥ 10)</td> </tr> <tr> <td>$0.4 < \Phi \leq 0.6$</td> <td colspan="3">2</td> </tr> <tr> <td>$0.6 < \Phi$</td> <td colspan="3">0</td> </tr> </table>			Zone Size (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.2$	Ignore			$0.2 < \Phi \leq 0.4$	3 (distance ≥ 10)			$0.4 < \Phi \leq 0.6$	2			$0.6 < \Phi$	0		
		Zone Size (mm)	Acceptable Qty																								
			A	B	C																						
		$\Phi \leq 0.2$	Ignore																								
		$0.2 < \Phi \leq 0.4$	3 (distance ≥ 10)																								
$0.4 < \Phi \leq 0.6$	2																										
$0.6 < \Phi$	0																										
4.0	SMT	According to IPC-A-610C class II standard . Function defect and missing part are major defect ,the others are minor defect.																									

5.0	TP Related	TP bubble/ accident spot	<table border="1"> <tr> <th rowspan="2">Size Φ(mm)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> <tr> <td>$\Phi \leq 0.1$</td> <td colspan="3">Ignore</td> </tr> <tr> <td>$0.1 < \Phi \leq 0.25$</td> <td colspan="3">3 (distance $\geq 10m$)</td> </tr> <tr> <td>$0.25 < \Phi \leq 0.3$</td> <td colspan="3">2</td> </tr> <tr> <td>$0.3 < \Phi$</td> <td colspan="3">0</td> </tr> </table>			Size Φ (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.1$	Ignore			$0.1 < \Phi \leq 0.25$	3 (distance $\geq 10m$)			$0.25 < \Phi \leq 0.3$	2			$0.3 < \Phi$	0		
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$0.25 < \Phi \leq 0.3$	2																											
$0.3 < \Phi$	0																											
Assembly deflection	beyond the edge of backlight $\leq 0.15mm$																											
Newton Ring	<p>Newton Ring area $> 1/3$ TP are a NG</p> <p>Newton Ring area $\leq 1/3$ TP are a OK</p>	 <p>1 规律性</p>	 <p>2 非规律性</p>																									

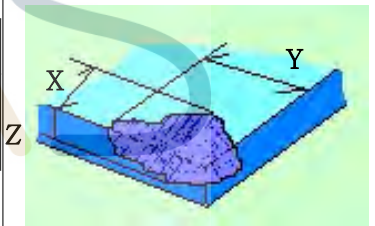




TP corner broken
X : length
Y : width
Z : height

X	Y	Z
$X \leq 3.0\text{mm}$	$Y \leq 3.0\text{mm}$	$Z < \text{LCD thickness}$

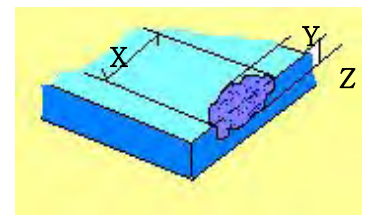
*
Circuitry broken is not allowed.



TP edge broken
X : length
Y : width
Z : height

X	Y	Z
$X \leq 6.0\text{mm}$	$Y \leq 2.0\text{mm}$	$Z < \text{LCD thickness}$

* Circuitry broken is not allowed.



Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed



5	TP no function	Not allowed
---	----------------	-------------

9. Reliability Test Result

9.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20°C, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	70°C90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20°C ↔ 70°C, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80°C, 96HR	3ea	pass	-
Low Temperature Storage test	-30°C, 96HR	3ea	pass	-
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66cm(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

10. Cautions and Handling Precautions

10.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the "Power ON" condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

10.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.



(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

11.Packing

-----TBD-----



design • manufacture • supply

