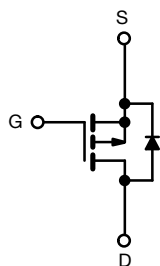
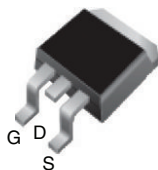


Power MOSFET

D²PAK (TO-263)


P-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V)	-100	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10$ V	0.20
Q_g max. (nC)	61	
Q_{gs} (nC)	14	
Q_{gd} (nC)	29	
Configuration	Single	

FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dV/dt rating
- Repetitive avalanche rated
- P-channel
- 175 °C operating temperature
- Fast Switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details



RoHS*
Available
HALOGEN
FREE
Available

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface-mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHF9540S-GE3	SiHF9540STRL-GE3 ^a
Lead (Pb)-free	IRF9540SPbF	IRF9540STRLPbF ^a

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current ^a	I_{DM}	-72	
Linear Derating Factor		1.0	W/°C
Linear Derating Factor (PCB mount) ^e		0.025	
Single Pulse Avalanche Energy ^b	E_{AS}	640	mJ
Repetitive Avalanche Current ^a	I_{AR}	-19	A
Repetitive Avalanche Energy ^a	E_{AR}	15	mJ
Maximum Power Dissipation	P_D	150	W
Maximum Power Dissipation (PCB mount) ^e		3.7	
Peak Diode Recovery dV/dt ^c	dV/dt	-5.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	°C
Soldering Recommendations (Peak temperature) ^d	For 10 s	300	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = -25$ V, starting $T_J = 25$ °C, $L = 2.7$ mH, $R_g = 25$ Ω , $I_{AS} = -19$ A (see fig. 12)
- $I_{SD} \leq -19$ A, $dI/dt \leq 200$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C
- 1.6 mm from case
- When mounted on 1" square PCB (FR-4 or G-10 material)

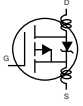
**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB mount) ^a	R _{thJA}	-	-	40	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	-	1.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

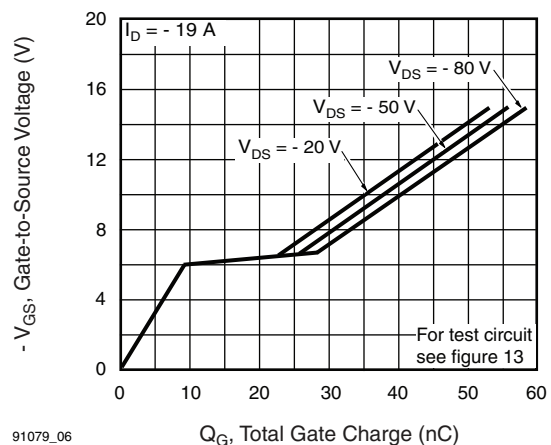
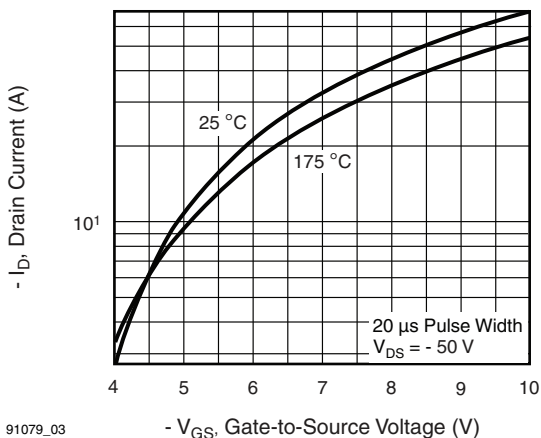
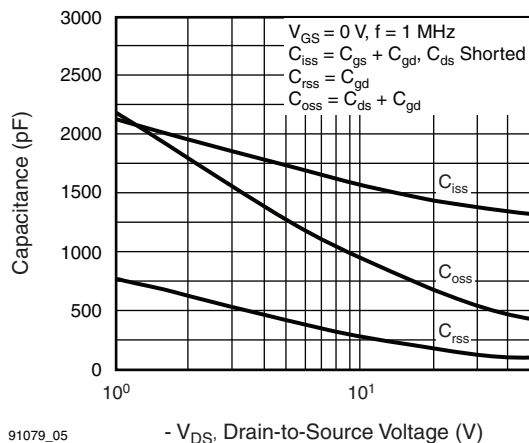
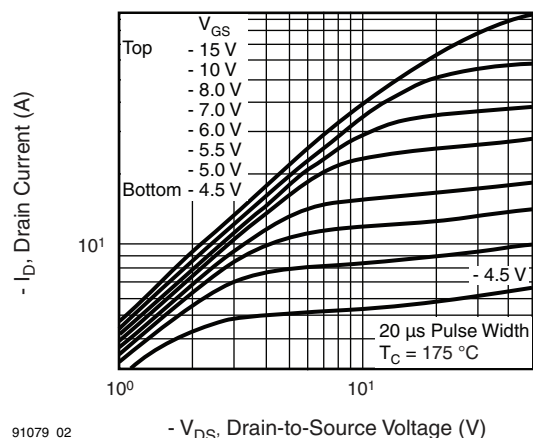
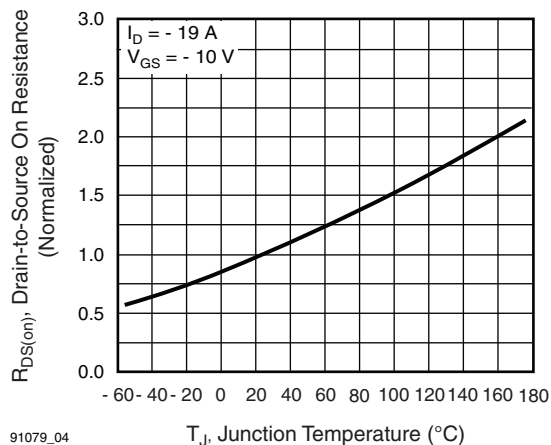
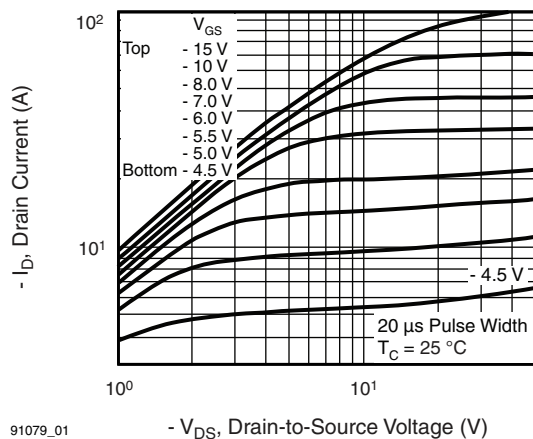
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = -250 μA		-100	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = -1 mA		-	-0.087	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA		-2.0	-	-4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -100 V, V _{GS} = 0 V		-	-	-100	μA
		V _{DS} = -80 V, V _{GS} = 0 V, T _J = 150 °C		-	-	-500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = -10 V	I _D = -11 A ^b	-	-	0.20	Ω
Forward Transconductance	g _{fs}	V _{DS} = -50 V, I _D = -11 A		6.2	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = -25 V, f = 1.0 MHz, see fig. 5		-	1400	-	pF
Output Capacitance	C _{oss}			-	590	-	
Reverse Transfer Capacitance	C _{rss}			-	140	-	
Total Gate Charge	Q _g	V _{GS} = -10 V	I _D = -19 A, V _{DS} = -80 V, see fig. 6 and 13 ^b	-	-	61	nC
Gate-Source Charge	Q _{gs}			-	-	14	
Gate-Drain Charge	Q _{gd}			-	-	29	
Turn-On Delay Time	t _{d(on)}	V _{DD} = -50 V, I _D = -19 A, R _G = 9.1 Ω, R _D = 2.4 Ω, see fig. 10 ^b		-	16	-	ns
Rise Time	t _r			-	73	-	
Turn-Off Delay Time	t _{d(off)}			-	34	-	
Fall Time	t _f			-	57	-	
Gate Input Resistance	R _g	f = 1 MHz, open drain		0.3	-	1.6	Ω
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	-19	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	-72	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = -19 A, V _{GS} = 0 V ^b		-	-	-5.0	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = -19 A, dI/dt = 100 A/μs ^b		-	130	260	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.35	0.70	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

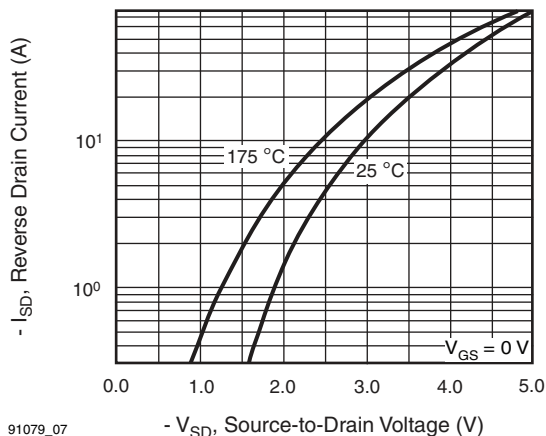
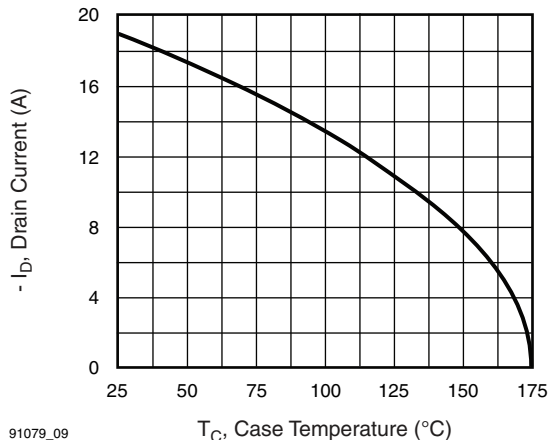
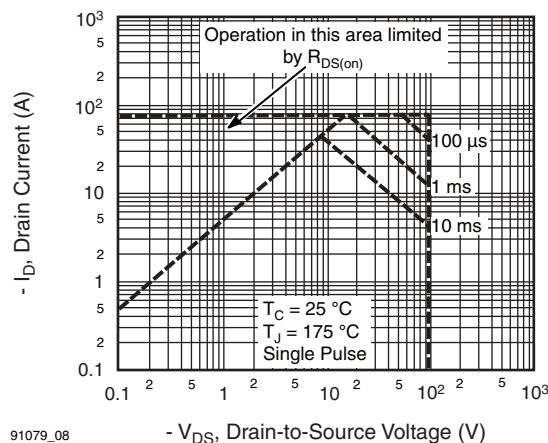
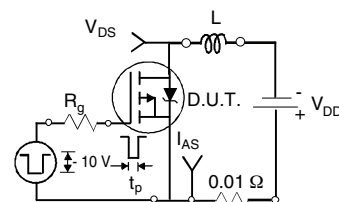
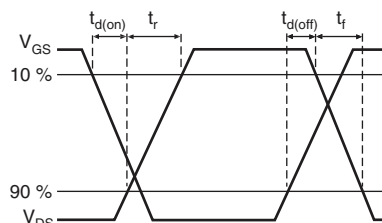
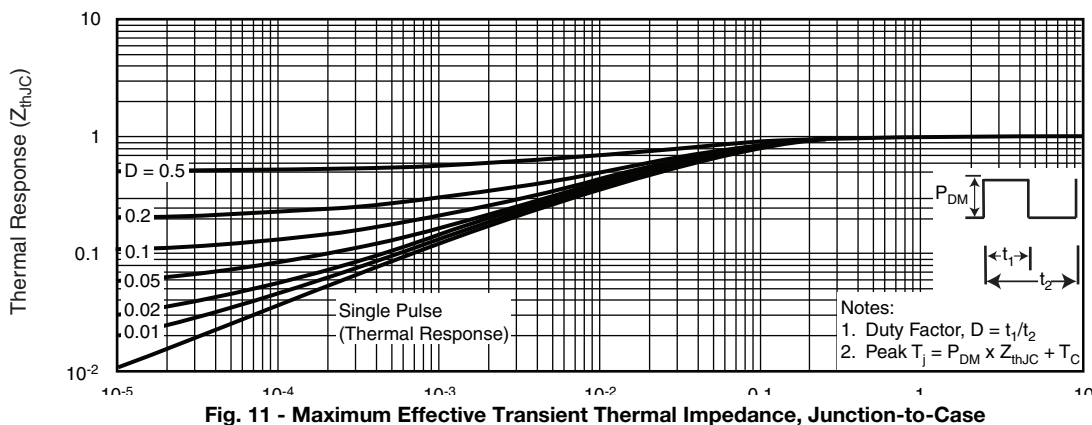
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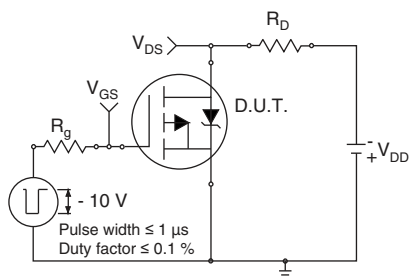
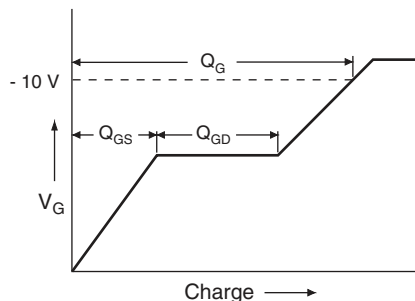
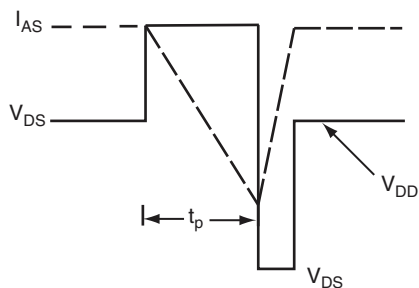
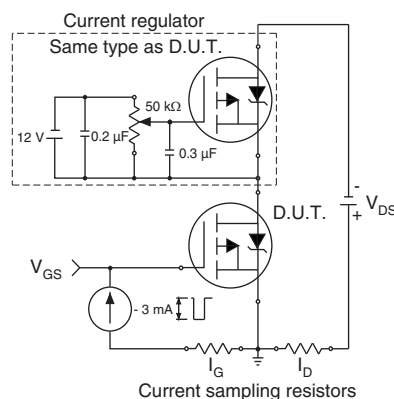
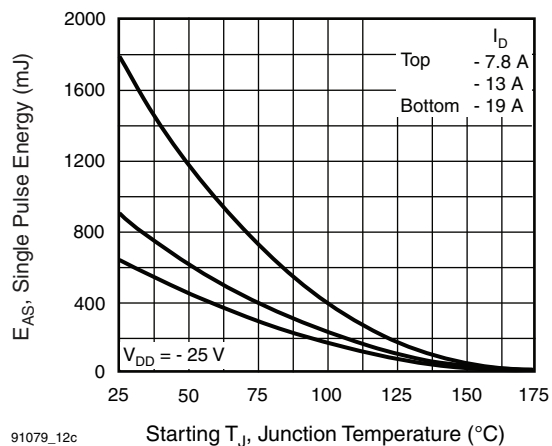
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)




Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Maximum Safe Operating Area

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 13a - Basic Gate Charge Waveform

Fig. 12b - Unclamped Inductive Waveforms

Fig 13b - Gate Charge Test Circuit

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

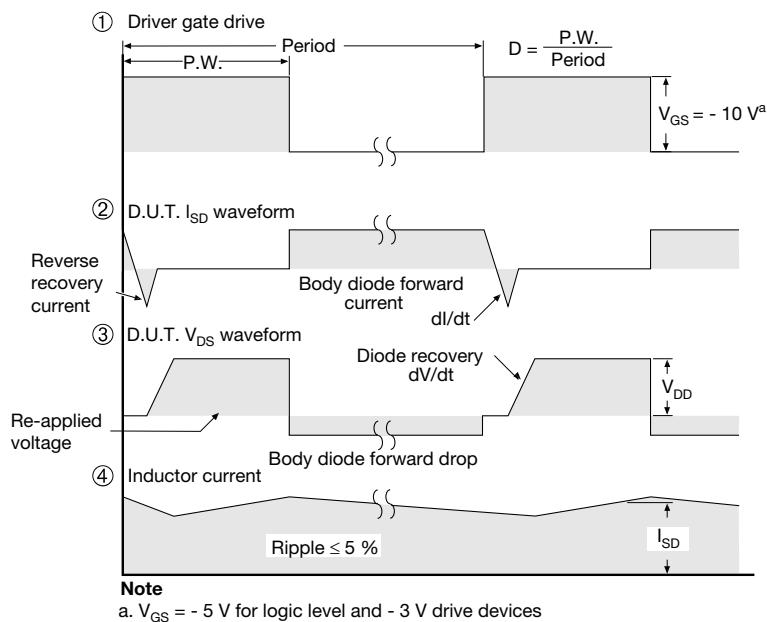
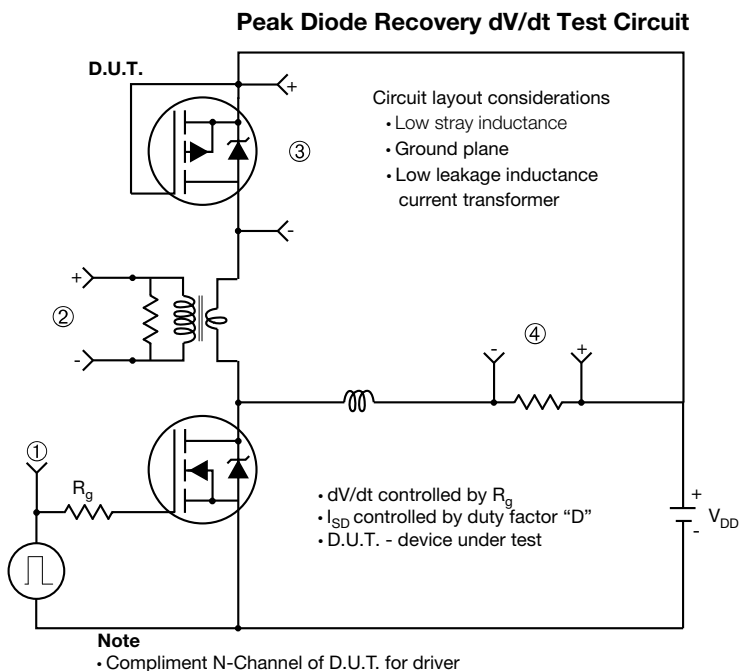
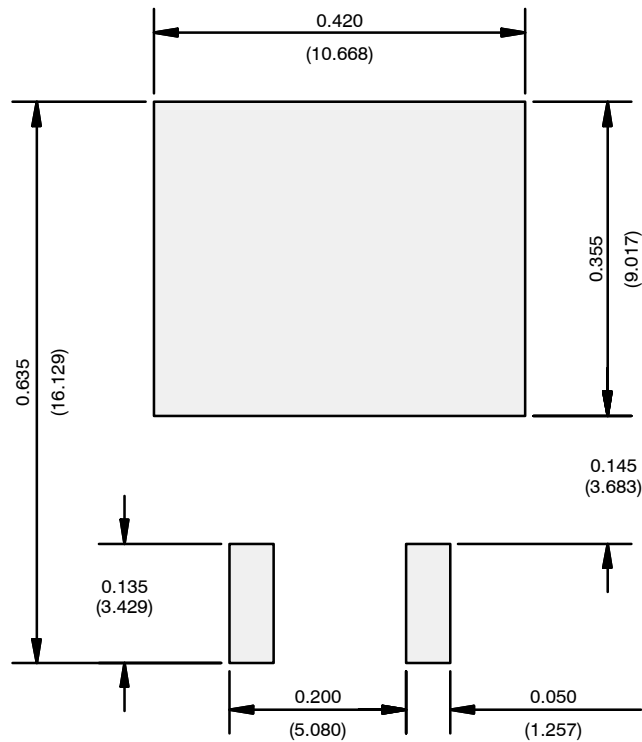


Fig. 14 - For P-Channel

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RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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