



SOLID STATE INC.

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BLOOMFIELD, NEW JERSEY 07003

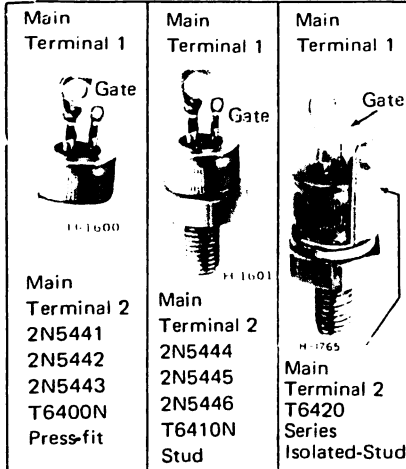
www.solidstateinc.com

Thyristors

2N5441 2N5442 2N5443

2N5444 2N5445 2N5446

T6400 T6410 T6420 Series



40-A Silicon Triacs

Press-Fit, Stud, and Isolated-Stud Packages

For 120-V Line Operation . . . 2N5441, 2N5444, T6420B

For 240-V Line Operation . . . 2N5442, 2N5445, T6420D

For High-Voltage Operation . . 2N5443, 2N5446, T6420M
T6400N, T6410N, T6420N

Features:

- di/dt Capability = 100 A/μs
- Shorted-Emitter, Center-Gate Design
- Low Switching Losses
- Low On-State Voltage at High Current Levels
- Low Thermal Resistance

Triacs are gate-controlled, full-wave silicon ac switches. They are designed to switch from an off-state to an on-state

for either polarity of applied voltage with positive or negative gate-triggering voltages.

MAXIMUM RATINGS, Absolute-Maximum Values:

For Operation with Sinusoidal Supply Voltage at Frequencies up to 50/60 Hz and with Resistive or Inductive Load.

REPETITIVE PEAK OFF-STATE VOLTAGE:

Gate open, $T_J = -65$ to 110°C

RMS ON-STATE CURRENT (Conduction angle = 360°):

Case temperature

- * $T_C = 70^\circ\text{C}$ (Press-fit types)
- * $= 65^\circ\text{C}$ (Stud types)
- * $= 60^\circ\text{C}$ (Isolated-stud types)

For other conditions

PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT:

For one cycle of applied principal voltage

- * 60 Hz (sinusoidal)
- * 50 Hz (sinusoidal)

For more than one cycle of applied principal voltage

RATE OF CHANGE OF ON-STATE CURRENT:

$V_{DM} = V_{DROM}$, $I_{GT} = 200\text{ mA}$, $t_r = 0.1\text{ }\mu\text{s}$ (See Fig. 13) . .

FUSING CURRENT (for Triac Protection):

$T_J = -65$ to 110°C , $t = 1.25$ to 10 ms

PEAK GATE-TRIGGER CURRENT:

For $1\text{ }\mu\text{s}$ max., See Fig. 7

*GATE POWER DISSIPATION:

PEAK (For $10\text{ }\mu\text{s}$ max., $I_{GTM} \leq 4\text{ A}$, See Fig. 7)

AVERAGE

TEMPERATURE RANGE:

Storage

Operating (Case)

*TERMINAL TEMPERATURE (During soldering):

For 10 s max. (terminals and case)

	2N5441	2N5442	2N5443	T6400N
	2N5444	2N5445	2N5446	T6410N
	T6420B	T6420D	T6420M	T6420N
V_{DROM}	200	400	600	800
	V			
$I_T(\text{RMS})$				
	_____ 40 _____			
	_____ 40 _____			
	_____ 40 _____			
	_____ See Fig. 3 _____			
I_{TSM}				
	_____ 300 _____			
	_____ 265 _____			
	_____ See Fig. 4 _____			
di/dt				
	_____ 100 _____			
	_____ A/μs _____			
I_2^t				
	_____ 350 _____			
	_____ A ² s _____			
I_{GTM}				
	_____ 12 _____			
	_____ A _____			
P_{GM}				
	_____ 40 _____			
	_____ W _____			
$P_{G(AV)}$				
	_____ 0.75 _____			
	_____ W _____			
T_{stg}				
	_____ -65 to 150 _____			
	_____ °C _____			
T_C				
	_____ -65 to 110 _____			
	_____ °C _____			
T_T				
	_____ 225 _____			
	_____ °C _____			

* In accordance with JEDEC registration data format (JS-14, R0F2) filed for the JEDEC (2N-Series) types.

• For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.

• For either polarity of gate voltage (V_G) with reference to main terminal

• For temperature measurement reference point, see Dimensional Outline.

ELECTRICAL CHARACTERISTICS

At Maximum Ratings Unless Otherwise Specified and at Indicated Case Temperature (T_C)

CHARACTERISTIC	SYMBOL	LIMITS			UNITS
		FOR ALL TYPES UNLESS OTHERWISE SPECIFIED			
		MIN.	TYP.	MAX.	
Peak Off-State Current: [♠] Gate open, $T_J = 110^\circ\text{C}$, $V_{DROM} = \text{Max. rated value}$	I_{DROM}	—	0.2	4*	mA
Maximum On-State Voltage: [♠] For $i_T = 100\text{ A (peak)}$, $T_C = 25^\circ\text{C}$ For $i_T = 56\text{ A (peak)}$, $T_C = 25^\circ\text{C}$	V_{TM}	— —	1.7 1.5	2 1.85*	V
DC Holding Current: [♠] Gate open, Initial principal current = 500 mA (dc), $v_D = 12\text{V}$: $T_C = 25^\circ\text{C}$ $T_C = -65^\circ\text{C}$ For other case temperatures	I_{HO}	— —	25 —	60 100*	mA
See Fig. 6					
Critical Rate of Rise of Commutation Voltage: [♠] For $v_D = V_{DROM}$, $I_{T(RMS)} = 40\text{ A}$, commutating $di/dt = 22\text{ A/ms}$, gate unenergized, (See Fig. 14): $T_C = 70^\circ\text{C}$ (Press-fit types) $T_C = 65^\circ\text{C}$ (Stud types) $T_C = 60^\circ\text{C}$ (Isolated-stud types)	dv/dt	5* 5* 5	30 30 30	— — —	V/ μs
Critical Rate of Rise of Off-State Voltage: [♠] For $v_D = V_{DROM}$, exponential voltage rise, gate open, $T_C = 110^\circ\text{C}$: 2N5441, 2N5444, T6420B, 2N5442, 2N5445, T6420D, 2N5443, 2N5446, T6420M, T6400N, T6410N, T6420N,	dv/dt	50* 30* 20* 10	200 150 100 75	— — — —	V/ μs
DC Gate-Trigger Current: ^{♠♠} For $v_D = 12\text{ V (dc)}$ $R_L = 30\ \Omega$ $T_C = 25^\circ\text{C}$ Mode V_{MT2} V_G I^+ positive positive III^- negative negative I^- positive negative III^+ negative positive	I_{GT}	— — — —	15 20 30 40	50 50 80 80	mA
For $v_D = 12\text{ V (dc)}$ $R_L = 30\ \Omega$ $T_C = -65^\circ\text{C}$ Mode V_{MT2} V_G I^+ positive positive III^- negative negative I^- positive negative III^+ negative positive		— — — —	— — — —	125* 125* 240* 240*	
For other case temperatures See Figs. 8 & 9					
DC Gate-Trigger Voltage: ^{♠♠} For $v_D = 12\text{ V (dc)}$, $R_L = 30\ \Omega$, $T_C = 25^\circ\text{C}$ $T_C = -65^\circ\text{C}$ For other case temperatures For $v_D = V_{DROM}$, $R_L = 125\ \Omega$, $T_C = 110^\circ\text{C}$	V_{GT}	— — 0.2	1.35 1.8 —	2.5 3.4* —	V
See Fig. 10					
Gate-Controlled Turn-On Time: (Delay Time + Rise Time) For $v_D = V_{DROM}$, $I_{GT} = 200\text{ mA}$, $t_r = 0.1\ \mu\text{s}$, $i_T = 60\text{ A (peak)}$, $T_C = 25^\circ\text{C}$ (See Figs. 11 & 15)	t_{gt}	—	1.7	3	μs
Thermal Resistance, Junction-to-Case: Steady-State Press-fit types Stud types Isolated-stud types Transient (Press-fit & stud types)	$R_{\theta JC}$	— — —	— — —	0.8* 0.9* 1	$^\circ\text{C/W}$
See Fig. 12					

* In accordance with JEDEC registration data format (JS-14, RDF 2) filed for the JEDEC (2N-Series) types.

♠ For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.♠♠ For either polarity of gate voltage (V_G) with reference to main terminal 1.

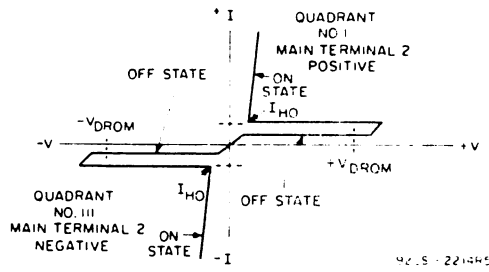


Fig. 1—Principal voltage-current characteristic.

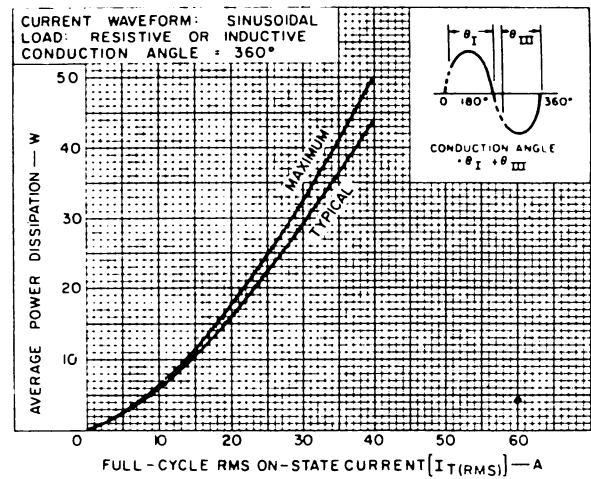


Fig. 2—Power dissipation vs. on-state current.

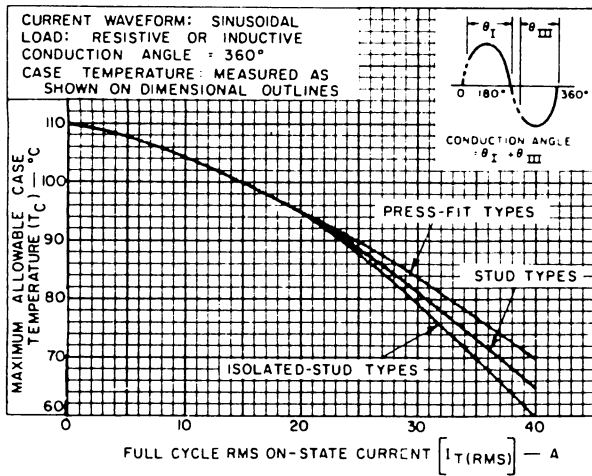


Fig. 3—Maximum allowable case temperature vs. on-state current.

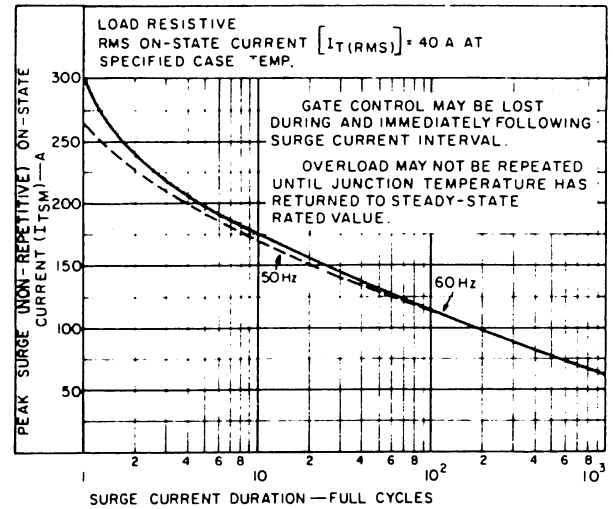


Fig. 4—Peak surge on-state current vs. surge current duration.

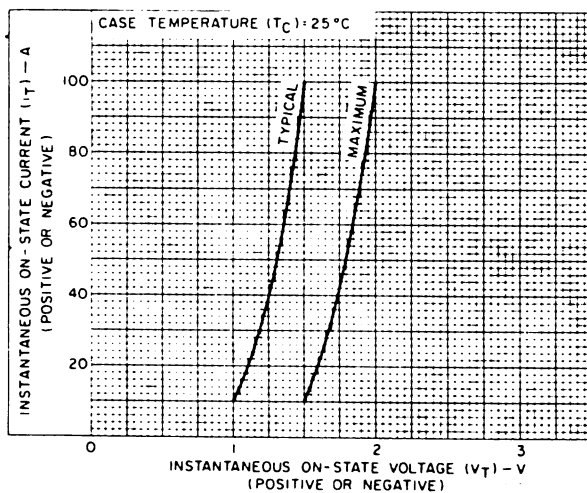


Fig. 5—On-state current vs. on-state voltage.

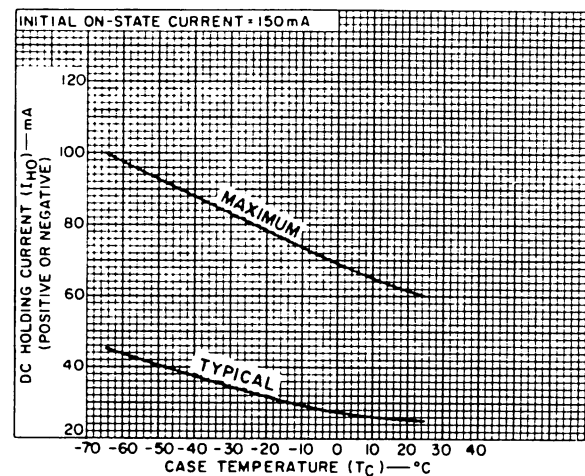


Fig. 6—DC holding current vs. case temperature.

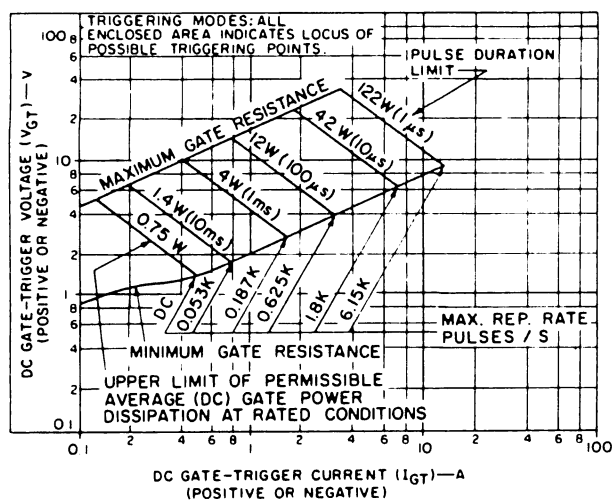


Fig. 7—Gate-trigger characteristics and limiting conditions for determination of permissible gate-trigger pulses.

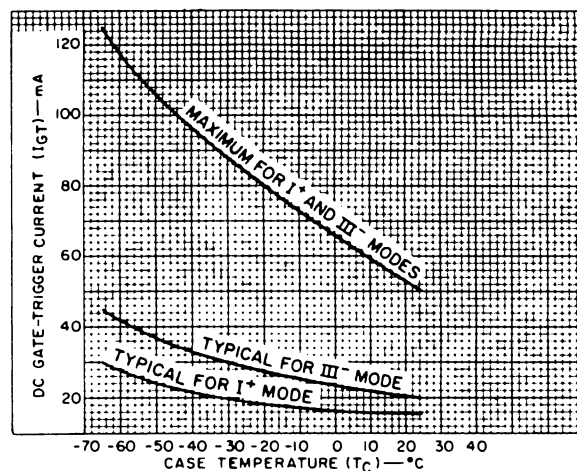


Fig. 8—DC gate-trigger current vs. case temperature (I* & III* modes).

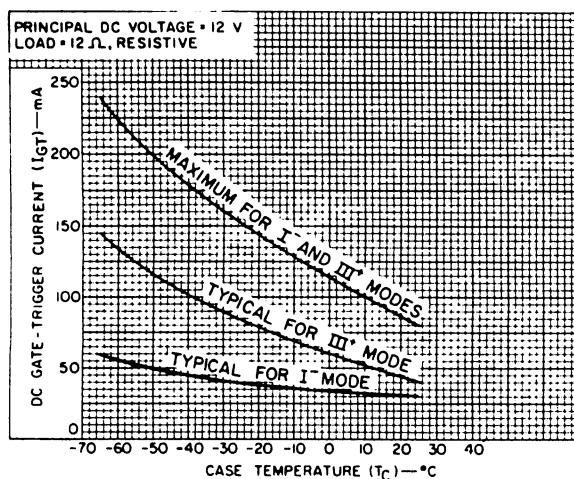


Fig. 9—DC gate-trigger current vs. case temperature (I* & III* modes).

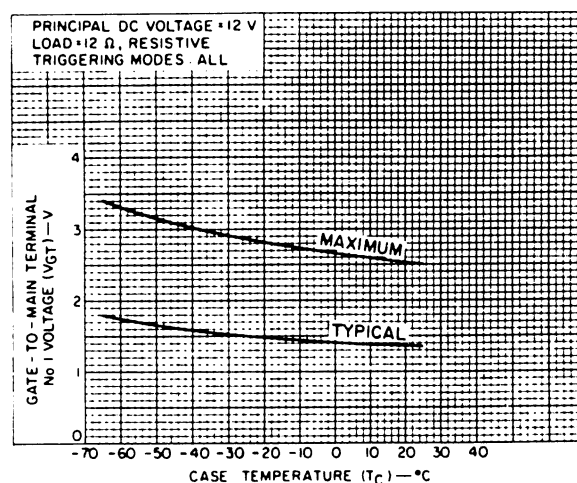


Fig. 10—DC gate-trigger voltage vs. case temperature.

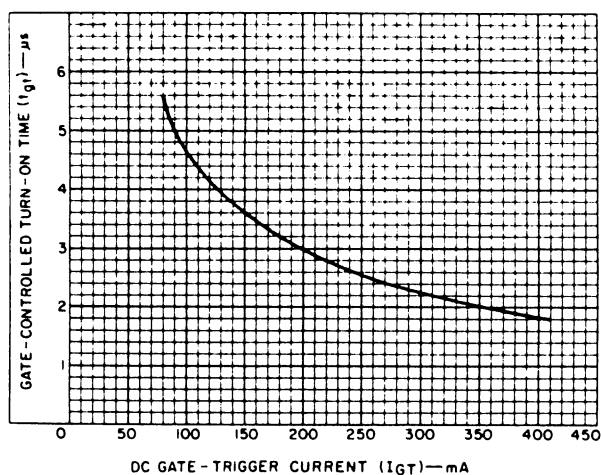


Fig. 11—Turn-on time vs. gate-trigger current.

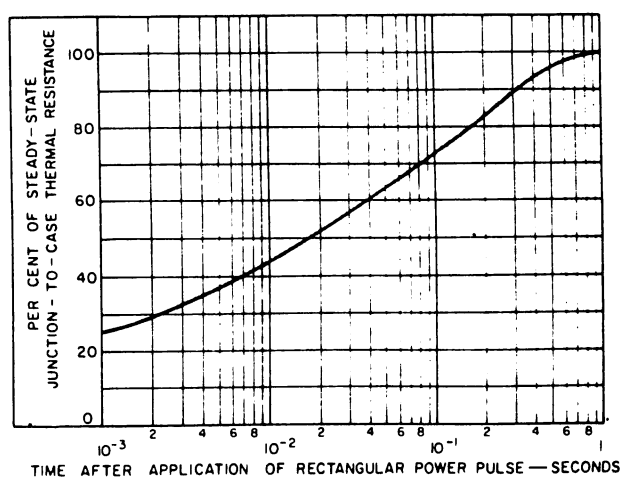


Fig. 12—Transient junction-to-case thermal resistance vs. time for press-fit and stud types.

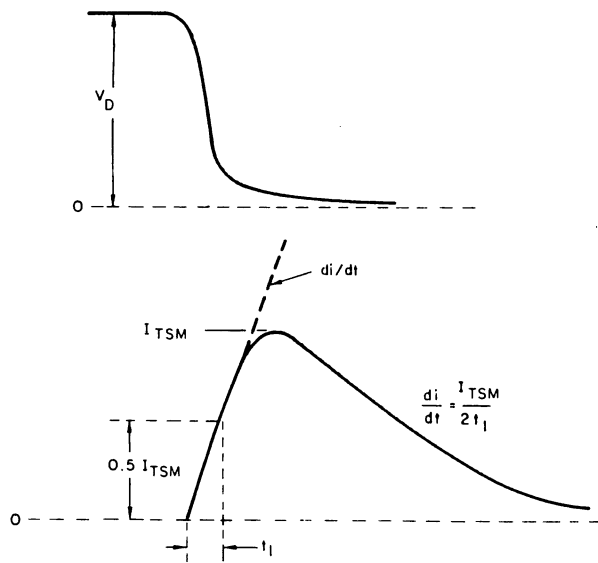


Fig. 13—Rate of change of on-state current with time (defining di/dt).

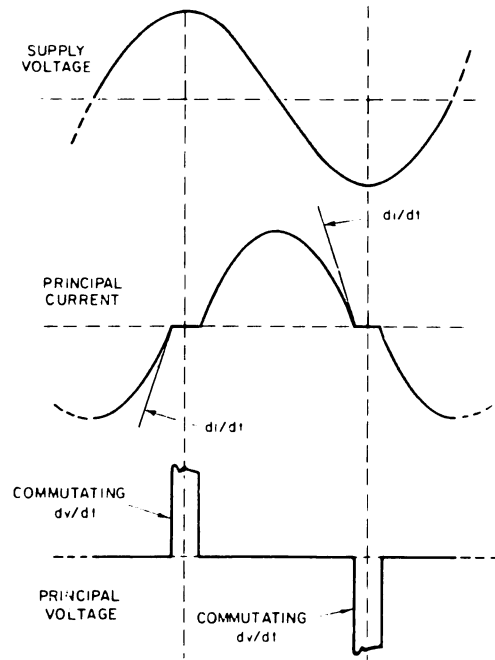


Fig. 14—Relationship between supply voltage and principal current (inductive load) showing reference points for definition of commutating voltage (dv/dt).

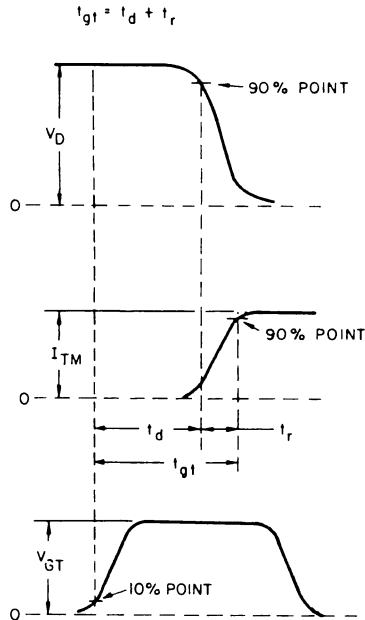


Fig. 15—Relationship between off-state voltage, on-state current, and gate-trigger voltage showing reference points for definition of turn-on time (t_{gt}).

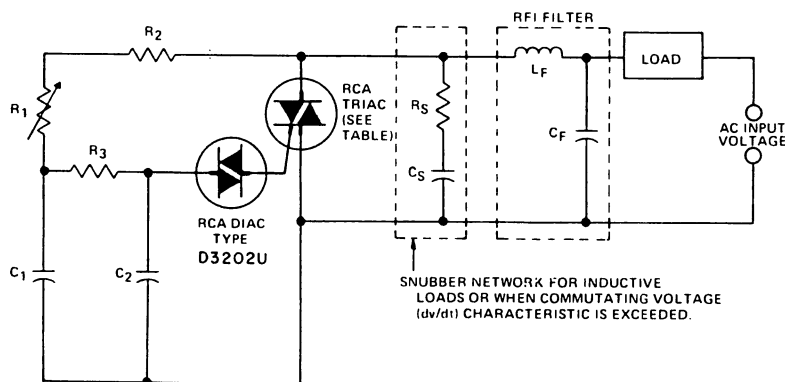


Fig. 16—Typical phase-control circuit for lamp dimming, heat control, and universal-motor speed control.

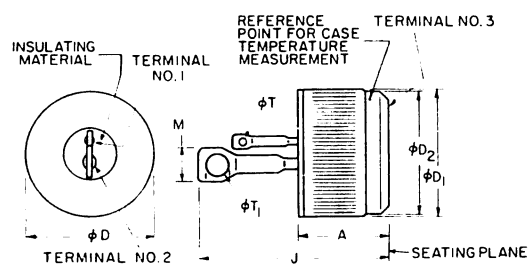
AC INPUT VOLTAGE	120V 60Hz	240V 60Hz	240V 50Hz
C_1	0.1 μ F 200V	0.1 μ F 400V	0.1 μ F 400V
C_2	0.1 μ F 100V	0.1 μ F 100V	0.1 μ F 100V
R_1	100K Ω 1/2W	200K Ω 1W	250K Ω 1W
R_2	2.2K Ω 1/2W	3.3K Ω 1/2W	3.3K Ω 1/2W
R_3	15K Ω 1/2W	15K Ω 1/2W	15K Ω 1/2W
SNUBBER NETWORK FOR 40-A (RMS)*INDUCTIVE LOAD	C_S	0.18 0.22 μ F 200V	0.18 0.22 μ F 400V
	R_S	330 390 Ω 1/2W	330 390 Ω 1/2W
RFI FILTER	C_F *	0.1 μ F 200V	0.1 μ F 400V
	L_F *	100 μ H	200 μ H
RCA TRIACS	2N5441	2N5442	2N5442
	2N5444	2N5445	2N5445
	T6420B	T6420D	T6420D

* For other RMS current values refer to

RCA Application Note AN-4745.

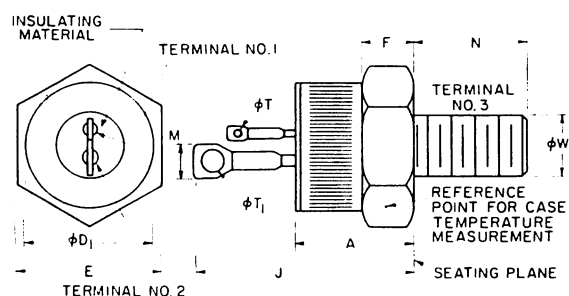
* Typical values for lamp dimming circuits.

DIMENSIONAL OUTLINE FOR TYPES
2N5441, 2N5442, 2N5443, T6400N
PRESS-FIT



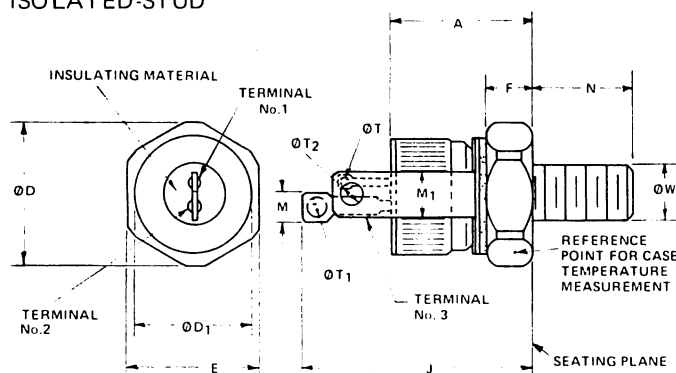
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.380	—	9.65	
ϕD	0.501	0.510	12.73	12.95	
ϕD_1	—	0.505	—	12.83	
ϕD_2	0.465	0.475	11.81	12.07	
J	0.825	1.000	20.95	25.40	
M	0.215	0.225	5.46	5.71	
ϕT	0.058	0.068	1.47	1.73	
ϕT_1	0.138	0.148	3.51	3.75	

DIMENSIONAL OUTLINE FOR TYPES
2N5444, 2N5445, 2N5446, T6410N
STUD



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.330	0.505	8.4	12.8	
ϕD_1	—	0.544	—	13.81	
E	0.544	0.562	13.82	14.28	
F	0.113	0.200	2.87	5.08	
J	0.950	1.100	24.13	27.94	
M	0.215	0.225	5.46	5.71	
N	0.422	0.453	10.72	11.50	
ϕT	0.058	0.068	1.47	1.73	
ϕT_1	0.138	0.148	3.51	3.75	
ϕW	¼-28	UNF-2A	¼-28	UNF-2A	

DIMENSIONAL OUTLINE FOR
T6420 SERIES
ISOLATED-STUD



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.673	—	17.09	
ϕD	0.604	0.614	15.34	15.59	
ϕD_1	0.501	0.505	12.72	12.82	
E	0.551	0.557	13.99	14.14	
F	0.100	0.110	2.54	2.79	
J	—	1.298	—	32.96	
M	0.210	0.230	5.33	5.84	
M_1	0.200	0.210	5.08	5.33	
N	0.422	0.452	10.72	11.48	
ϕT	0.058	0.068	1.47	1.73	
ϕT_1	0.138	0.148	3.51	3.75	
ϕT_2	0.138	0.148	3.51	3.75	
ϕW	¼-28	UNF-2A	¼-28	UNF-2A	

TERMINAL CONNECTIONS

- No. 1—Gate
 No. 2—Main Terminal 1
 Case, No. 3—Main Terminal 2