LYT3314-3328
LYTSwitch-3 Family

Single-Stage LED Driver IC with Combined PFC and Constant Current Output for Outstanding TRIAC Dimming in Isolated and Non-Isolated Topologies

Product Highlights

Combined Single-Stage PFC + Accurate CC Output

- Less than ±3% CC regulation over line and load
- Power Factor >0.9
- Ensures monotonic VA reduction with TRIAC phase angle
- Low THD, 15% typical for dimmable bulbs, as low as 7% in optimized designs

Advanced Integrated TRIAC Dimmer Detection

- Detects leading-edge and trailing-edge TRIAC dimmers
- High-efficiency mode when no dimmer is present
- Selectable dimming profile increases design flexibility
- Fast turn-on (<500 ms)
- Low pop-on and dead-travel
- Active bleeder drive for widest dimmer compatibility

Design Flexibility

- Supports buck, buck-boost, tapped buck-boost, boost, isolated and non-isolated flyback
- Up to 20 W output

Highest Reliability

- No electrolytic bulk capacitors or optoisolators for increased lifetime
- Comprehensive protection features
  - Input and output overvoltage
  - Output short-circuit and open-loop protection
- Advanced thermal control
  - Thermal foldback ensures that light continues to be delivered at elevated temperatures
  - End-stop shutdown provides protection during fault conditions

Description

The LYTSwitch™-3 family is ideal for single-stage power factor corrected constant current LED bulbs and downlighters.

Each device incorporates a high-voltage power MOSFET and discontinuous mode, variable frequency variable on-time controller. The controller also provides cycle-by-cycle current limit, output OVP, line overvoltage, comprehensive protection features, plus advanced thermal management circuitry.

All LYTSwitch-3 ICs have a built-in TRIAC detector that discriminates between leading-edge and trailing-edge dimmers. This capability together with load monitoring circuitry regulates bleeder current during each switching cycle. The controller disables the bleeder circuit completely if no dimmer is detected, significantly increasing efficiency.

The combination of a low-side switching topology, cooling via electronically quiet SOURCE pins and frequency jitter ensure extremely low EMI. This reduces the size of the input filter components – greatly reducing audible noise during dimming.

The part numbers shown in Table 1 describe 4 different power levels and two MOSFET voltage options to cost-optimize designs while EcoSmart™ switching technology insures maximum efficiency for each device size and load condition.

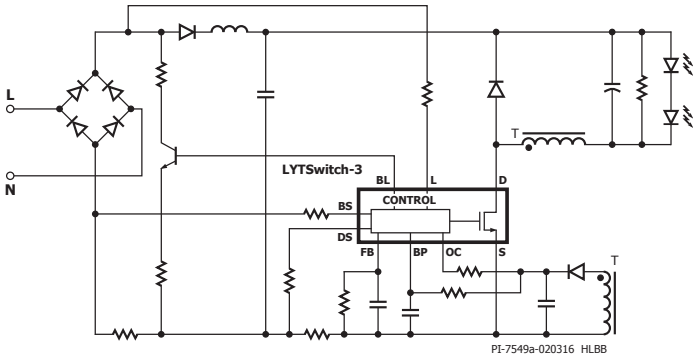


Figure 1. Simplified Schematic (Buck).

Output Power Table

Product[2]	Output Power[1]
	85-132 VAC or 185-265 VAC
LYT33x4D[3]	5.7 W
LYT33x5D	8.8 W
LYT33x6D	12.6 W
LYT33x8D	20.4 W

Table 1. Output Power Table (Buck Topology).

Notes:

1. Maximum practical continuous power in an open frame design with adequate heat sinking, measured at 50°C ambient (see Key Applications Considerations for more information).
2. Package: D: SO-16B.
3. "x" digit describes $V_{DSON(MAX)}$ of the integrated switching MOSFET, 650 V = 1, 725 V = 2.

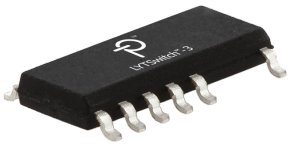


Figure 2. SO-16B (D Package).

This Product is Covered by Patents and/or Pending Patent Applications.

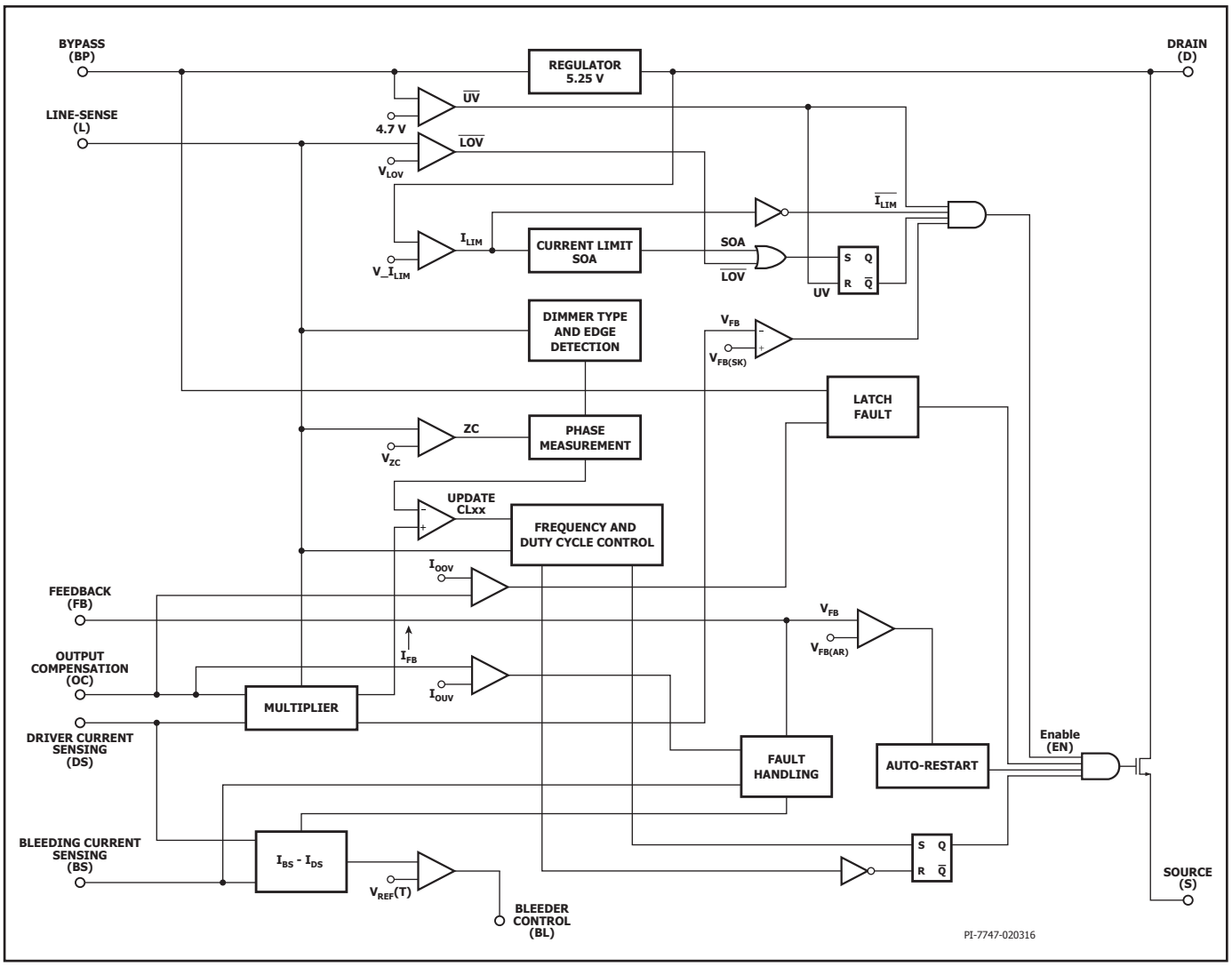


Figure 3. Block Diagram.

Pin Functional Description

LINE-SENSE (L) Pin
LINE-SENSE pin implements input voltage waveform detection: conduction angle is detected accurately since SOURCE pin is referenced to bulk capacitor ground. Input OVP is activated when LINE-SENSE pin current exceeds the predetermined threshold.

BLEEDER CURRENT SENSE (BS) Pin
BLEEDER CURRENT SENSE pin measures the total input current – active bleeder current plus switch current. This current is sensed in order to keep TRIAC current above its holding level. This is achieved by modulating the bleeder dissipation.

R_{BS} (Ω)	Dim Curve	Load Shut Down (LSD)
6 k	Max. Dim Curve	No
12 k	Min. Dim Curve	No
24 k	Min. Dim Curve	Yes

Table 2. BS Pin Resistor Programming.

DRIVER CURRENT SENSE (DS) Pin
DRIVER CURRENT SENSE pin senses the driver current. This current is used to deduce output current: it is multiplied by the input voltage and the result is then divided by the output voltage to obtain output current.

R_{DS} (Ω)	Topology
6 k	Buck, Buck-Boost, Isolated Flyback
24 k	Non-Isolated Flyback

Table 3. Topology Selection Resistor.

BLEEDER CONTROL (BL) Pin
BLEEDER CONTROL pin drives the external bleeder transistor in order to maintain the driver input current above the holding current of the dimmer TRIAC.

FEEDBACK (FB) Pin
In normal operation and full conduction the preset threshold on the FEEDBACK pin is 300 mV. This threshold gets reduced linearly with conduction angle until a minimum level is reached.

Cycle skipping is triggered when voltage on this pin exceeds 600 mV.

BYPASS (BP) Pin
5.25 V supply rail.

OUTPUT COMPENSATION (OC) Pin
Output OVP for all topologies. Output voltage compensation for indirect output current sense topologies.

DRAIN (D) Pin
High-voltage internal MOSFET (725 V or 650 V).

SOURCE (S) Pin:
Power and signal ground.

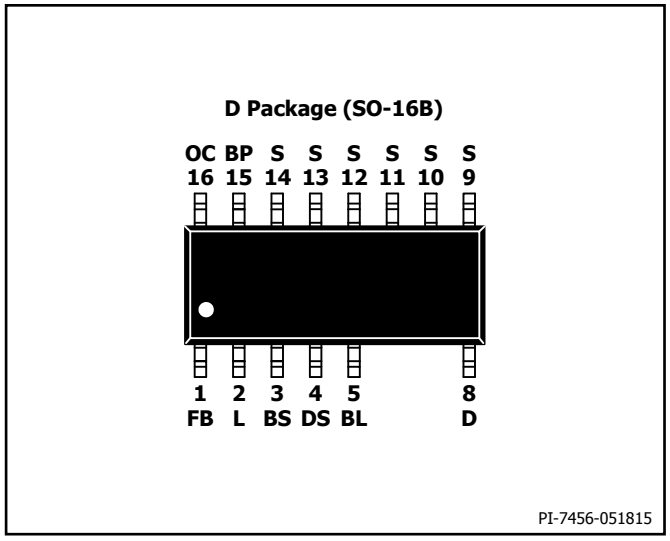


Figure 4. Pin Configuration.

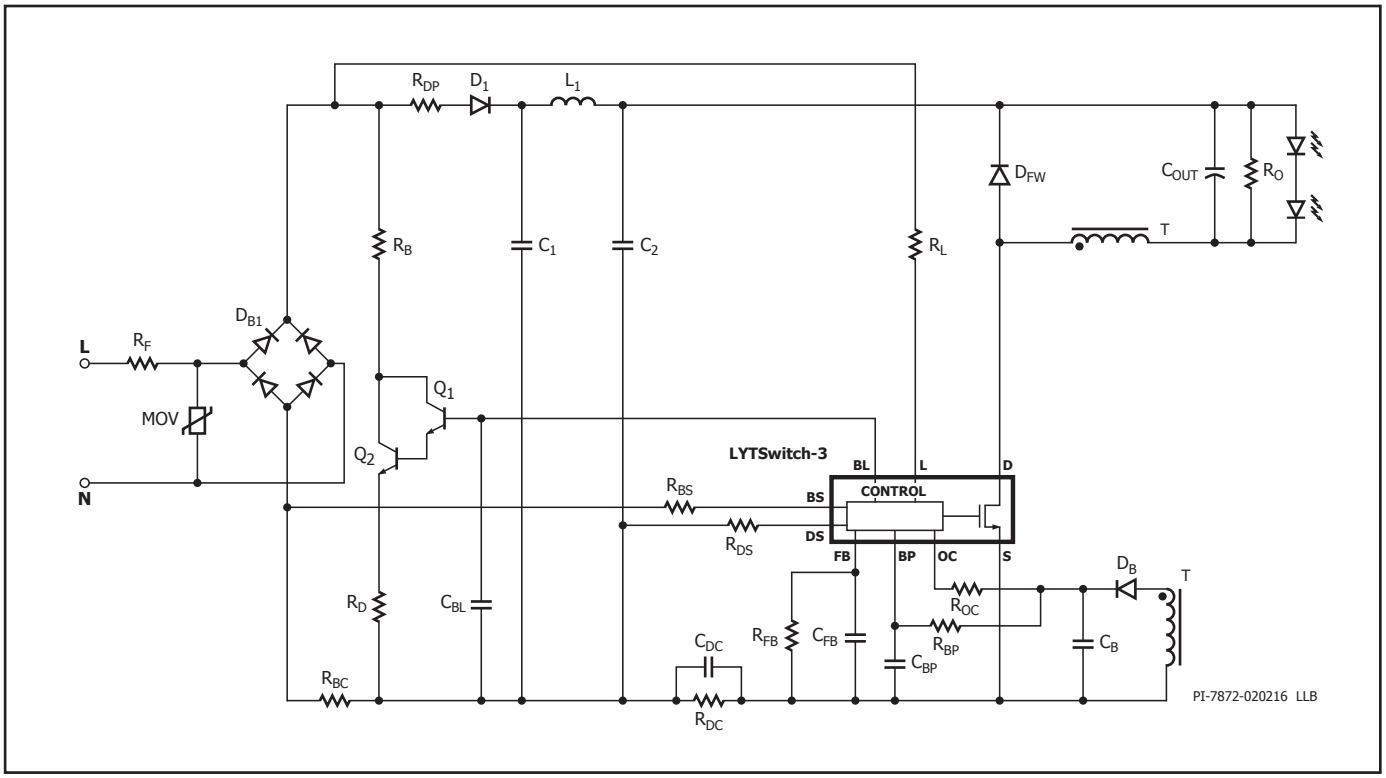


Figure 5. Typical Schematic Buck (Low-Line).

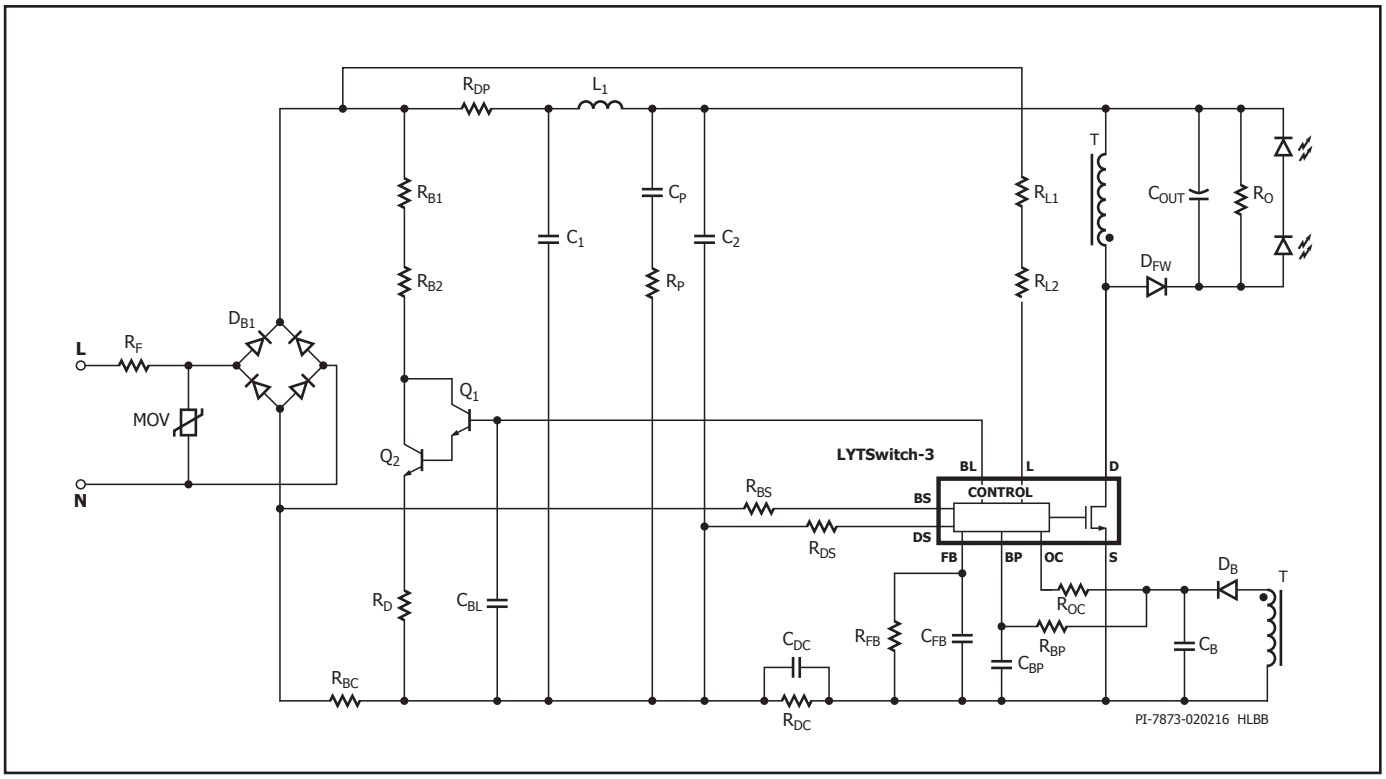


Figure 6. Typical Schematic Buck-Boost (High-Line).

Applications Example

DER-524 8 W A19 LED Bulb Driver Dimmable, Tight Regulation, High Power factor, Low ATHD Design Example

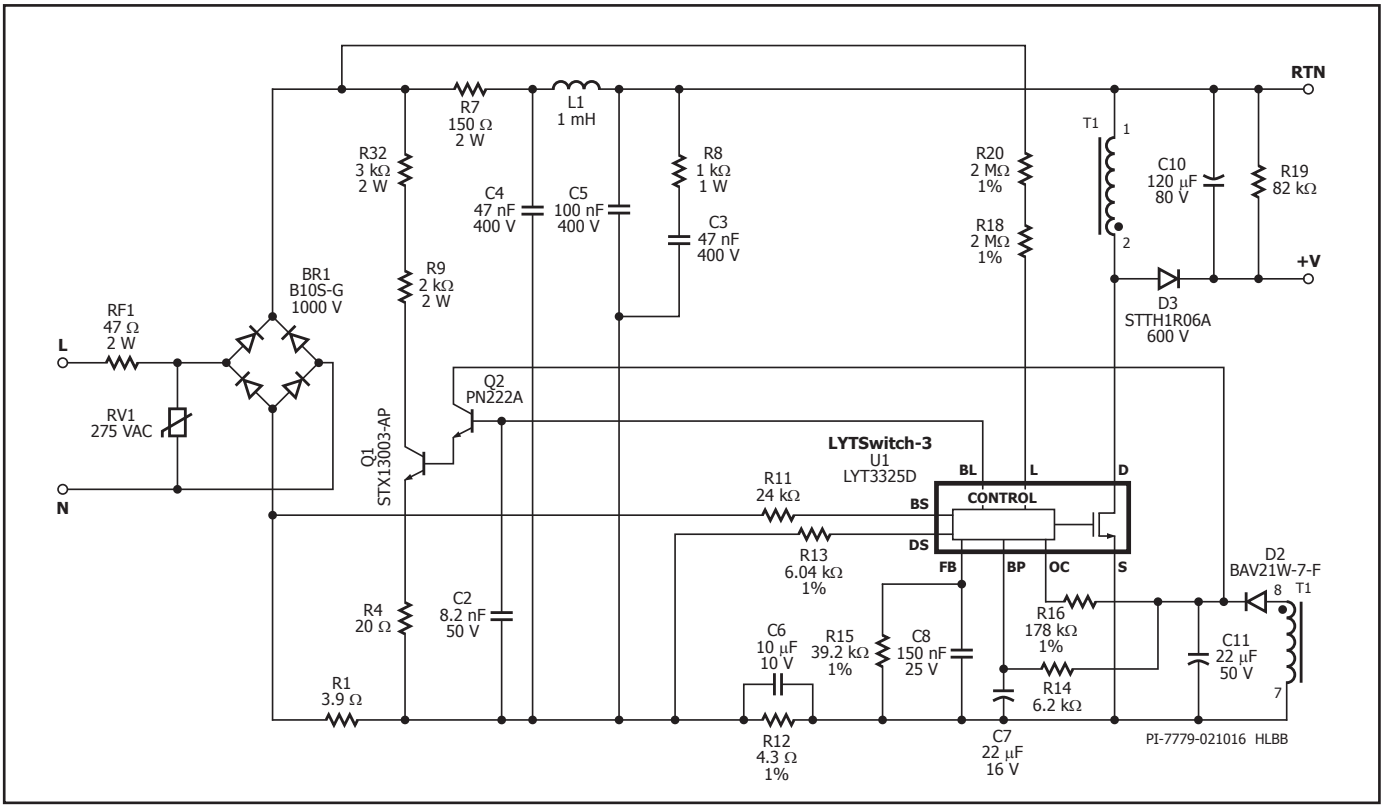


Figure 7. DER-524 8 W, 72 V, 115 mA Non-Isolated Dimmable A19 LED Bulb Driver using LYT3325D.

The circuit shown in Figure 7 is configured as a buck-boost power supply utilizing the LYT3325D from the LYTSwitch-3 family of ICs. This type of LED driver configuration is common for dimmable bulb applications where high dimmer compatibility, accurate regulation, high efficiency, high power factor and low ATHD are required along with low component count for high reliability. The output can drive an LED load from 68 V to 76 V with a constant output current of 115 mA ±3% across an input range of 195 VAC to 264 VAC and can operate in maximum ambient temperature of 100 ºC with good margin below the thermal foldback protection point. It has an efficiency of greater than 86%, very low ATHD% (less than 20%) and high power factor of greater than 0.9 measured across the input range.

Circuit Description

The LYTSwitch-3 device (U1 - LYT3325D) combines a high-voltage power MOSFET, variable frequency and on-time control engine, fast start-up, selectable dimming curves with load shutdown at deep dimming and protection functions including line and output overvoltage into a single package, greatly reducing component count. The integrated 725 V power MOSFET provides a large drain voltage margin in high-line input AC applications thus increasing reliability. A 625 V power MOSFET option is also offered to reduce cost in applications where the voltage stress on the power MOSFET is lower. Configured to operate as a discontinuous conduction mode buck-boost converter, U1 provides high power factor and very low ATHD via its internal control algorithm (the design also features low input capacitance to further reduce THD and increase PF). Discontinuous conduction mode inherently eliminates reverse current from the output diode when the power MOSFET is in the OFF-state reducing high frequency noise and allowing the use of a simpler, smaller EMI filter which also improves efficiency.

Input Filter

AC input power is rectified by bridge BR1. A 1000 V voltage rating is recommended (the maximum clamp voltage for a typical 275 V varistor is 720 V). The rectified DC is filtered by the input capacitors C4 and C5. Too much capacitance degrades power factor and ATHD, so the values of the input capacitors were adjusted to the minimum values necessary to meet EMI with a suitable margin. Inductor L1, C4 and C5 form a π (pi) filter, which attenuates conducted differential and common mode EMI currents. Optional resistor R10 across L1 damps the Q of the filter inductor to improve filtering without reducing low frequency attenuation. Fuse RF1 in Figure 7 provides protection against catastrophic failures such as short-circuit at the input. For cost reduction, this can be replaced by a fusible resistor (typically a flame proof wire-wound type) which would need to be rated to withstand the instantaneous dissipation induced when charging the input capacitance when first connected to the input line.

Selection of fuse RF1 in Figure 7 type and rating is dependent on input surge requirements. Typical minimum requirement for bulb application is 500 V differential surges. This design meets a 1 kV surge specification, so a 47 Ω fusible resistor in Figure 7 was used. A fast-blow fuse with high ampere energy (I^2T) rating could also be used.

LYTSwitch-3 Output Regulation

In order to maintain very tight output current regulation – within ±3%, the FEEDBACK (FB) pin voltage (with an appropriately selected low-pass filter comprising R15 and C8) is compared to a preset average feedback voltage (V_{FB}) of 300 mV. When the detected signal is above or below the preset average V_{FB} threshold voltage, the onboard averaging-engine will adjust the frequency and/or on-time to maintain regulation.

The bias winding voltage is proportional to the output voltage (controlled by the turns-ratio between the bias supply and output-main winding). This allows the output voltage to be monitored without the need for output-side feedback components. Resistor R16 in Figure 7 converts the bias voltage into a current which is fed into the OUTPUT COMPENSATION (OC) pin of U1. The OUTPUT COMPENSATION pin current is also used to detect output overvoltage which is set to 30% above the nominal output voltage. Once the current exceeds the I_{OOV} threshold the IC will trigger a latch, which disables switching which prevents the output from rising further. An AC recycle is needed to reset this protection mode once triggered.

In order to provide line input voltage information to U1 the rectified input AC voltage is fed into the LINE SENSE (L) pin of U1 as a current via R20 and R18. This sensed current is also used by U1 to detect the input zero crossing, type of dimmer (i.e. leading or trailing edge) connected to the input and set the input line overvoltage protection threshold. In a line overvoltage condition once this current exceeds the I_{LOV+} threshold, the IC will instantaneously disable switching to protect the power MOSFET from further voltage stress. The IC will start switching as soon as the line voltage drops to safe levels indicated by the LINE SENSE pin current dropping by 5 µA.

The primary switched current is sensed via R12 and filtered with C6. The signal is fed into the DRIVER CURRENT SENSE (DS) pin. A low ESR ceramic capacitor of at least 10 µF is recommended for capacitor C6 for better regulation and reduced the AC RMS loss across R6. The DRIVER CURRENT SENSE pin program resistor R13 is 6.04 kΩ 1% for primary-side regulation for indirectly sensing of the output current.

The internal frequency/on-time engine inside the LYTSwitch-3 IC combines the OUTPUT COMPENSATION pin current, the LINE SENSE pin current and the DRIVER CURRENT SENSE pin current information to deduce the FEEDBACK pin signal. This is compared to an internal V_{FB} threshold to maintain accurate constant output current.

It is important to note that for accurate output current regulation the use of 1% tolerance for LINE SENSE pin resistors (R20 and R18) is recommended. This recommendation also applies to OUTPUT COMPENSATION pin resistor R16, FEEDBACK pin resistor R15 (capacitor C8 at least X7R type), and DRIVER CURRENT SENSE pin resistor R12 and R13.

Diode D2 and C11 provides a bias supply for U1 from an auxiliary winding on the transformer. Bias supply recommended voltage level is 20 V, when this voltage drops at low conduction angle during dimming would be high enough to maintain supply for U1. Filter capacitor C11 should be sized to ensure a low ripple voltage. Capacitor C7 serves as local decoupling for the BYPASS pin of U1 which is the supply pin for the internal controller. Current via R14 is typically limited to 2.5 mA. During start-up, C7 is charged to ~5.3 V from an internal high-voltage current source internally fed from the DRAIN pin. This allows U1 to start switching even at low conduction angle when in dimming. After start-up the operating supply current is provided from the bias supply via R14. The recommended value for the BYPASS pin capacitor C7 is 22 µF. The voltage rating for the capacitor should be greater than 7 V. The capacitor can be a ceramic or electrolytic type, but tolerance should be less than 50%. The capacitor must be physically located close to BYPASS and SOURCE pins for effective noise decoupling.

Output Rectification

During the switching OFF-state the output from the transformer main winding is rectified by D3 and filtered by C10. An ultrafast 1 A, 600 V with 35 ns reverse recovery time (t_{RR}) diode was selected for efficiency. The value of the output capacitor C10 was selected to give peak-to-peak LED ripple current equal to 30% of the mean value. However, the output ripple current will also depend on the type and impedance characteristic of the LED load, so it is recommended to, use the actual LED load for sizing the capacitor value for the output ripple current. For designs where lower ripple is desirable the output capacitance value can be increased unlike traditional power supplies, low ESR capacitors are not required for the output stage of LED designs.

A small output pre-load resistor R19 discharges the output capacitor when the driver is turned off, giving a relatively quick and smooth decay of the LED light. Recommended pre-load power dissipation is ≤0.5% of the output power.

Phase-Cut Dimming

The biggest challenge in designing dimmable LED bulb is high compatibility with a broad range of dimmer types and power rating. As different type of dimmers have different minimum loading requirements the dimmable LED bulb may manifest varying incompatibility behavior depending on the dimming conditions from light flickering or shimmering, ghosting, huge pop-on to low dim ratio.

There are two main types of phase-cut dimmers namely leading edge (Figure 8) and trailing edge (Figure 9). Each type has its own characteristic and nuances that particularly makes it challenging for LED driver to achieve high compatibility and no one can ever know what type of dimmer an LED bulb will be used with therefore it is imperative that the designer must use a controller with bleeder with the capability to satisfy the requirement depending the type of the dimmer.

The requirement to provide flicker-free output dimming with low-cost, TRIAC-based, leading edge phase dimmers introduces a number of trade-off in the design. Due to the much lower power consumed by LED based lighting the current drawn by the overall lamp is below the holding current of the TRIAC within the dimmer. This causes undesirable behaviors such as limited dimming range and/or flickering. The relatively large impedance the LED lamp presents to the line allows significant ringing to occur due to the inrush current charging the input capacitance when the TRIAC turns on. This too can cause similar undesirable behavior as the ringing may cause the TRIAC current to fall to zero and turn-off.

Figure 9 shows the line voltage and current at the input of the power supply with a trailing edge dimmer. In this example, the dimmer conducts at 90 degrees. Many of these dimmers use back-to-back connected power FETs rather than a TRIAC to control the load. This eliminates the holding current issue of TRIACs and since the conduction begins at the zero crossing, high current surges and line ringing are minimized. Typically these types of dimmers do not require damping circuits. However, would require a bleeder circuit to provide a low impedance path for the internal supply to recharge and reset its internal controller in order to operate normally and avoid misfiring for the succeeding cycle of the incoming input.

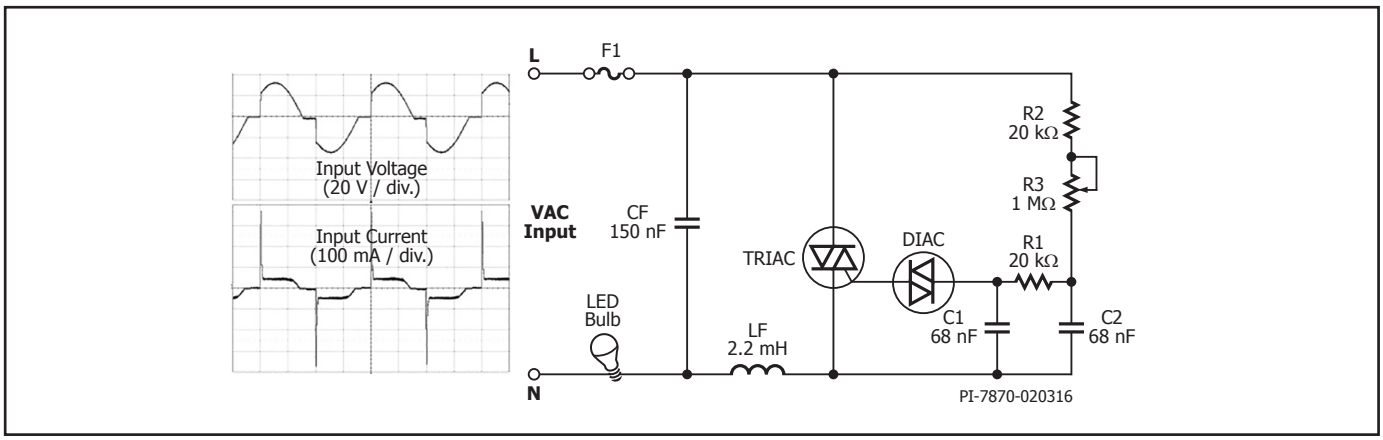


Figure 8. Typical Voltage and Current Waveform and Schematic of a TRIAC-Based Leading Edge Dimmer.

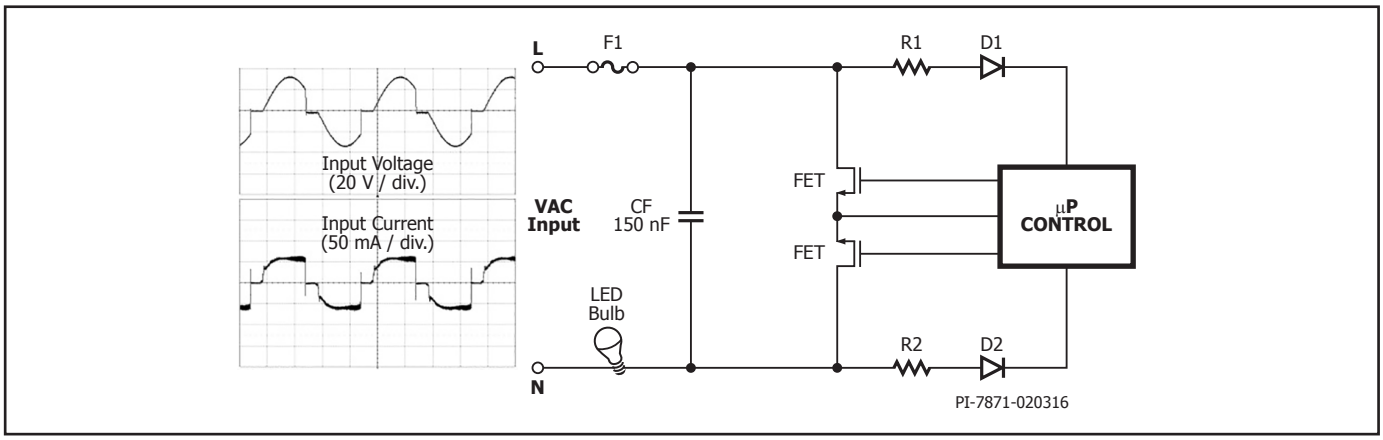


Figure 9. Typical Voltage and Current Waveforms and Schematic of a MOSFET-Based Trailing Edge Dimmer.

LYTSwitch-3 Smart Active Bleeder

To overcome the challenges of designing for dimmable LED driver with high compatibility on any type of dimmer, LYTSwitch-3 family features a built-in TRIAC detector that is able to discriminate between leading-edge and trailing-edge dimmers. This capability together with load monitoring circuitry enables the controller to adjust bleeder operation during each switching cycle to ensure a TRIAC input impedance, or to disable the bleeder circuitry completely if no dimmer is detected (significantly increasing efficiency). The active bleeder also helps in keeping the input current above the TRIAC holding and latching current while the input current corresponding to the effective driver resistance increases during each AC half-cycle.

The LYTSwitch-3 ICs provide excellent dimming performance with its close loop smart bleeder function. Transistor Q1 together with Q2 in emitter follower connection, function as a high gain active switch that pulls current from the input via R9 and R32. This maintains the holding current and latching current necessary to keep the TRIAC on during the entire input cycle. The analog signal from the BLEEDER CONTROL (BL) pin of U1 drives Q1 and Q2 linearly when the input current falls below the holding current thus maintaining the current set by the resistor R1. The holding current can be set using the equation R1 = 120 mV / A. For this design (DER-524) it is 30 mA. Bleeder resistors R9 and R32 recommended total value is 5 kΩ with 2 W power rating each resistor for high-line application (1.2 kΩ total for low-line at 50 mA holding current).

Capacitor C2 and degenerative resistor R4 serve as stabilizing network for the bleeder transistors for optimized dimming performance. Resistor R4 typical range of value is 20 – 47 Ω while C2 is between 4.7 – 22 nf.

Passive Bleeder and Damper

Both capacitor C3 and resistor R8 together with fusible resistor RF1 and damper R7 act as damper reducing the ringing current induced by the spike of current charging the input bulk capacitors after the TRIAC fired at the onset of input AC. The value of C3 is typically from 47 nf to 220 nf, while R8 can be between 470 Ω to 1 kΩ.

Key Design Considerations

Device Selection

The data sheet power table (Table 4) represents the maximum practical continuous output power that can be delivered in an open frame design with adequate heat sinking.

Output Power Table

Product	Output Power
	85-132 VAC or 185-265 VAC
LYT33x4D	5.7 W
LYT33x5D	8.8 W
LYT33x6D	12.6 W
LYT33x8D	20.4 W

Table 4. Output Power Table.

DER-524 is an 8 W LED dimmable driver. Where LYT3325D was chosen for its higher voltage power MOSFET rating of 725 V because the topology chosen was a buck-boost and the specification called for a maximum input voltage of 264 VAC. In other applications where surge and line voltage conditions allow, it may be possible to use the 650 V power MOSFET option to reduce design cost without impacting reliability.

Magnetics Design

A very common core type was selected, an EE10 with ferrite core material and a wide winding window that allowed better convection cooling for the winding.

To ensure that discontinuous conduction mode (DCM) operation of LYTSwitch-3 is maintained over line input and inductance tolerance variations that is needed for tight output current regulation, it is recommended that the LYTSwitch-3 PIXIs spreadsheet located at PI Expert online (https://piexpertonline.power.com/site/login) should be used for magnetics calculations.

EMI Considerations

Total input capacitance affects PF and ATHD – increasing the value will degrade performance. With LYTSwitch-3 the combination of a low-side switching configuration and frequency jitter reduces EMI and enables the use of small and simple pi (π) filter. It also allows simple magnetic construction where the main winding can be wound continuously using the automated winding approach preferred for low-cost manufacturing. The recommended location of the EMI filter is after the bridge rectifier. This allows the use of regular film capacitors as opposed to more expensive safety rated X-capacitors that would be required if the filter is placed before the bridge.

Surge Immunity Consideration

This design assumed a differential surge requirement of up to 1 kV which can be met easily with LYTSwitch-3's very accurate line overvoltage protection and a MOV (RV1).

Thermal and Lifetime Considerations

Lighting applications present thermal challenges to the driver. In many cases the LED load dissipation determines the working ambient temperature experienced by the drive. Thermal evaluation should be performed with the driver inside the final enclosure. Temperature has a direct impact on driver and LED lifetime. For every 10 °C rise in temperature, component life is reduced by a factor of 2. Therefore it is important to verify and optimize the operating temperatures of all components.

Provide enough spacing between bleeder and damper components for better natural heat convection cooling.

Quick Design Checklist

Maximum Drain Voltage – Verify that the peak Drain voltage stress (VDS) does not exceed 725 V under all operating conditions, including start-up and fault conditions.

Maximum Drain Current – Measure the peak Drain current under all operation conditions (including start-up and fault conditions). Look for transformer saturation (usually occurs at highest operating ambient temperatures). Verify that the peak current is less than the stated Absolute Maximum Rating in the data sheet.

Thermal Check – At maximum output power, for both minimum and maximum line voltage and maximum ambient temperature; verify that temperature specifications are not exceeded for the LYTSwitch-3, transformer, output diodes, output capacitors and clamp components.

PCB Layout Considerations

The EMI filter components should be located close together to improve filter effectiveness. Place the EMI filter components C4 and L1 as far away as possible from any switching nodes on the circuit board especially U1 drain node, output diode (D3) and the transformer (T1).

Care should be taken in placing the components on the layout that are used for processing input signals for the feedback loop – any high frequency noise coupled to the signal pins of U1 may affect proper system operation. The critical components in DER-524 are R18, R16, C8, R15, R13 and R11. It is highly recommended that these components be placed very close to the pins of U1 (to minimize long traces which could serve as antenna) and far away as much as possible from any high-voltage and high current nodes in the circuit board to avoid noise coupling.

The BYPASS pin supply capacitor C7 should be placed directly across BYPASS pin and SOURCE pin of U1 for effective noise decoupling.

As shown in Figure 10, minimize the loop areas of the following switching circuit elements to lessen the creation of EMI.

- Loop area formed by the transformer output winding (T1), output rectifier diode (D3) and output capacitor (C10).
- Loop area formed by transformer bias winding (T1), rectifier diode (D2) and filter capacitor (C11).
- Loop area formed by input capacitor (C5), sense resistor R12, internal power MOSFET (U1) and transformer (T1) main winding.

Lastly, unlike discrete MOSFET designs where heat sinking is through the drain tab and which generates significant EMI, LYTSwitch-3 ICs employ low-side switching and the ground potential SOURCE pins are used for heat sinking. This allows the designer to maximize the copper area for good thermal management but without having the risk of increased EMI.

Design Tools

Up-to-date information on design tools can be found at the Power Integrations web site: www.power.com

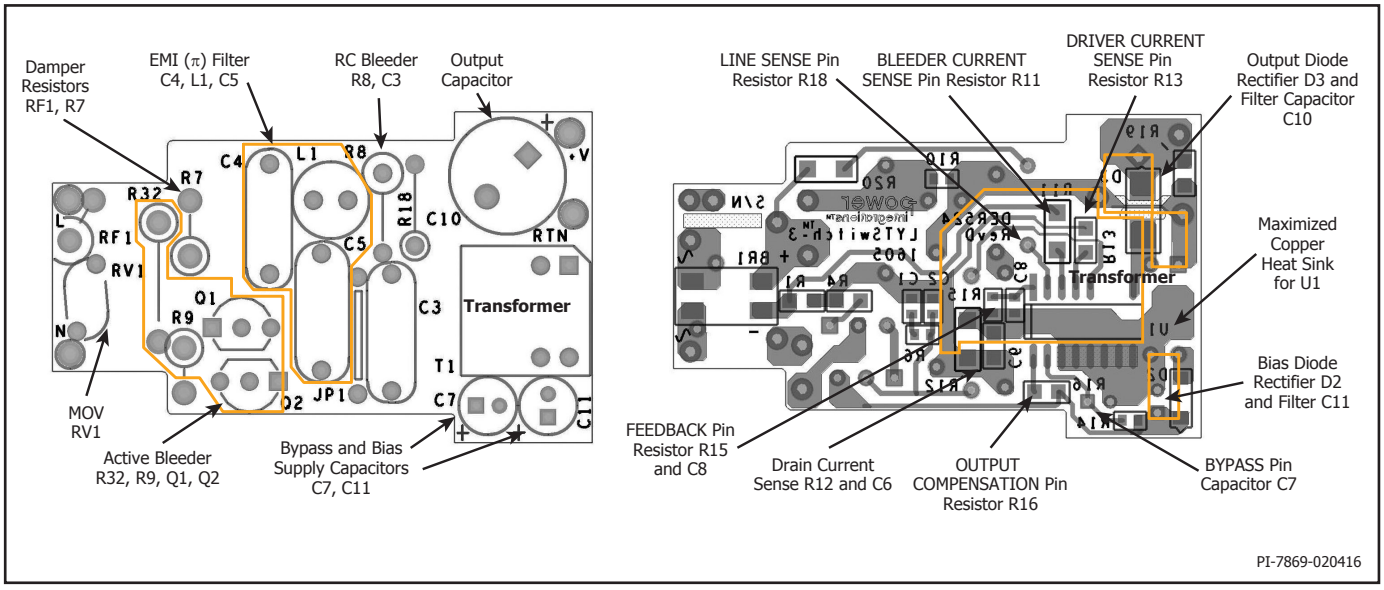


Figure 10. Single-Side PCB Layout Example Showing the Arrangement and Location of Critical Components.

Absolute Maximum Ratings[1,3]

DRAIN Pin Voltage: LYT331x ..... -0.3 V to 650 V
LYT332x ..... -0.3 V to 725 V
DRAIN Pin Peak Current[4] LYT3314 ..... 1.85 A (2.28 A)
LYT3324 ..... 1.44 A (2.33 A)
LYT3315 ..... 2.39 A (2.95 A)
LYT3325 ..... 1.95 A (3.16 A)
LYT3316 ..... 3.25 A (4.00 A)
LYT3326 ..... 2.64 A (4.35 A)
LYT3318 ..... 5.06 A (6.30 A)
LYT3328 ..... 4.16 A (6.86 A)
BP, BS, DS, BL, OC, L DS, FB Pin Voltage ..... -0.3 V to 6.5 V
Lead Temperature[2] ..... 260 °C
Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature ..... -40 to 150 °C

Notes:
1. All voltages referenced to Source, T_A = 25 °C.
2. 1/16 in. from case for 5 seconds.
3. The Absolute Maximum Ratings specified may be applied, one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings for extended periods of time may affect product reliability.
4. The higher peak Drain current (in parentheses) is allowed while the Drain voltage is simultaneously less than 400 V for 725 V integrated MOSFET version, or less than 325 V for 650 V integrated MOSFET version.

Thermal Resistance

Thermal Resistance: SO-16B Package:
(θ_{JA}) ..... 78 °C/W[2]
(θ_{JA}) ..... 68 °C/W[3]
(θ_{JC})[1] ..... 43 °C/W

Notes:
1. Measured on the SOURCE pin close to plastic interface.
2. Soldered to 0.36 sq. inch (232 mm^2) 2 oz. (610 g/m^2) copper clad, with no external heat sink attached.
3. Soldered to 1 sq. in. (645 mm^2), 2 oz, (610 g/m^2) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to +125 °C (Note C) (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Maximum Output Frequency	f_{MAX}	T_J = 25 °C	Average	115.3	124	132.7	kHz
			Peak-to-Peak Jitter		8		%
Minimum Output Frequency	f_{MIN}	T_J = 0 °C to 125 °C	Average		40		kHz
			Peak-to-Peak Jitter		8		%
Frequency Jitter Modulation Rate	f_M	See Note A			1.76		kHz
Maximum On-Time	$T_{ON(MAX)}$	T_J = 25 °C		5.75	6.25	6.75	µs
Minimum On-Time	$T_{ON(MIN)}$	T_J = 25 °C		0.95	1.05	1.15	µs
FEEDBACK Pin Voltage	V_{FB}	T_J = 25 °C		291	300	309	mV
FEEDBACK Pin Voltage Triggering Cycle Skipping	$V_{FB(SK)}$				600		mV
FEEDBACK Pin Overvoltage Threshold	$V_{FB(OV)}$				2000		mV
FEEDBACK Pin Undervoltage Threshold	$V_{FB(UV)}$				22		mV
Feedback Pull-Up Current	I_{FB}			-1.3	-1.0	-0.7	µA

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to +125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
DRAIN Supply Current	I_{S1}	$V_{FB(ON)} > V_{FB} > V_{FB(SK)}$ (MOSFET not switching)			0.8	1.0	mA
	I_{S2}	MOSFET Switching at f_{MAX}	LYT3314		0.9	1.2	mA
			LYT3324		1.0	1.3	
			LYT3315		1.0	1.3	
			LYT3325		1.1	1.4	
			LYT3316		1.1	1.4	
			LYT3326		1.1	1.4	
			LYT3318		1.2	1.5	
			LYT3328		1.3	1.6	
BYPASS Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C	LYT33x4	-8.5	-7.5	-6.0	mA
			LYT33x5-8	-11.5	-9.5	-7.5	
BYPASS Pin Charge Current	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C	LYT33x4	-6.5	-5.2	-4.0	mA
			LYT33x5-8	-8.8	-6.8	-4.8	
BYPASS Pin Voltage	V_{BP}			4.75	5.00	5.25	V
BYPASS Pin Shunt Voltage	V_{SHUNT}	I_{BP} = 5 mA		5.1	5.30	5.5	
BYPASS Pin Power-Up Reset Threshold Voltage	$V_{BP(RESET)}$			4.4	4.6	4.8	V
Circuit Protection							
Current Limit	I_{LIMIT}	di/dt = 662 mA/µs T_J = 25 °C	LYT33x4	843	907	970	mA
		di/dt = 974 mA/µs T_J = 25 °C	LYT33x5	1232	1325	1418	
		di/dt = 1403 mA/µs T_J = 25 °C	LYT33x6	1767	1900	2033	
		di/dt = 2239 mA/µs T_J = 25 °C	LYT33x8	2860	3075	3290	
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C		130	165		ns
Current Limit Delay	T_{ILD}	T_J = 25 °C, See Note A			160		ns
Thermal Foldback Temperature	T_{FB}	See Note A		138	142	146	°C
Thermal Shutdown Temperature	T_{SD}	See Note A		155	160	165	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$	See Note A			75		°C
SOA Switch ON-Time	$T_{ON(SOA)}$	T_J = 25 °C			610	690	ns

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to +125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection (cont.)							
Auto-Restart Current Threshold for Output Undervoltage	I_{OUV}	T_J = 25 °C		40	52	58	µA
Current Threshold for Input Overvoltage	I_{LOV+}	T_J = 25 °C	Threshold	116	120	124	µA
			Hysteresis		5		
Latch-Off Current Threshold for Output Overvoltage	I_{OOV}	T_J = 25 °C		127	134	144	µA
LINE-SENSE Pin Voltage	V_L	I_L = 100 µA, T_J = 25 °C		2.05	2.25	2.45	V
Output							
OUTPUT COMPENSATION Pin Voltage	V_{OC}	I_{OC} = 100 µA T_J = 25 °C		2.05	2.25	2.45	V
ON-State Resistance	$R_{DS(ON)}$	LYT33x4 I_D = 150 mA	T_J = 25 °C		5.40	6.20	Ω
			T_J = 100 °Cdrdxd		8.40	9.70	
		LYT33x5 I_D = 200 mA	T_J = 25 °C		3.80	4.35	
			T_J = 100 °C		5.70	6.55	
		LYT33x6 I_D = 300 mA	T_J = 25 °C		2.75	3.15	
			T_J = 100 °C		4.25	4.90	
		LYT33x8 I_D = 500 mA	T_J = 25 °C		1.75	2.00	
			T_J = 100 °C		2.70	3.10	
OFF-State Leakage	I_{DSS}	V_{BP} = 5.3 V, V_{FB} > $V_{FB(SK)}$, V_{DS} = 580 V T_J = 125 °C				200	µA
Breakdown Voltage	BV_{DSS}	V_{BP} = 5.3 V, V_{FB} > $V_{FB(SK)}$ T_J = 25 °C	LYT331x	650			V
			LYT332x	725			

NOTES:
A. Guaranteed by design.

Typical Performance Curves

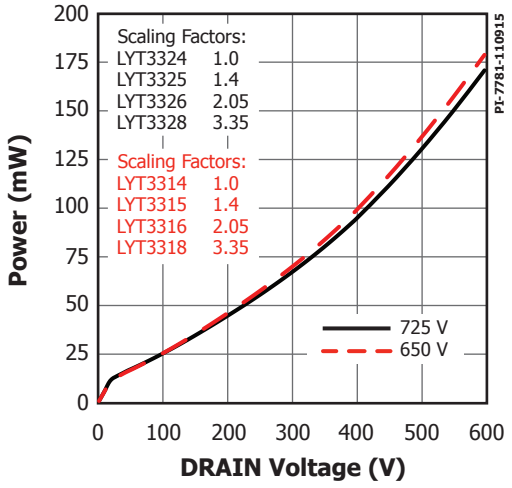


Figure 11. Power vs. Drain Voltage.

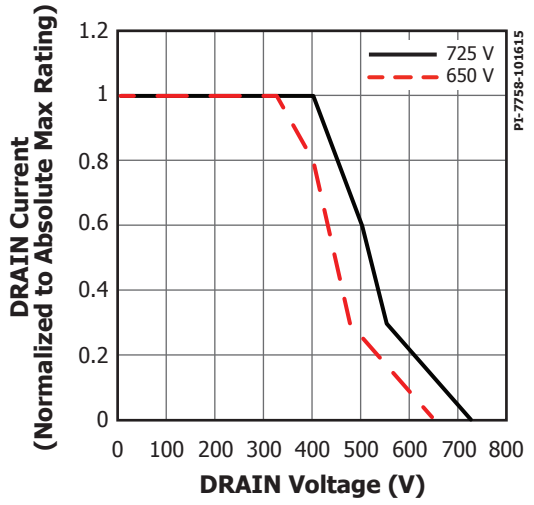


Figure 12. Maximum Allowable Drain Current vs. Drain Voltage.

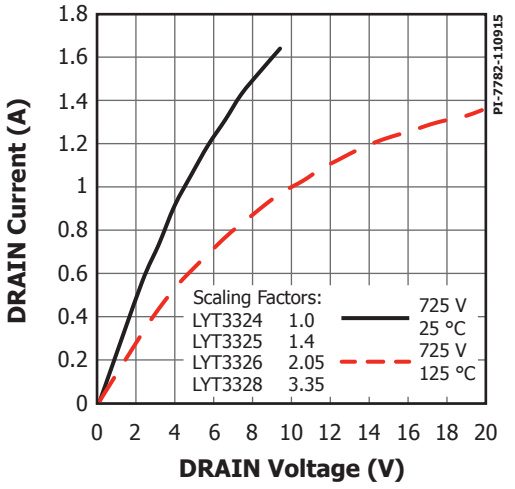


Figure 13. Drain Current vs. Drain Voltage.

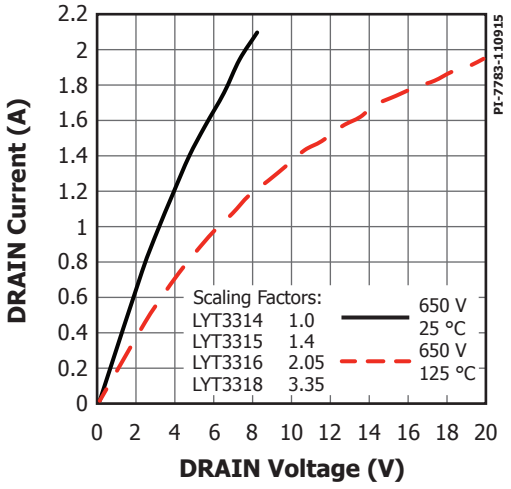


Figure 14. Drain Current vs. Drain Voltage.

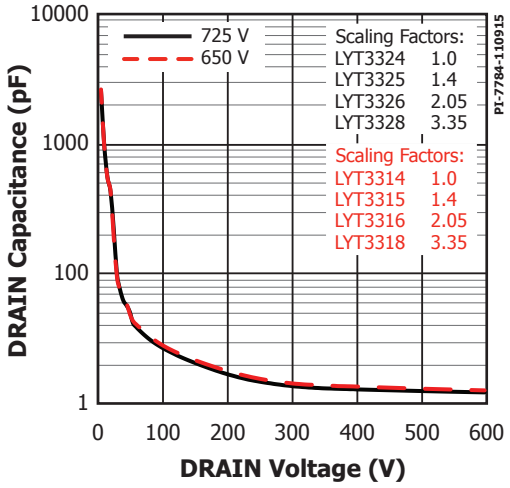
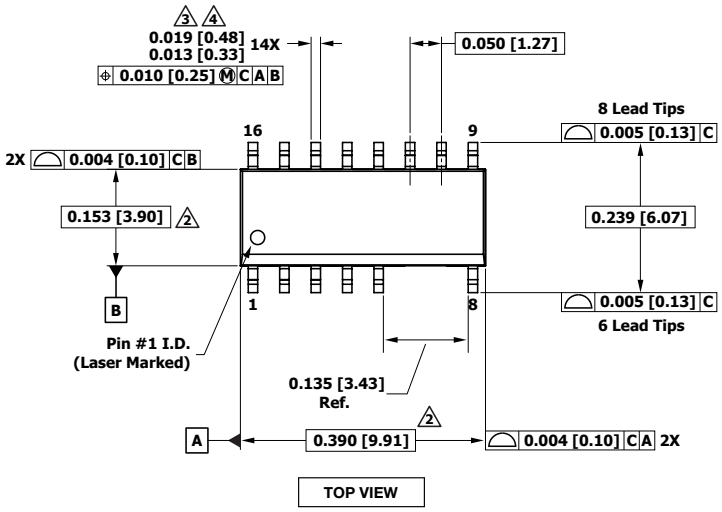
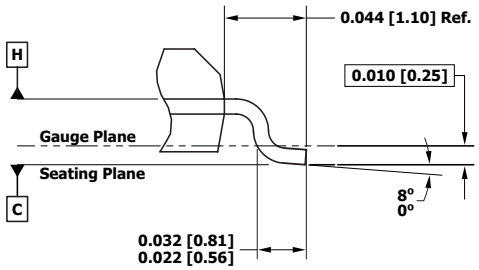


Figure 15. Drain Capacitance vs. DRAIN Pin Voltage.

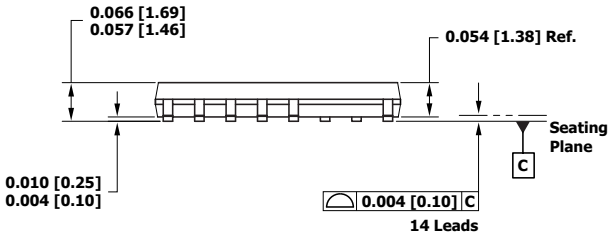
SO-16B



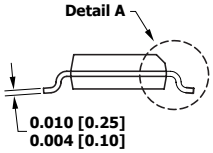
TOP VIEW



DETAIL A



SIDE VIEW



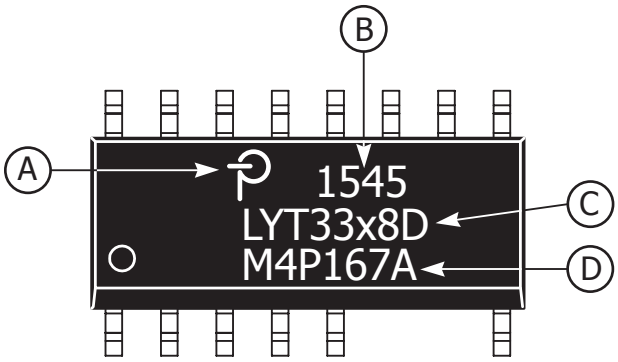
END VIEW

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and inter-lead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.25 mm per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Dimensions in Inches [mm].
6. Datums A and B to be determined in Datum H.
7. JEDEC reference: MS – 012.

PI-7473-061515
POD-SO-16B Rev A

PACKAGE MARKING

SO-16B



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code

PI-7801-111915

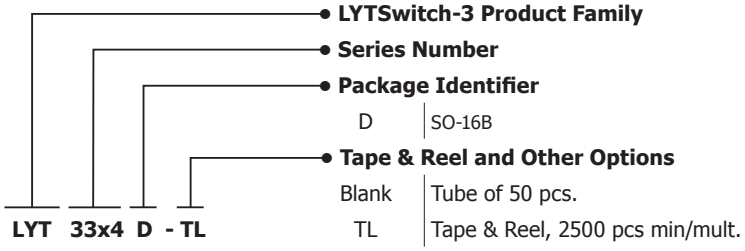
MSL Table

Part Number	MSL Rating
LYT33x4	3
LYT33x5	3
LYT33x6	3
LYT33x8	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 2.5 kV (max) on all pins
Human Body Model ESD	JESD22-A114F	> ±2000 V on all pins
Machine Model ESD	JESD22-A115CA	> ±200 V on all pins

Part Ordering Information



Notes

Revision	Notes	Date
A	Code S Release.	09/15
B	Added Block diagram and Typical Performance Curves.	11/09/15
C	Code A Release.	02/16
D	Corrected I_{S2} parameter. Added V_{OC} and V_L parameters.	03/16
D	$T_{ON(MAX)}$ parameter errors fixed.	04/01/16

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