



PBSS4260PANS

60 V, 2 A NPN/NPN low V_{CEsat} double transistor

30 September 2025

Product data sheet

1. General description

NPN/NPN low V_{CEsat} double transistor in a leadless medium power DFN2020D-6 (SOT1118D) Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

PNP/PNP complement: PBSS5260PAPS

2. Features and benefits

- Very low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain h_{FE} at high I_C
- Reduced Printed-Circuit Board (PCB) requirements
- Exposed heat sink for excellent thermal and electrical conductivity
- High energy efficiency due to less heat generation
- Suitable for Automatic Optical Inspection (AOI) of solder joints

3. Applications

- Load switch
- Battery-driven devices
- Power management
- Charging circuits
- LED lighting
- Power switches (e.g. motors, fans)

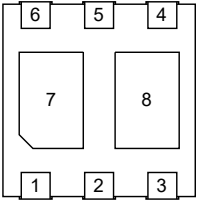
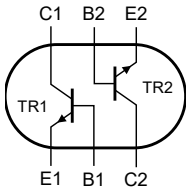
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	60	V
I_C	collector current		-	-	2	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	3	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = 1$ A; $I_B = 50$ mA; pulsed; $t_p \leq 300$ μ s; $\delta \leq 0.02$; $T_{amb} = 25$ °C	-	-	200	m Ω

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 Transparent top view DFN2020D-6 (SOT1118D)	 sym140
2	B1	base TR1		
3	C2	collector TR2		
4	E2	emitter TR2		
5	B2	base TR2		
6	C1	collector TR1		
7	C1	collector TR1		
8	C2	collector TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBSS4260PANS	DFN2020D-6	plastic, leadless thermally enhanced ultra thin and small outline package with side-wettable flanks (SWF); 6 terminals; 0.65 mm pitch; 2 mm x 2 mm x 0.65 mm body	SOT1118D

7. Marking

Table 4. Marking codes

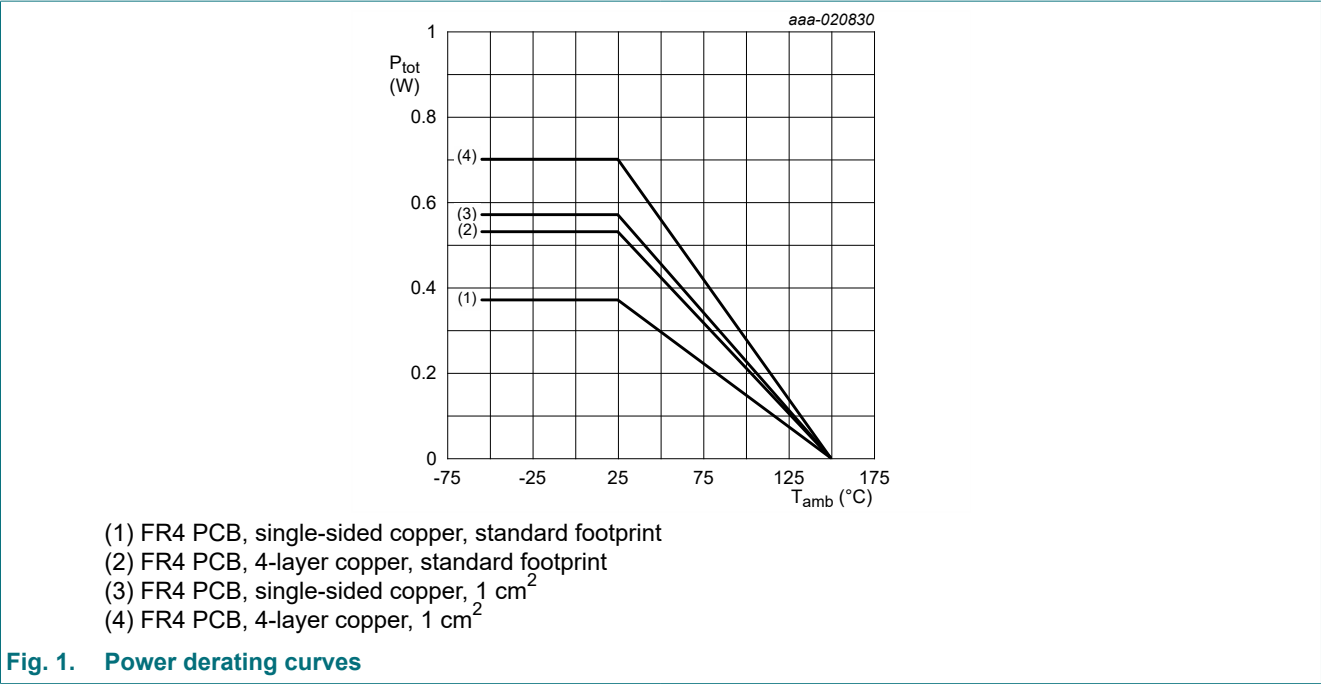
Type number	Marking code
PBSS4260PANS	3L

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V _{CBO}	collector-base voltage	open emitter		-	60	V
V _{CEO}	collector-emitter voltage	open base		-	60	V
V _{EBO}	emitter-base voltage	open collector		-	7	V
I _C	collector current			-	2	A
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms		-	3	A
I _B	base current			-	0.3	A
I _{BM}	peak base current	single pulse; t _p ≤ 1 ms		-	1	A
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	370	mW
			[2]	-	570	mW
			[3]	-	530	mW
			[4]	-	700	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	510	mW
			[2]	-	780	mW
			[3]	-	730	mW
			[4]	-	960	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single sided copper, tin-plated; mounting pad for collector 1 cm².
[3] Device mounted on an FR4 Printed-Circuit Board (PCB), 4-layer copper, tin-plated and standard footprint.
[4] Device mounted on an FR4 Printed-Circuit Board (PCB), 4-layer copper, tin-plated; mounting pad for collector 1 cm².

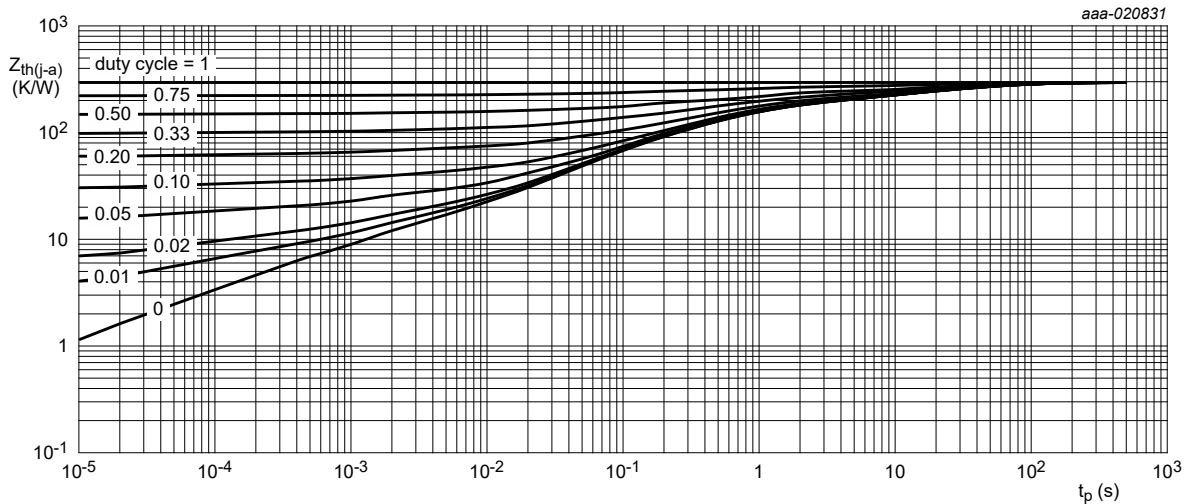


9. Thermal characteristics

Table 6. Thermal characteristics

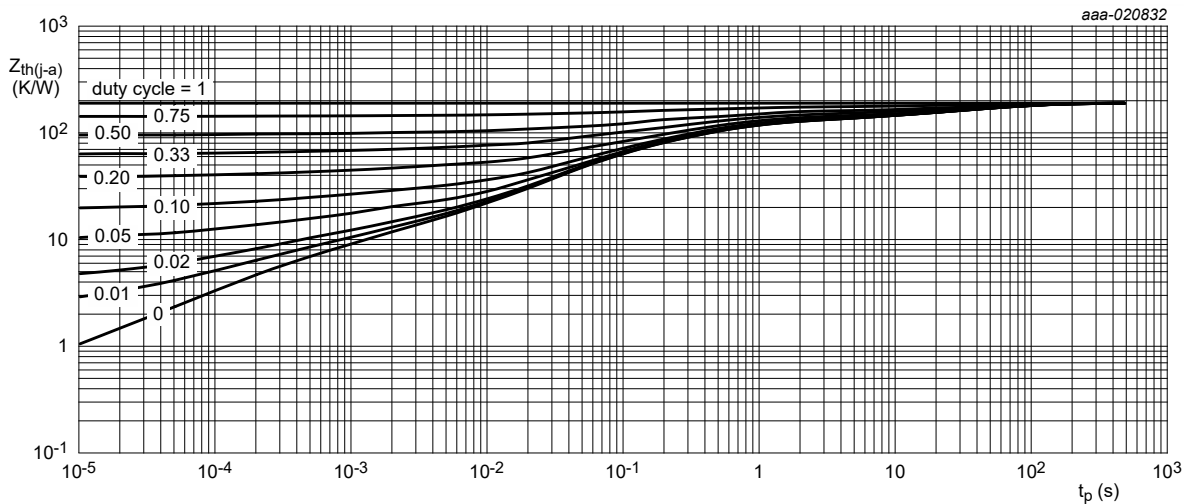
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	338	K/W
			[2]	-	-	219	K/W
			[3]	-	-	236	K/W
			[4]	-	-	179	K/W
Per device							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	246	K/W
			[2]	-	-	161	K/W
			[3]	-	-	172	K/W
			[4]	-	-	131	K/W

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for collector 1 cm².
[3] Device mounted on an FR4 Printed-Circuit Board (PCB), 4-layer copper, tin-plated and standard footprint.
[4] Device mounted on an FR4 Printed-Circuit Board (PCB), 4-layer copper, tin-plated, mounting pad for collector 1 cm².



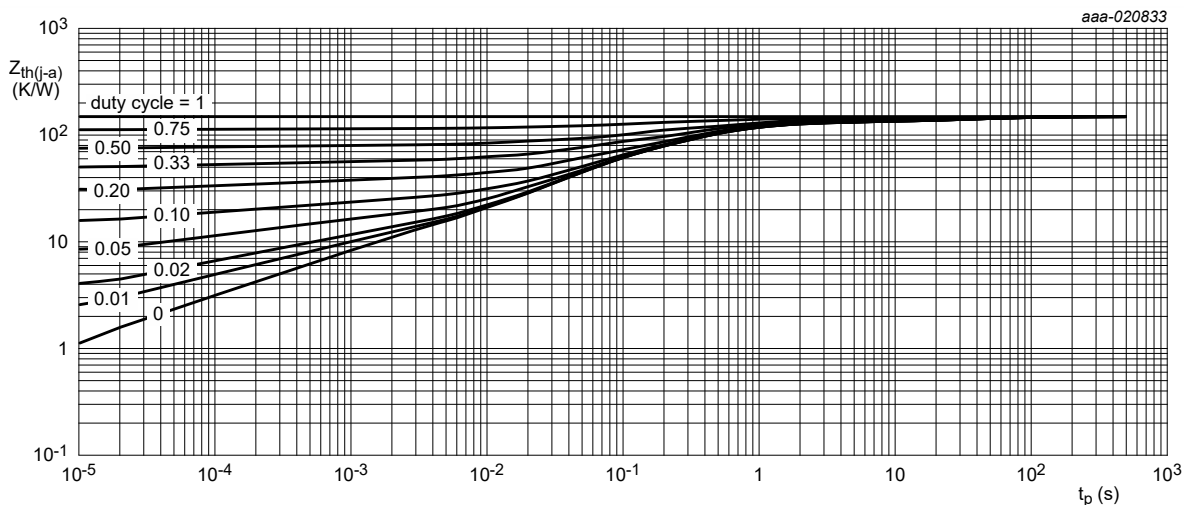
FR4 PCB, standard footprint

Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



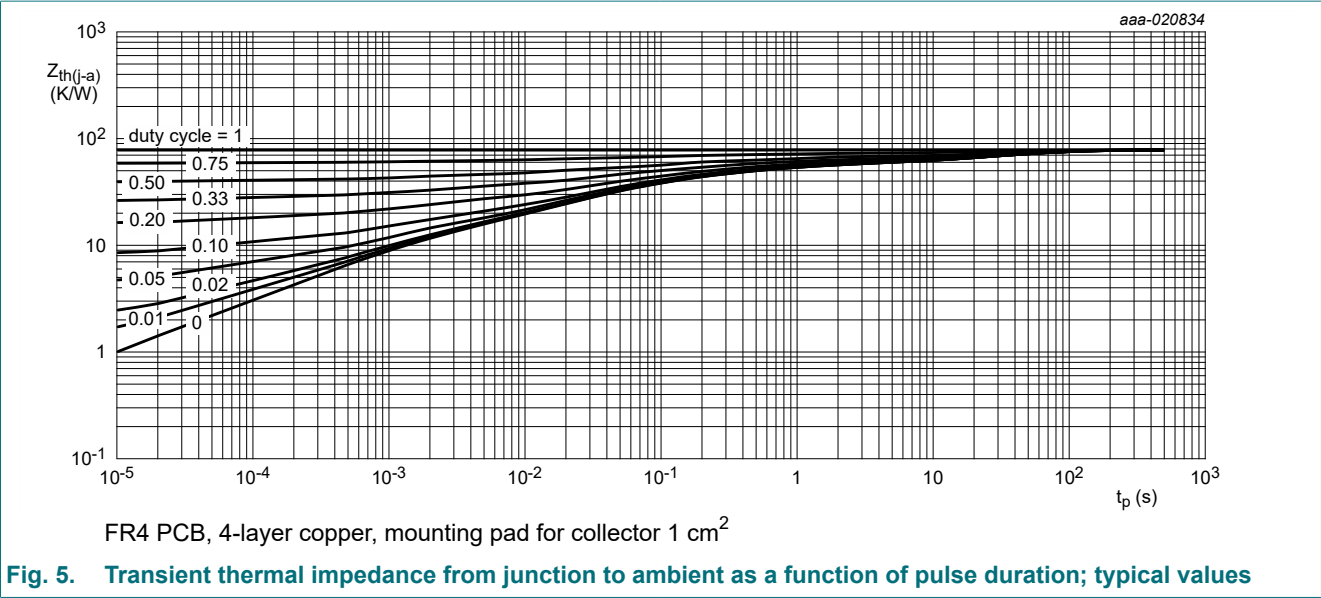
FR4 PCB, mounting pad for collector 1 cm²

Fig. 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, 4-layer copper, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
I_{CBO}	collector-base cut-off current	$V_{CB} = 48 \text{ V}; I_E = 0 \text{ A}; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	-	100	nA
		$V_{CB} = 48 \text{ V}; I_E = 0 \text{ A}; T_j = 150 \text{ }^{\circ}\text{C}$		-	-	50	μA
I_{CES}	collector-emitter cut-off current	$V_{CE} = 48 \text{ V}; V_{BE} = 0 \text{ V}; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	-	100	nA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_C = 0 \text{ A}; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	-	100	nA
h_{FE}	DC current gain	$V_{CE} = 2 \text{ V}; I_C = 100 \text{ mA}; \text{pulsed}; t_p \leq 300 \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^{\circ}\text{C}$		250	400	-	
		$V_{CE} = 2 \text{ V}; I_C = 500 \text{ mA}; \text{pulsed}; t_p \leq 300 \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^{\circ}\text{C}$		210	330	-	
		$V_{CE} = 2 \text{ V}; I_C = 1 \text{ A}; \text{pulsed}; t_p \leq 300 \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^{\circ}\text{C}$		120	190	-	
		$V_{CE} = 2 \text{ V}; I_C = 2 \text{ A}; \text{pulsed}; t_p \leq 300 \mu\text{s}; \delta \leq 0.02$		50	80	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 0.5 \text{ A}; I_B = 50 \text{ mA}; \text{pulsed}; t_p \leq 300 \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	70	100	mV
		$I_C = 1 \text{ A}; I_B = 50 \text{ mA}; \text{pulsed}; t_p \leq 300 \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	140	200	mV
		$I_C = 2 \text{ A}; I_B = 200 \text{ mA}; \text{pulsed}; t_p \leq 300 \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	260	350	mV
R_{CEsat}	collector-emitter saturation resistance	$I_C = 1 \text{ A}; I_B = 50 \text{ mA}; \text{pulsed}; t_p \leq 300 \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	-	200	m Ω
V_{BEsat}	base-emitter saturation voltage	$I_C = 0.5 \text{ A}; I_B = 50 \text{ mA}; \text{pulsed}; t_p \leq 300 \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	0.92	1	V
		$I_C = 1 \text{ A}; I_B = 50 \text{ mA}; \text{pulsed}; t_p \leq 300 \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	0.96	1.1	V
		$I_C = 2 \text{ A}; I_B = 200 \text{ mA}; \text{pulsed}; t_p \leq 300 \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	1.18	1.3	V
V_{BE}	base-emitter voltage	$V_{CE} = 2 \text{ V}; I_C = 0.5 \text{ A}; \text{pulsed}; t_p \leq 300 \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	0.77	0.9	V
t_d	delay time	$I_C = 1 \text{ A}; I_{B(on)} = 50 \text{ mA}; I_{B(off)} = -50 \text{ mA}; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	10	-	ns
t_r	rise time			-	140	-	ns
t_{on}	turn-on time			-	150	-	ns
t_s	storage time			-	445	-	ns
t_f	fall time			-	180	-	ns
t_{off}	turn-off time			-	625	-	ns
f_T	transition frequency	$V_{CE} = 10 \text{ V}; I_C = 500 \text{ mA}; f = 100 \text{ MHz}; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	140	-	MHz
C_c	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = 0 \text{ A}; i_e = 0 \text{ A}; f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	6.5	-	pF

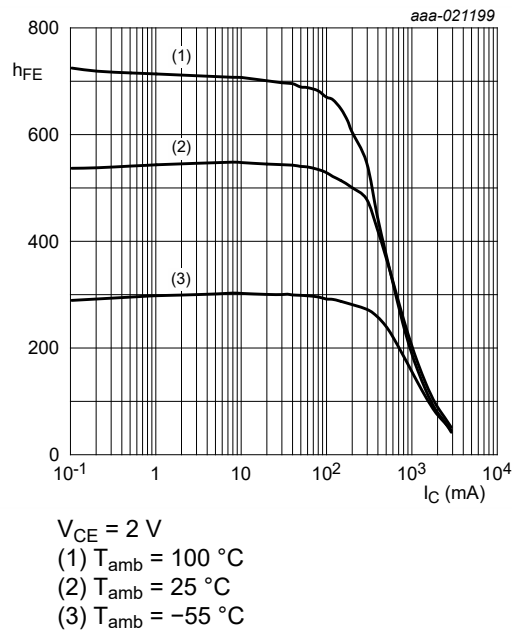


Fig. 6. DC current gain as a function of collector current; typical values

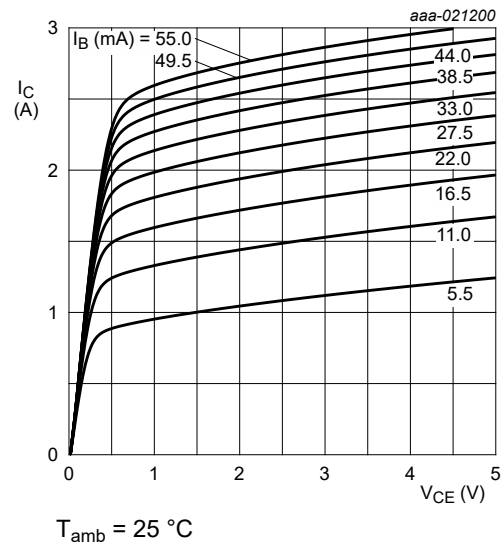


Fig. 7. Collector current as a function of collector-emitter voltage; typical values

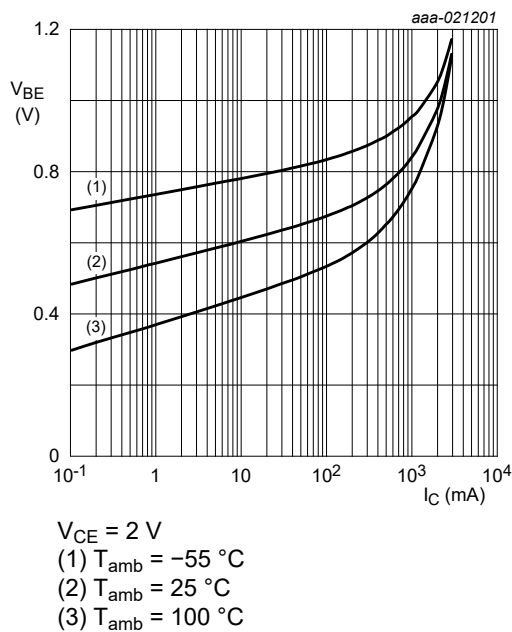


Fig. 8. Base-emitter voltage as a function of collector current; typical values

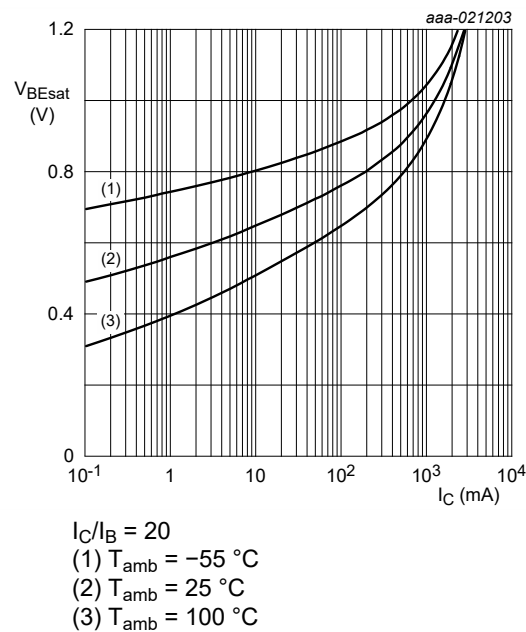


Fig. 9. Base-emitter saturation voltage as a function of collector current; typical values

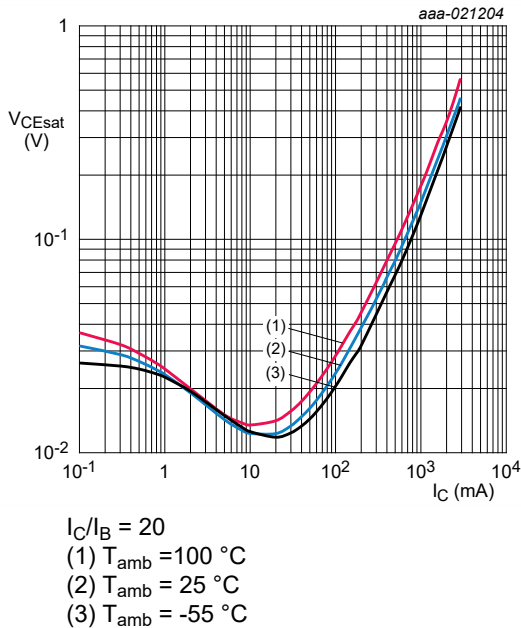


Fig. 10. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

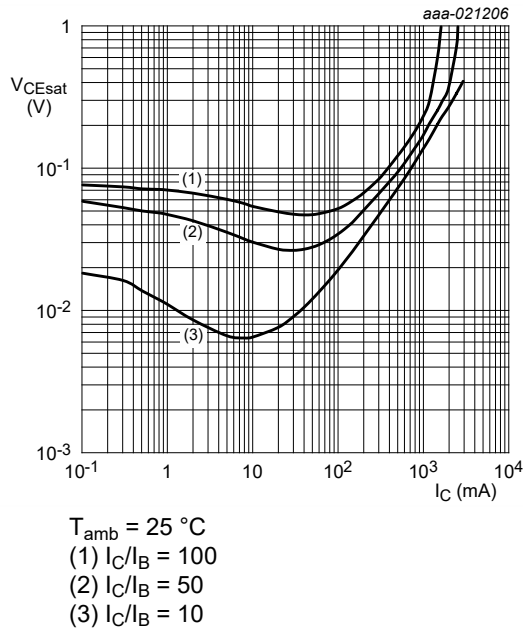


Fig. 11. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

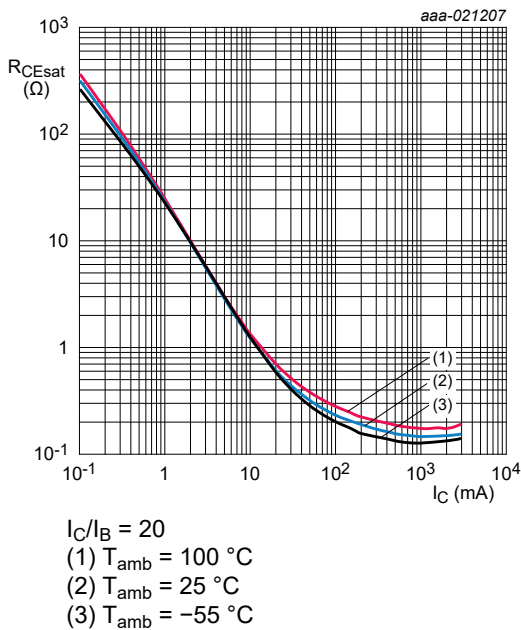


Fig. 12. Collector-emitter saturation resistance as a function of collector current; typical values

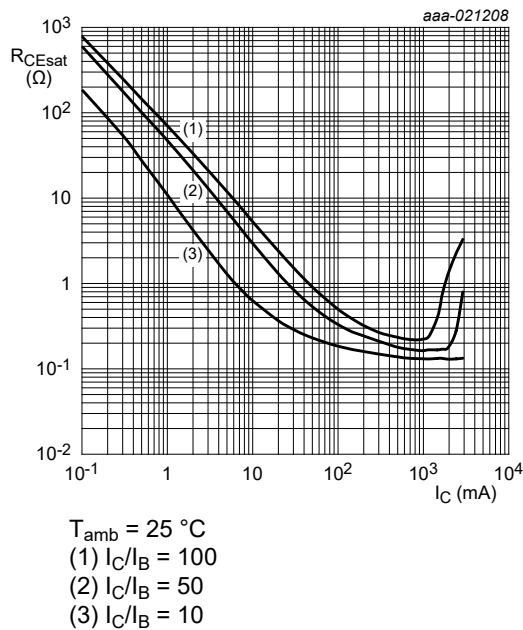


Fig. 13. Collector-emitter saturation resistance as a function of collector current; typical values

11. Test information

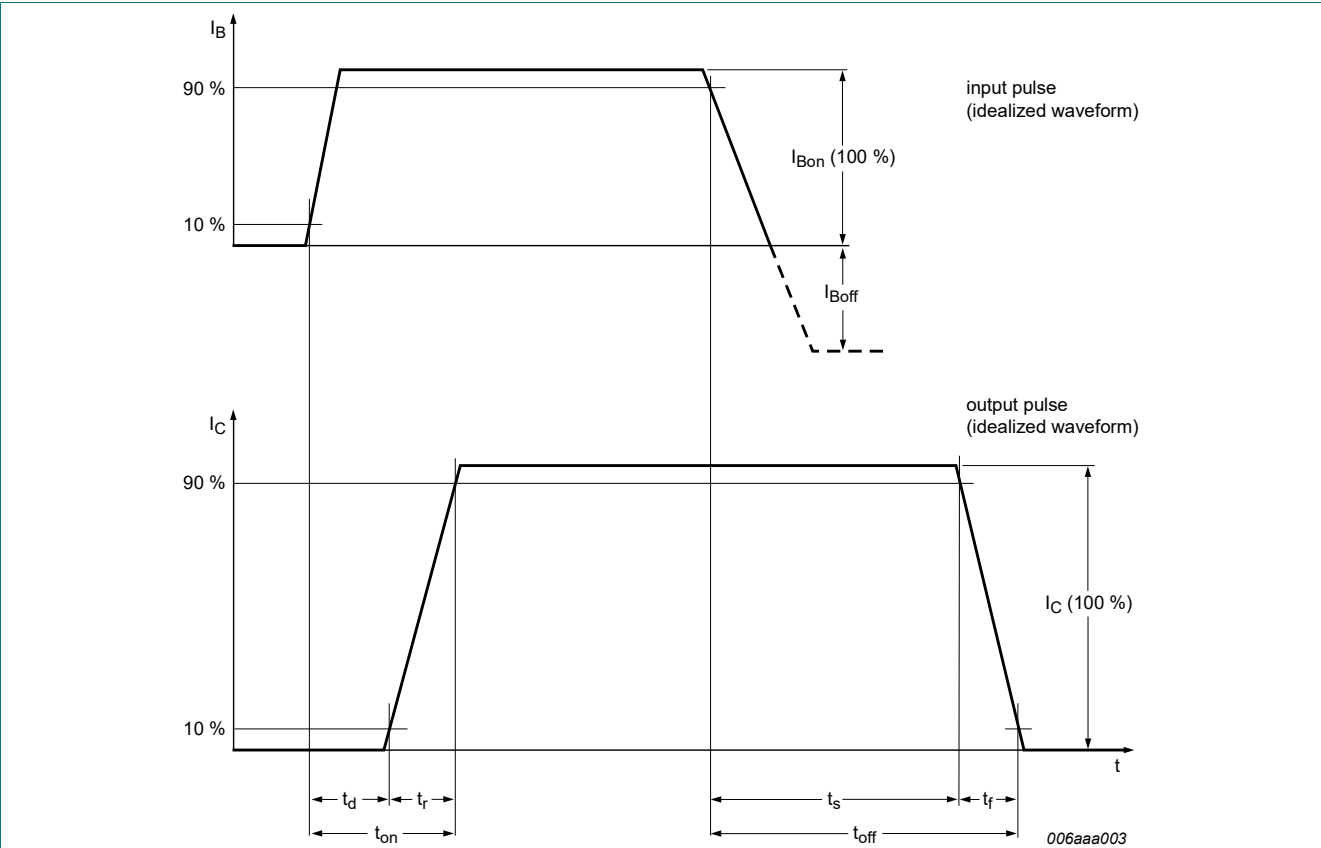


Fig. 14. Switching time definition

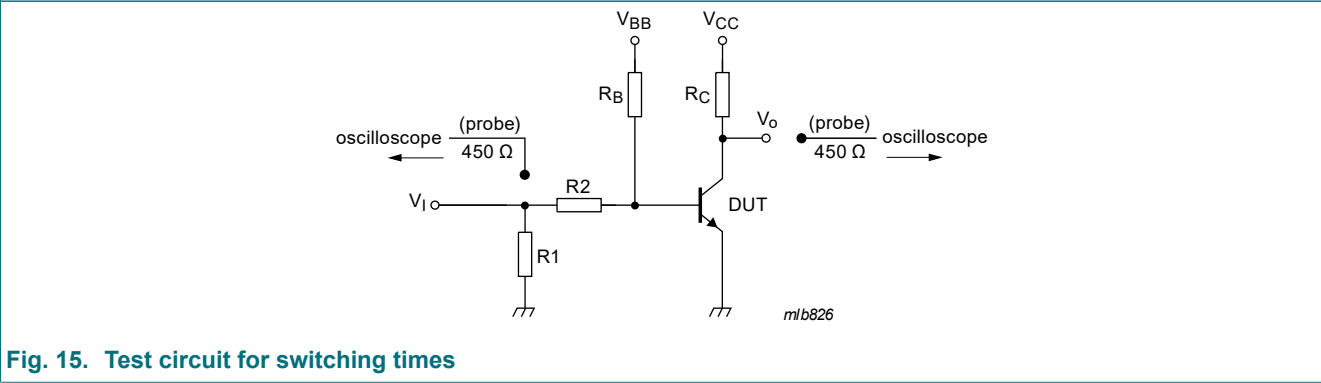
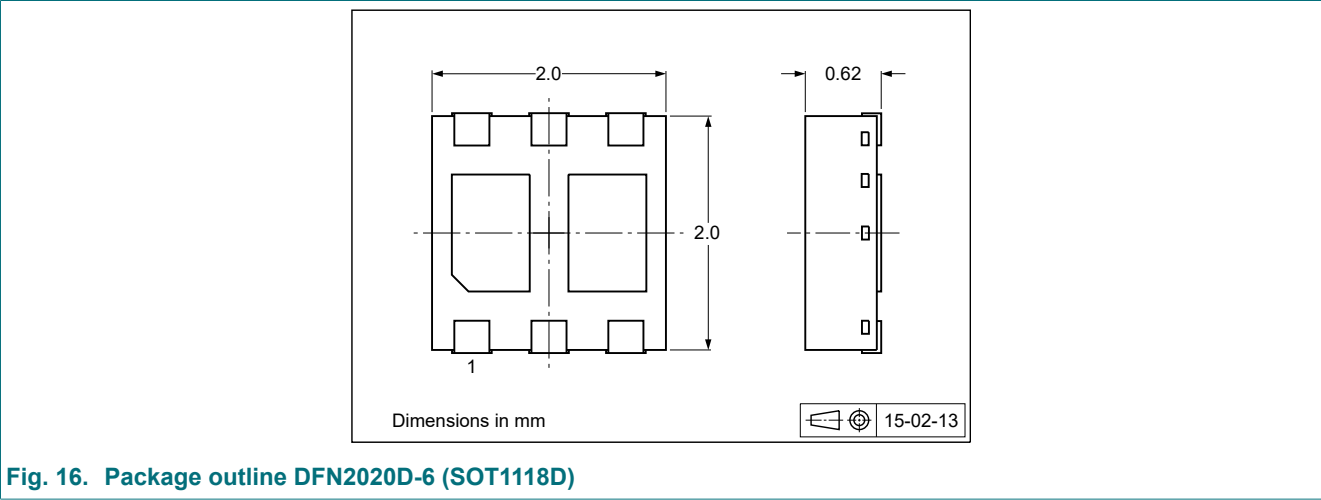
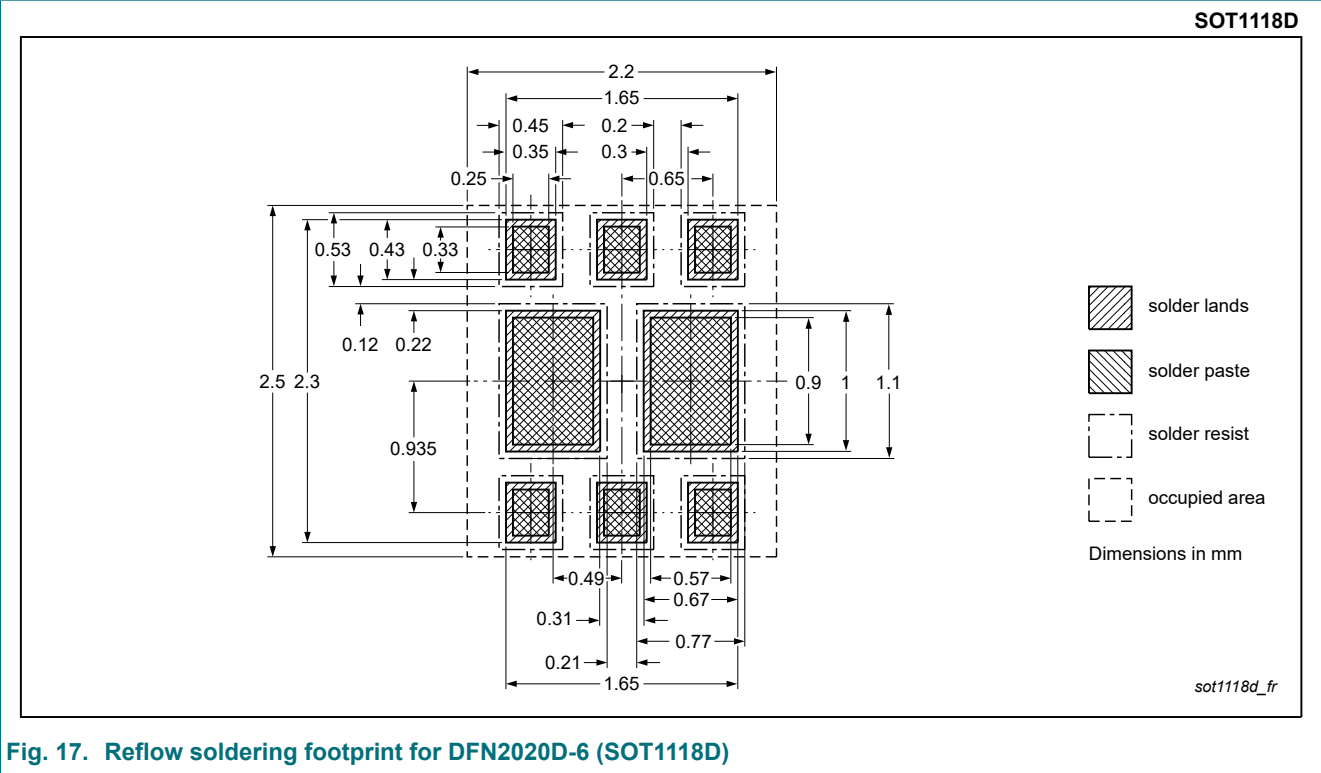


Fig. 15. Test circuit for switching times

12. Package outline



13. Soldering



14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4260PANS v.2	20250930	Product data sheet	-	PBSS4260PANS v.1
Modifications:	Product(s) changed to non-automotive qualification. Please refer to nexperia.com for automotive (-Q) product alternative(s).			
PBSS4260PANS v.1	20151215	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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