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Kind regards,

Team Nexperia



BSS84AKMB

50 V, single P-channel Trench MOSFET

Rev. 1 — 6 June 2012

Product data sheet

1. Product profile

1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1006B-3 (SOT883B) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Logic-level compatible
- Very fast switching
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection up to 1 kV
- Ultra thin package profile with 0.37 mm height

1.3 Applications

- Relay driver
- High-speed line driver
- High-side load switch
- Switching circuits

1.4 Quick reference data

Table 1. Quick reference data

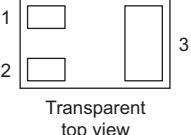
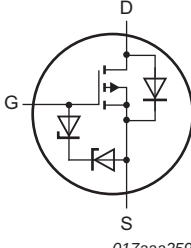
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$	-	-	-50	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = -10\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-230	mA
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}$; $I_D = -100\text{ mA}$; $T_j = 25\text{ }^{\circ}\text{C}$	-	4.5	7.5	Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm².



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SOT883B (DFN1006B-3)	 017aaa259
2	S	source		
3	D	drain		

3. Ordering information

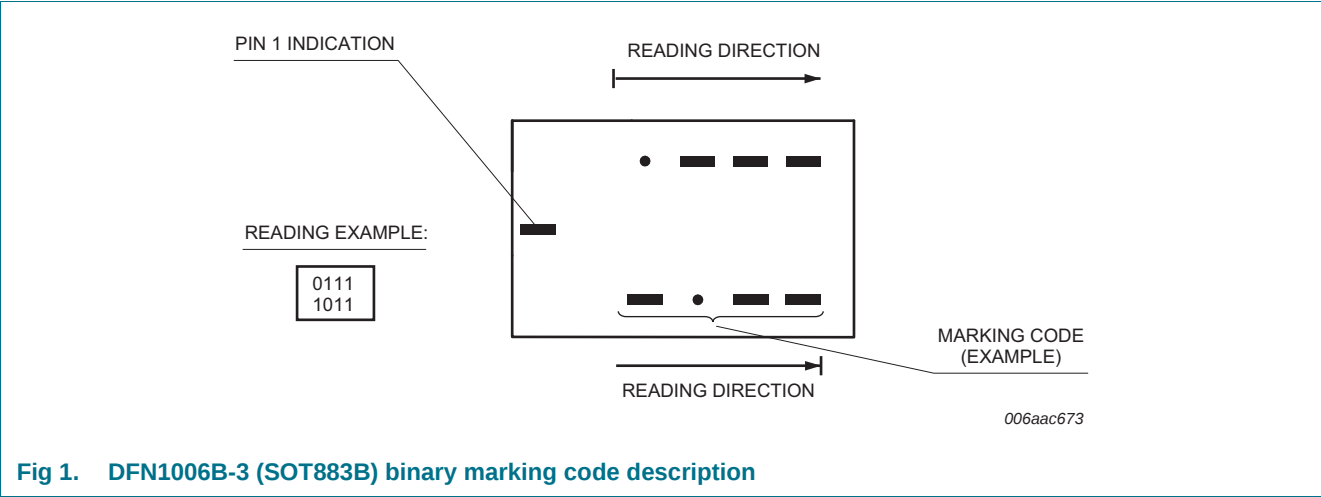
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BSS84AKMB	DFN1006B-3	Leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.37 mm	SOT883B

4. Marking

Table 4. Marking codes

Type number	Marking code
BSS84AKMB	0000 0010



5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$	-	-50	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = -10\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-230	mA
		$V_{GS} = -10\text{ V}; T_{amb} = 100\text{ }^{\circ}\text{C}$	[1]	-150	mA
I_{DM}	peak drain current	$T_{amb} = 25\text{ }^{\circ}\text{C}$; single pulse; $t_p \leq 10\text{ }\mu\text{s}$	-	-0.9	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[2]	360	mW
			[1]	715	mW
		$T_{sp} = 25\text{ }^{\circ}\text{C}$	-	2700	mW
T_j	junction temperature		-55	150	$^{\circ}\text{C}$
T_{amb}	ambient temperature		-55	150	$^{\circ}\text{C}$
T_{stg}	storage temperature		-65	150	$^{\circ}\text{C}$

Source-drain diode

I_S	source current	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-230	mA
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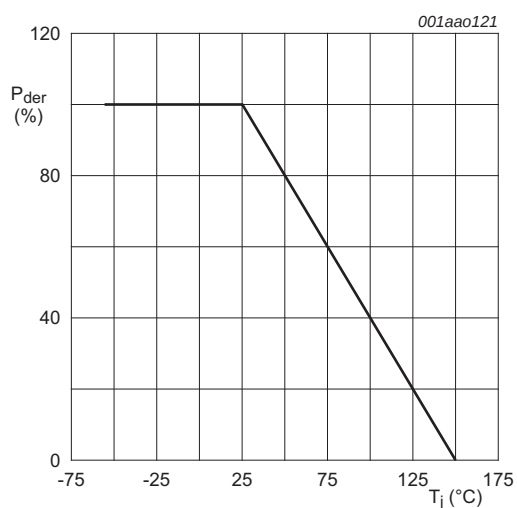
ESD maximum rating

V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	1000	V
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[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm².

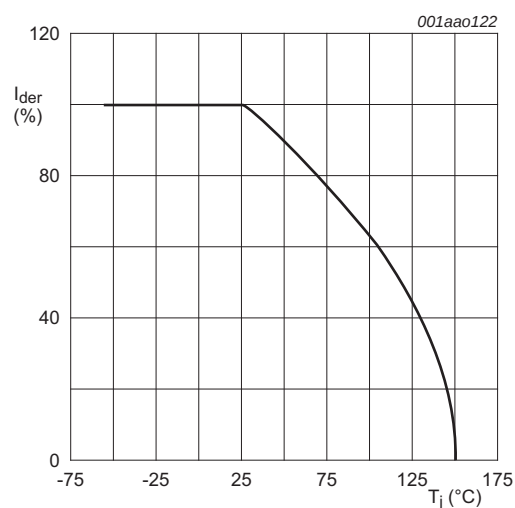
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.



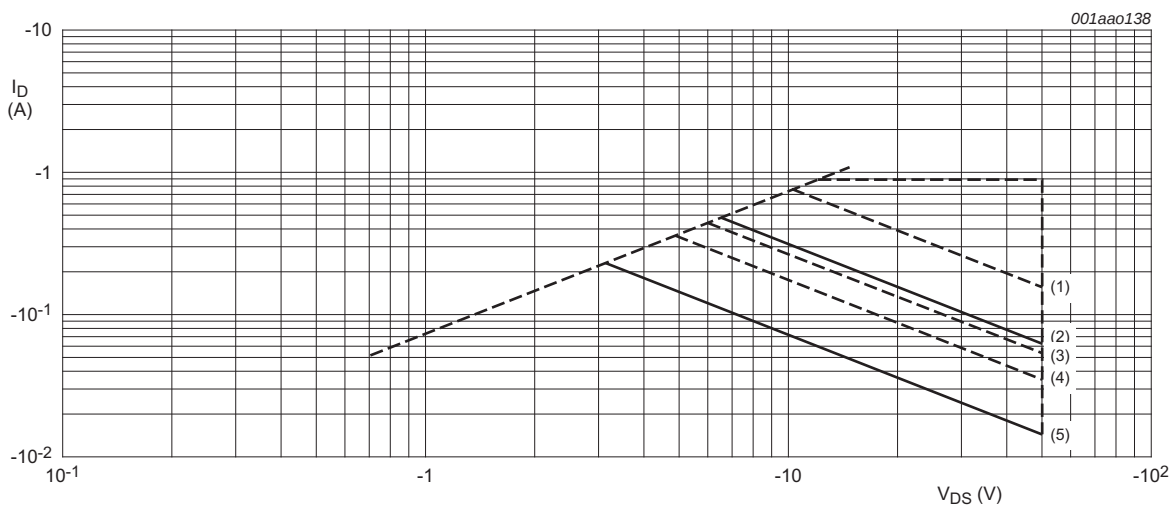
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

Fig 3. Normalized continuous drain current as a function of junction temperature



I_{DM} is single pulse
(1) $t_p = 1\text{ ms}$
(2) DC; $T_{sp} = 25\text{ }^{\circ}\text{C}$
(3) $t_p = 10\text{ ms}$
(4) $t_p = 100\text{ ms}$
(5) DC; $T_{amb} = 25\text{ }^{\circ}\text{C}$; drain mounting pad 1 cm^2

Fig 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	305	350 K/W
			[2]	-	150	175 K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	40	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm^2 .

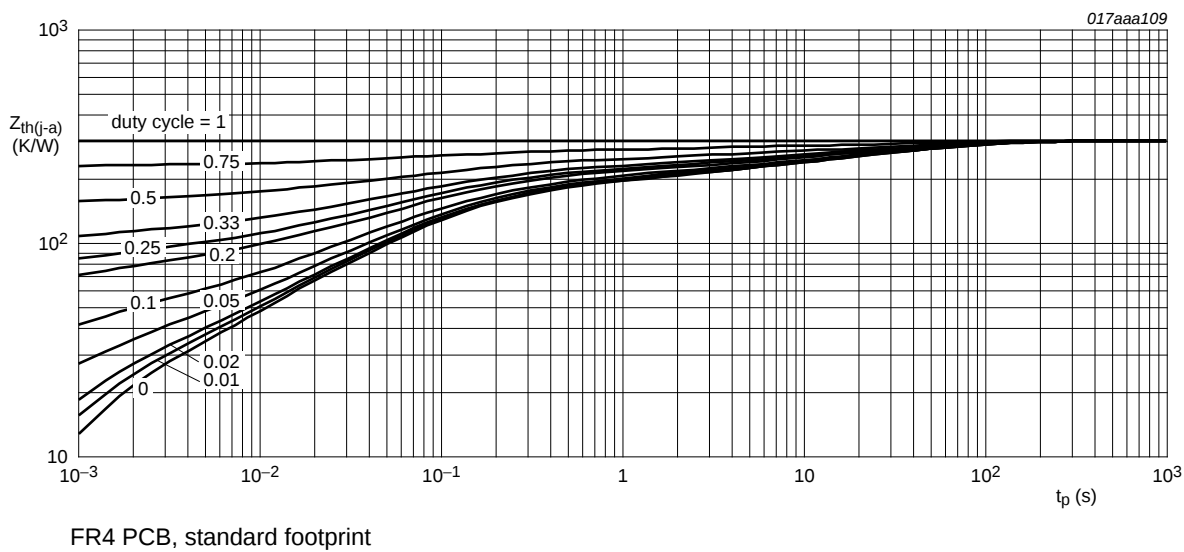


Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

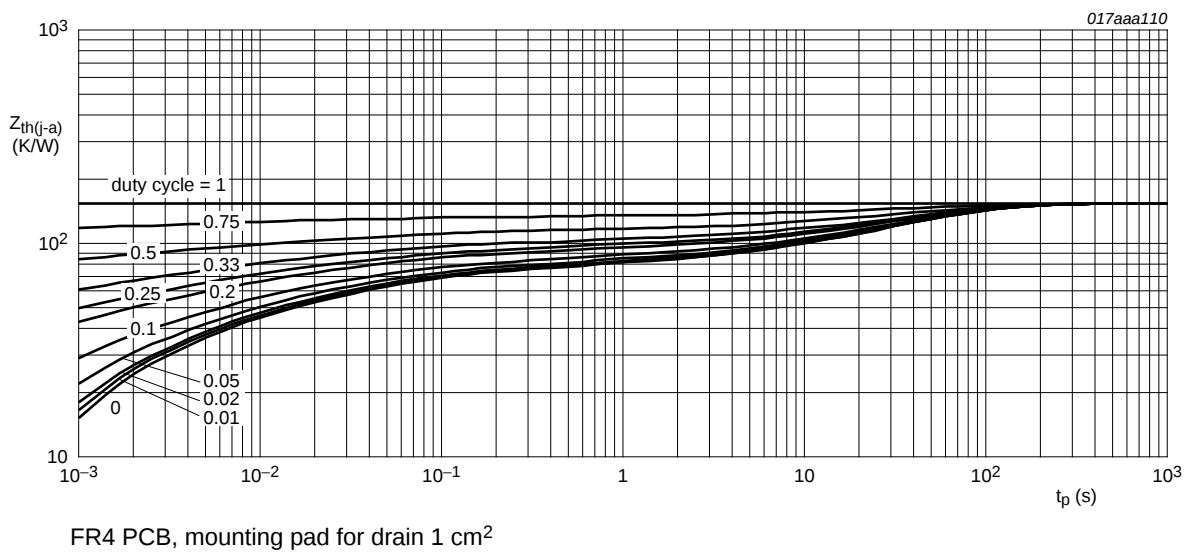
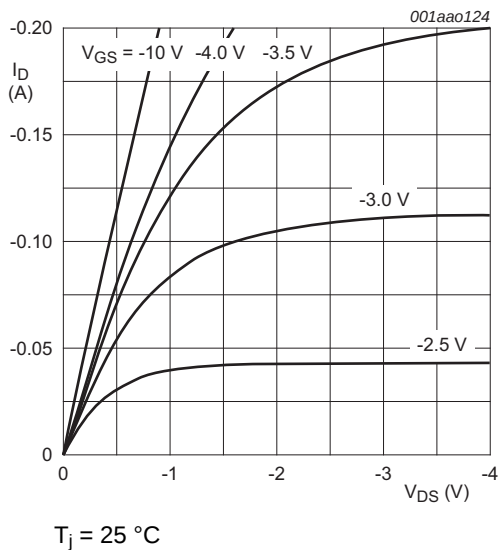


Fig 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

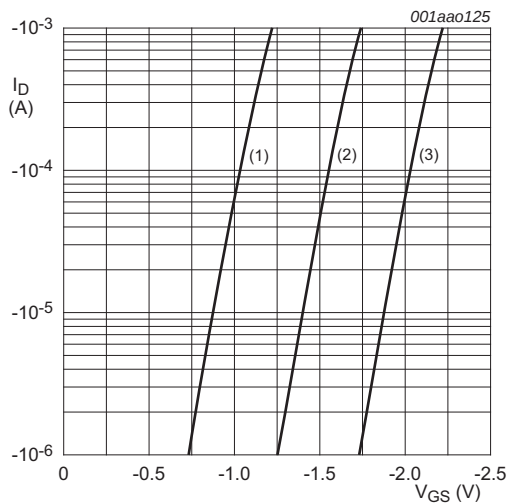
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	-50	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu A$; $V_{DS} = V_{GS}$; $T_j = 25 ^\circ C$	-1.1	-1.6	-2.1	V
I_{DSS}	drain leakage current	$V_{DS} = -50 V$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	-	-	-1	μA
		$V_{DS} = -50 V$; $V_{GS} = 0 V$; $T_j = 150 ^\circ C$	-	-	-2	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	-	-10	μA
		$V_{GS} = 20 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	-	-10	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -10 V$; $I_D = -100 mA$; $T_j = 25 ^\circ C$	-	4.5	7.5	Ω
		$V_{GS} = -10 V$; $I_D = -100 mA$; $T_j = 150 ^\circ C$	-	8	13.5	Ω
		$V_{GS} = -5 V$; $I_D = -100 mA$; $T_j = 25 ^\circ C$	-	5.7	8.5	Ω
g_{fs}	forward transconductance	$V_{DS} = -10 V$; $I_D = -100 mA$; $T_j = 25 ^\circ C$	-	150	-	mS
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -25 V$; $I_D = -200 mA$; $V_{GS} = -5 V$; $T_j = 25 ^\circ C$	-	0.26	0.35	nC
Q_{GS}	gate-source charge		-	0.12	-	nC
Q_{GD}	gate-drain charge	$V_{DS} = -10 V$; $I_D = -200 mA$; $V_{GS} = -5 V$; $T_j = 25 ^\circ C$	-	0.09	-	nC
C_{iss}	input capacitance	$V_{DS} = -25 V$; $f = 1 MHz$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	-	24	36	pF
C_{oss}	output capacitance		-	4.5	-	pF
C_{rss}	reverse transfer capacitance		-	1.3	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -30 V$; $R_L = 250 \Omega$; $V_{GS} = -10 V$; $R_{G(ext)} = 6 \Omega$; $T_j = 25 ^\circ C$	-	13	26	ns
t_r	rise time		-	11	-	ns
$t_{d(off)}$	turn-off delay time		-	48	96	ns
t_f	fall time		-	25	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = -115 mA$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	-0.48	-0.85	-1.2	V



T_j = 25 °C

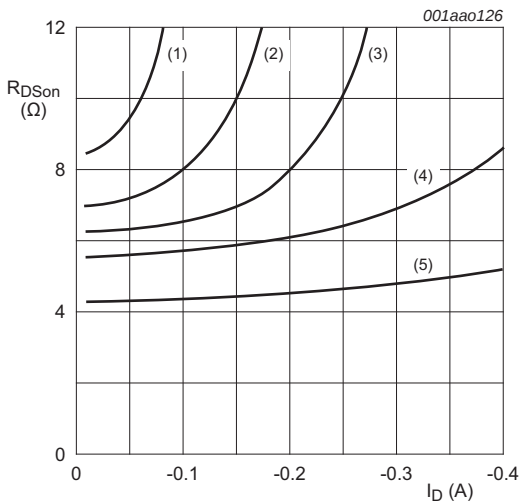
Fig 7. Output characteristics; drain current as a function of drain-source voltage; typical values



T_j = 25 °C; V_{DS} = -5 V

- (1) minimum values
- (2) typical values
- (3) maximum values

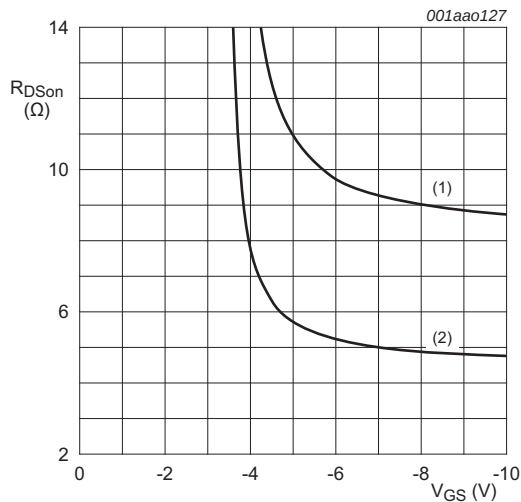
Fig 8. Subthreshold drain current as a function of gate-source voltage



T_j = 25 °C

- (1) V_{GS} = -3.0 V
- (2) V_{GS} = -3.5 V
- (3) V_{GS} = -4.0 V
- (4) V_{GS} = -5.0 V
- (5) V_{GS} = -10.0 V

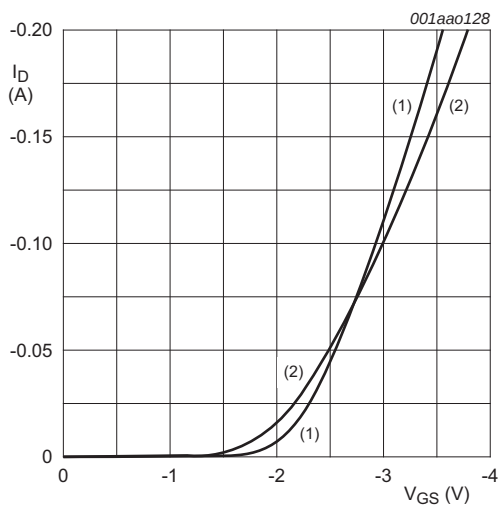
Fig 9. Drain-source on-state resistance as a function of drain current; typical values



I_D = -200 mA

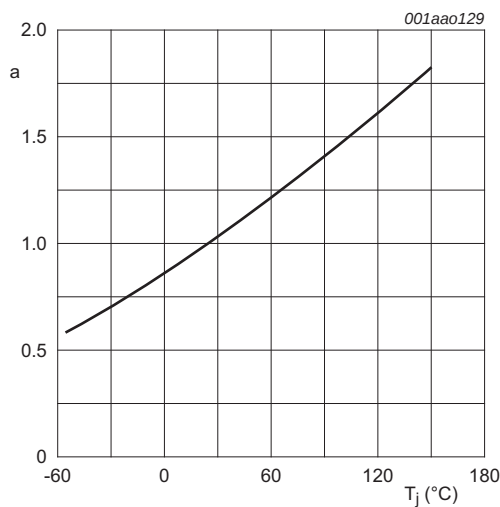
- (1) T_j = 150 °C
- (2) T_j = 25 °C

Fig 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



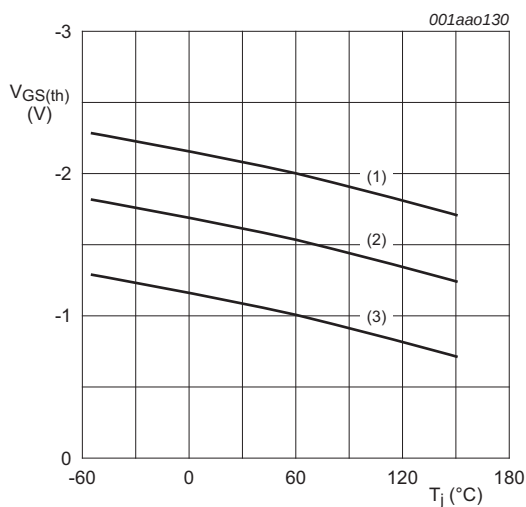
$V_{DS} > I_D \times R_{DSon}$
(1) $T_j = 25\text{ }^{\circ}\text{C}$
(2) $T_j = 150\text{ }^{\circ}\text{C}$

Fig 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values



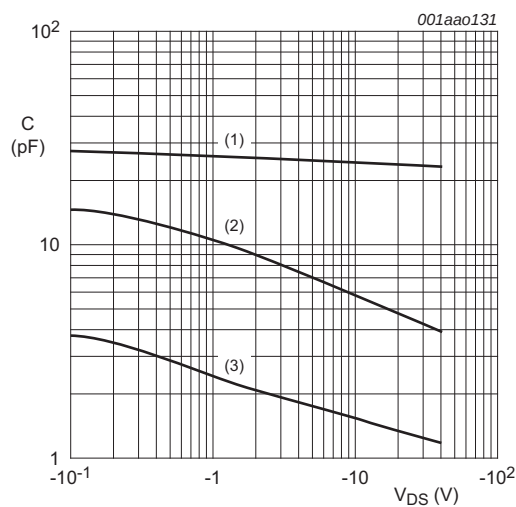
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values



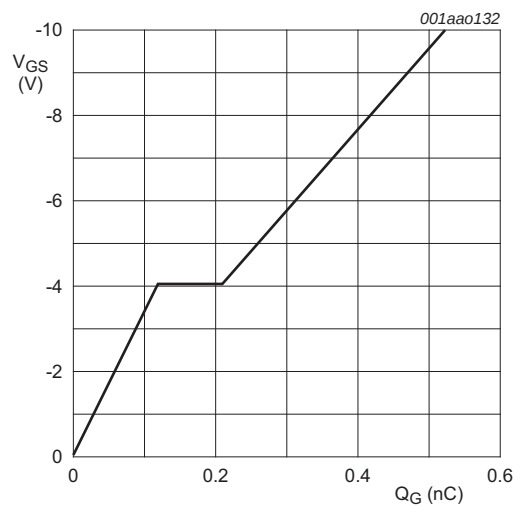
$I_D = -0.25\text{ mA}$; $V_{DS} = V_{GS}$
(1) maximum values
(2) typical values
(3) minimum values

Fig 13. Gate-source threshold voltage as a function of junction temperature



$f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$
(1) C_{iss}
(2) C_{oss}
(3) C_{rss}

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = -0.2$ A; $V_{DS} = -25$ V; $T_{amb} = 25$ °C

Fig 15. Gate-source voltage as a function of gate charge; typical values

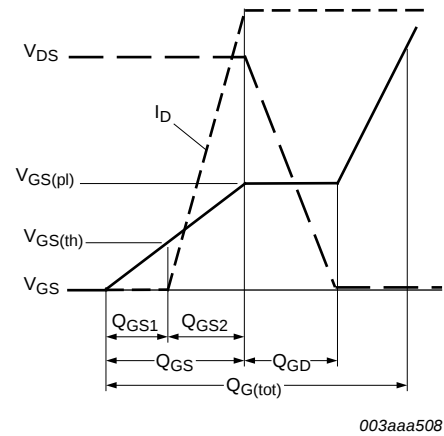
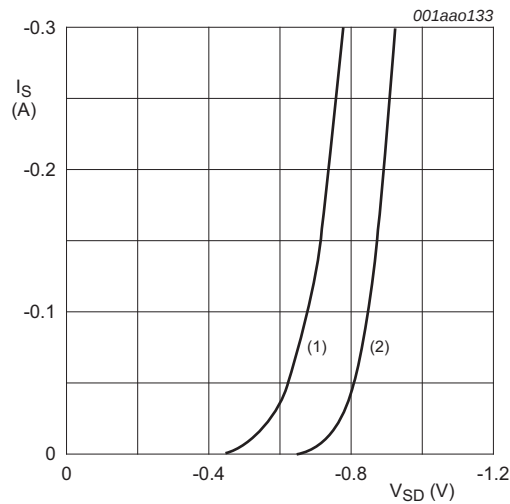


Fig 16. Gate charge waveform definitions



$V_{GS} = 0$ V
(1) $T_j = 150$ °C
(2) $T_j = 25$ °C

Fig 17. Source current as a function of source-drain voltage; typical values

8. Test information

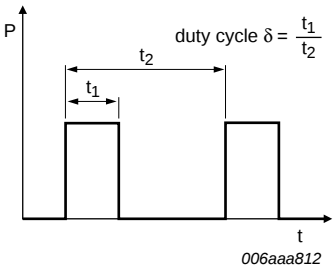


Fig 18. Duty cycle definition

9. Package outline

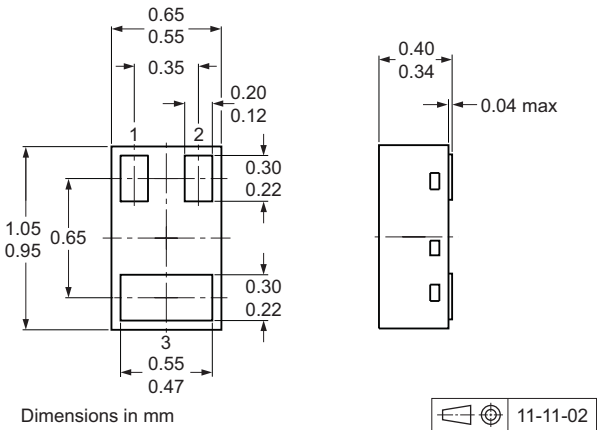
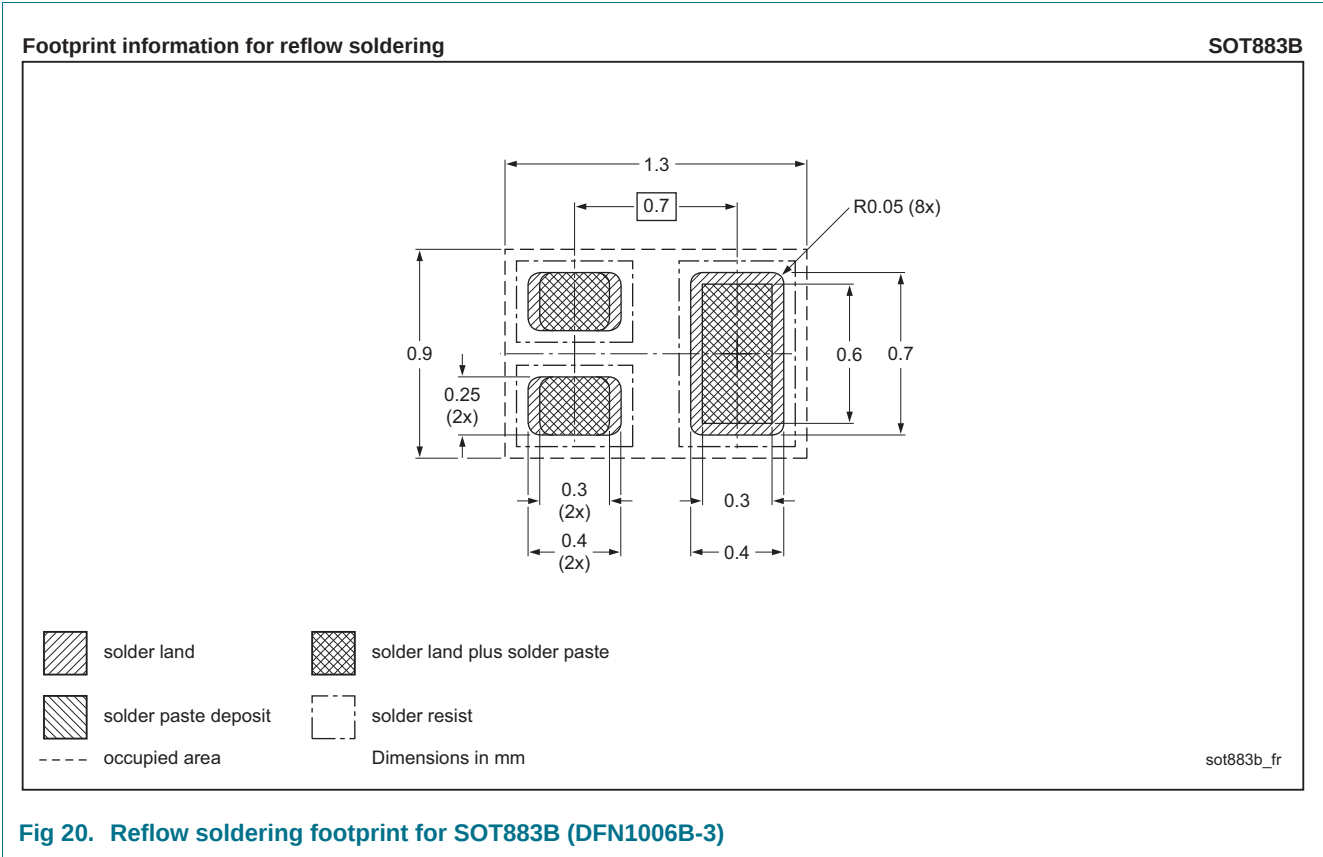


Fig 19. Package outline SOT883B (DFN1006B-3)

10. Soldering



11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BSS84AKMB v.1	20120606	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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