OptiMOS™ Power-MOSFET

Features

- Optimized for high performance Buck converter (Server,VGA)
- Very Low FOM_{QOSS} for High Frequency SMPS
- Low FOM_{SW} for High Frequency SMPS
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

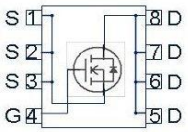
Pb-Free RoHS Halogen-Free

Product Summary

V_{DS}		25	V
$R_{DS(on),max}$	V_{GS}=10 V	1.8	mΩ
	V_{GS}=4.5 V	2.4	
I_D		40	A

PG-TSDSON-8
(fused leads)

Type	Package	Marking
BSZ018NE2LS	PG-TSDSON-8 (fused leads)	018NE2L



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS}=10 V, T_C=25 °C	40	A
		V_{GS}=10 V, T_C=100 °C	40	
		V_{GS}=4.5 V, T_C=25 °C	40	
		V_{GS}=4.5 V, T_C=100 °C	40	
		V_{GS}=4.5 V, T_A=25 °C, R_{thJA}=60 K/W	23	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C	160	
Avalanche current, single pulse[3]	I_{AS}	T_C=25 °C	20	
Avalanche energy, single pulse	E_{AS}	I_D=20 A, R_{GS}=25 Ω	150	mJ
Gate source voltage	V_{GS}		±20	V

[1] J-STD20 and JESD22
[2] See figure 3 for more detailed information
[3] See figure 13 for more detailed information

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
	P_{tot}	T_C=25 °C	69	W
		T_A=25 °C, R_{thJA}=60 K/W	2.1	
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	1.8	K/W
Device on PCB	R_{thJA}	6 cm^2 cooling area[4)]	-	-	60	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	25	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250 µA	1.2	-	2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=25 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=25 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=30 A	-	1.9	2.4	mΩ
		V_{GS}=10 V, I_D=30 A	-	1.5	1.8	
Gate resistance	R_G		0.4	0.8	1.6	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=30 A	70	140	-	S

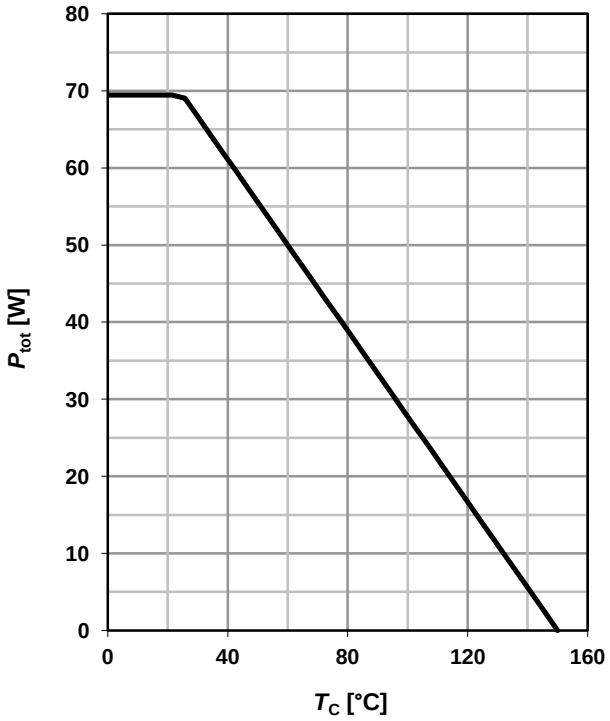
[4)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=12 V, f=1 MHz	-	2800	3724	pF
Output capacitance	C_{oss}		-	1000	1330	
Reverse transfer capacitance	C_{rss}		-	110	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=12 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω	-	5.5	-	ns
Rise time	t_r		-	4.4	-	
Turn-off delay time	$t_{d(off)}$		-	26	-	
Fall time	t_f		-	3.4	-	
Gate Charge Characteristics[5)]						
Gate to source charge	Q_{gs}	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V	-	7.0	9.3	nC
Gate charge at threshold	$Q_{g(th)}$		-	4.5	-	
Gate to drain charge	Q_{gd}		-	4.3	6.5	
Switching charge	Q_{sw}		-	6.7	-	
Gate charge total	Q_g		-	18.6	25	
Gate plateau voltage	$V_{plateau}$		-	2.5	-	V
Gate charge total	Q_g	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 10 V	-	39	52	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V	-	16.2	-	
Output charge	Q_{oss}	V_{DD}=12 V, V_{GS}=0 V	-	21	28	
Reverse Diode						
Diode continuous forward current	I_S	T_C=25 °C	-	-	40	A
Diode pulse current	$I_{S,pulse}$		-	-	160	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=20 A, T_j=25 °C	-	0.8	1	V
Reverse recovery charge	Q_{rr}	V_R=15 V, I_F=I_S, di_F/dt=400 A/µs	-	20	-	nC

[5)] See figure 16 for gate charge parameter definition

1 Power dissipation

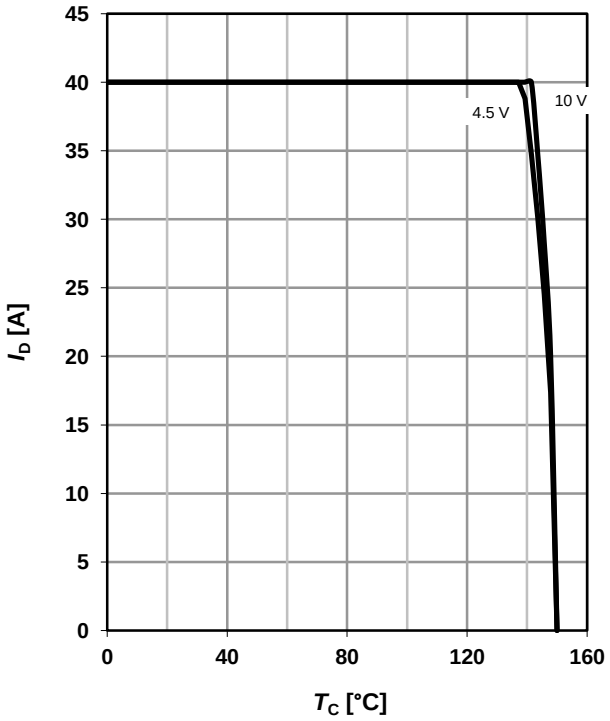
$P_{tot}=f(T_C)$



2 Drain current

$I_D=f(T_C)$

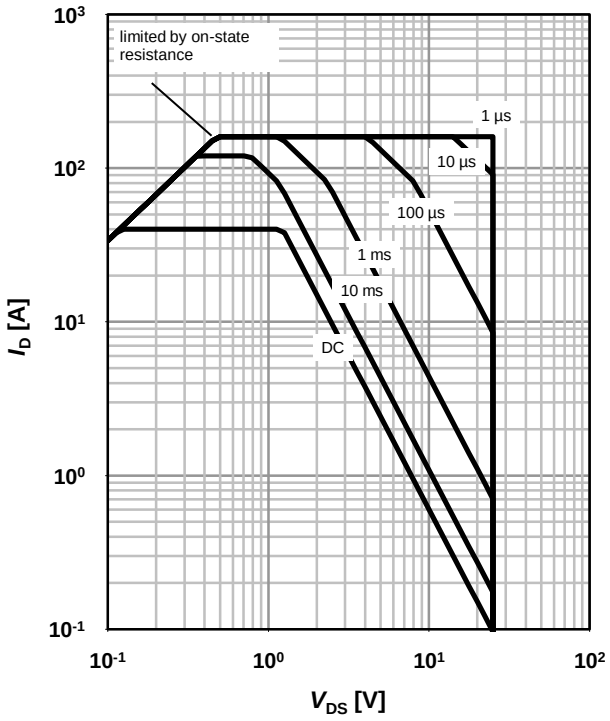
parameter: V_{GS}



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

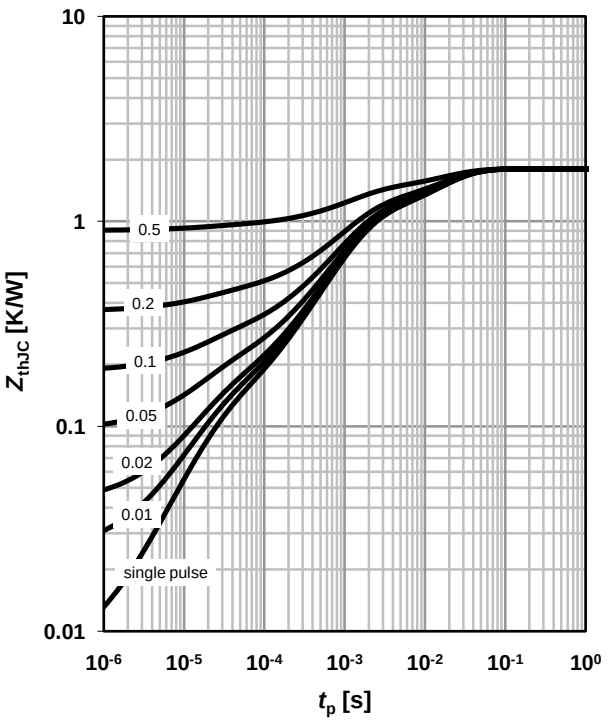
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

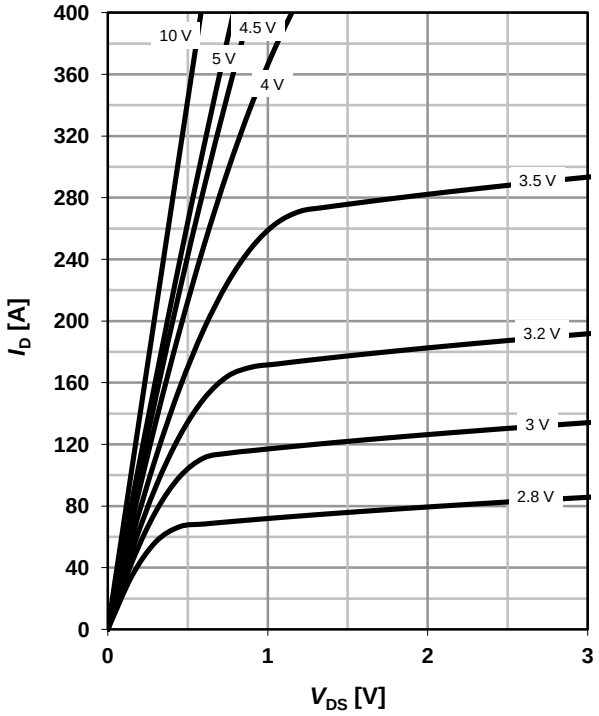
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=25$ °C

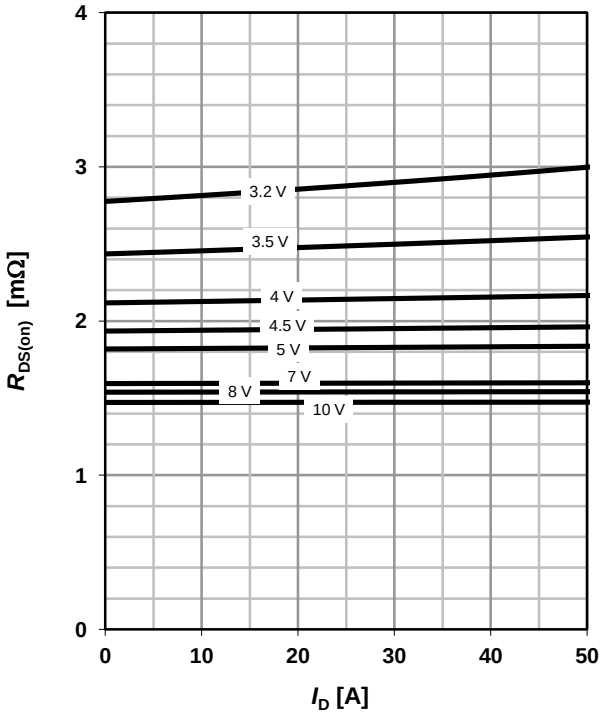
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}=f(I_D)$; $T_j=25$ °C

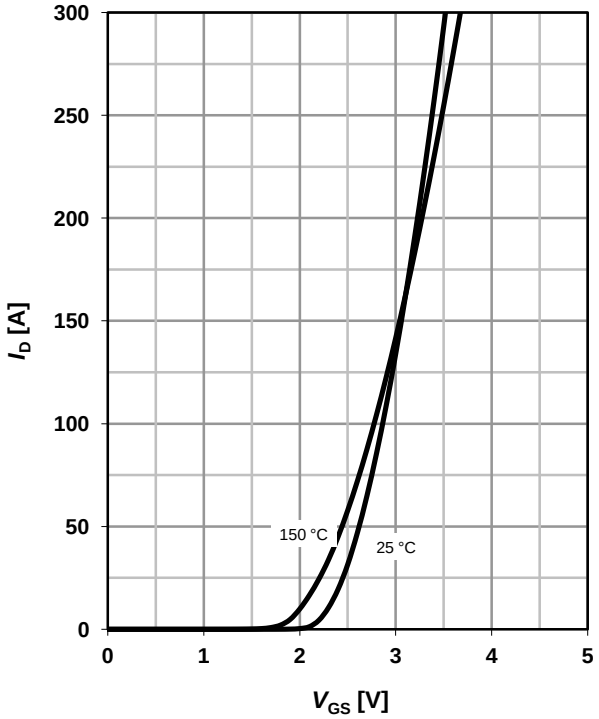
parameter: V_{GS}



7 Typ. transfer characteristics

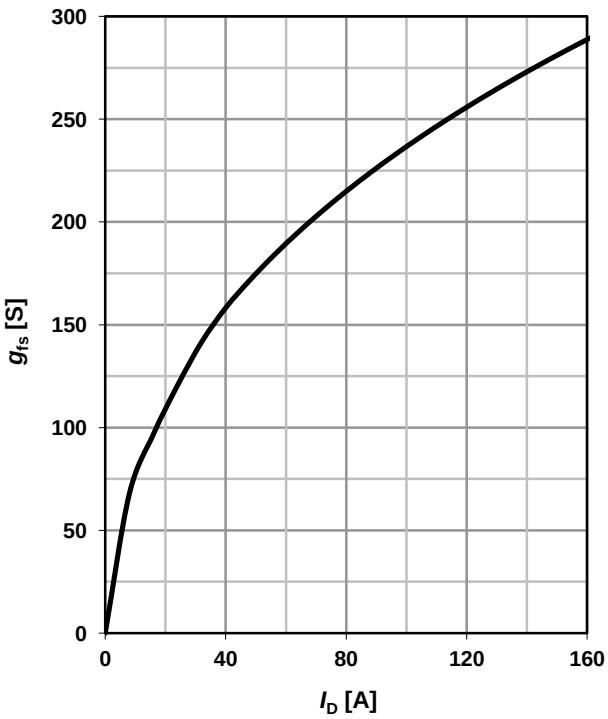
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



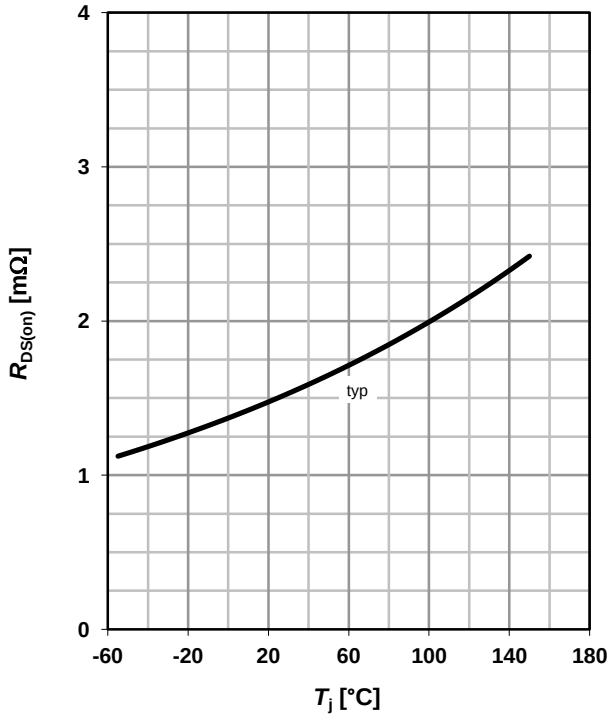
8 Typ. forward transconductance

$g_{fs}=f(I_D)$; $T_j=25$ °C



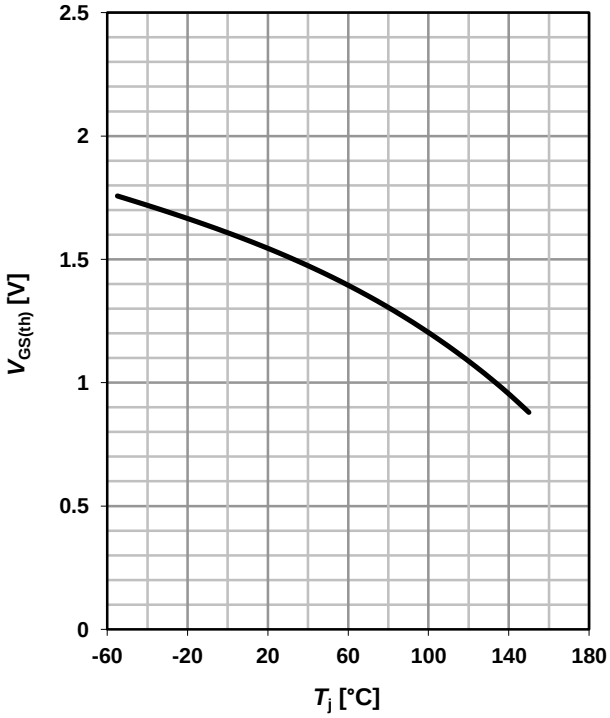
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=30 A; V_{GS}=10 V



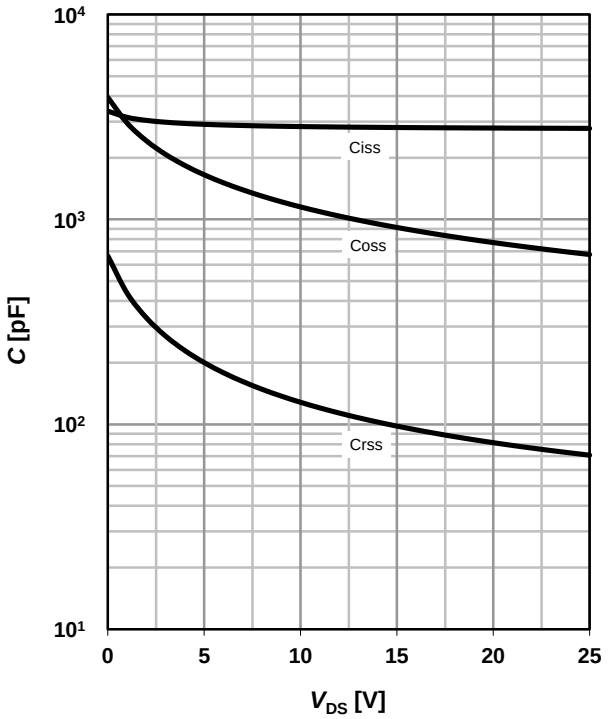
10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=250 µA



11 Typ. capacitances

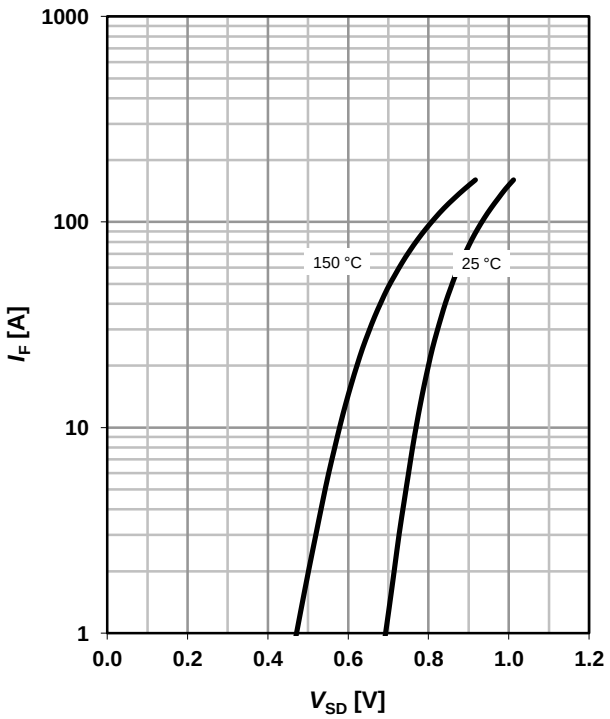
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

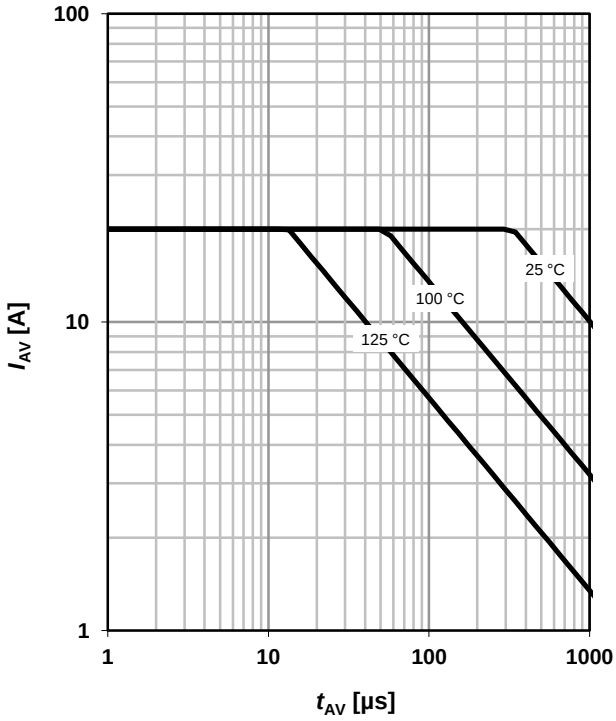
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

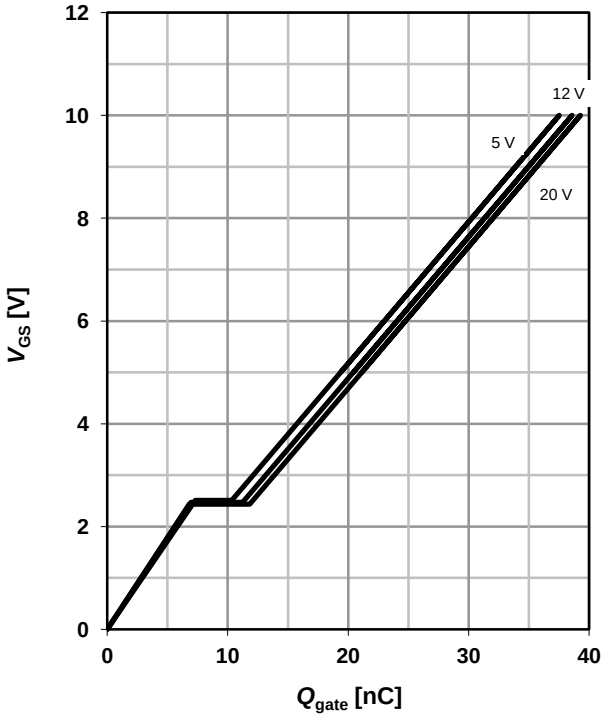
parameter: $T_{j(start)}$



14 Typ. gate charge

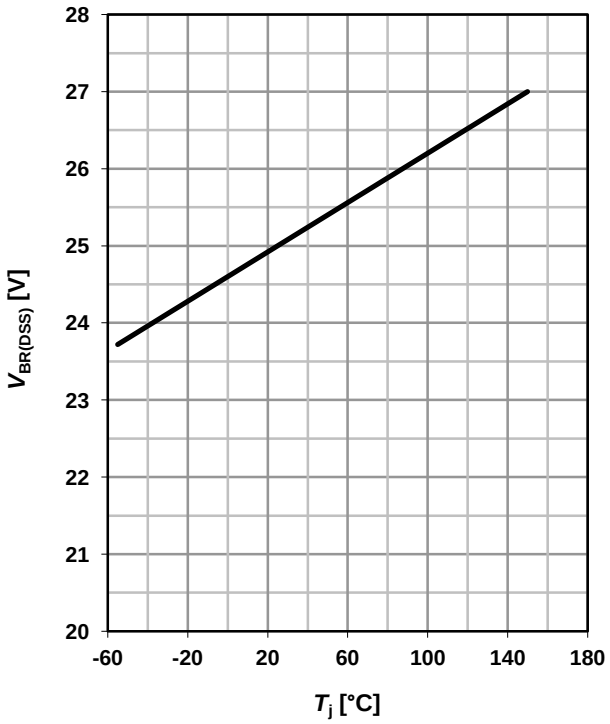
V_{GS}=f(Q_{gate}); I_D=30 A pulsed

parameter: V_{DD}

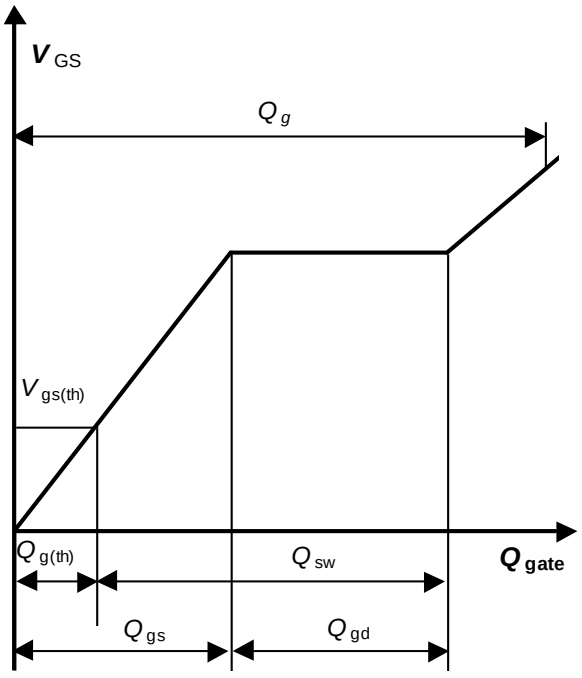


15 Drain-source breakdown voltage

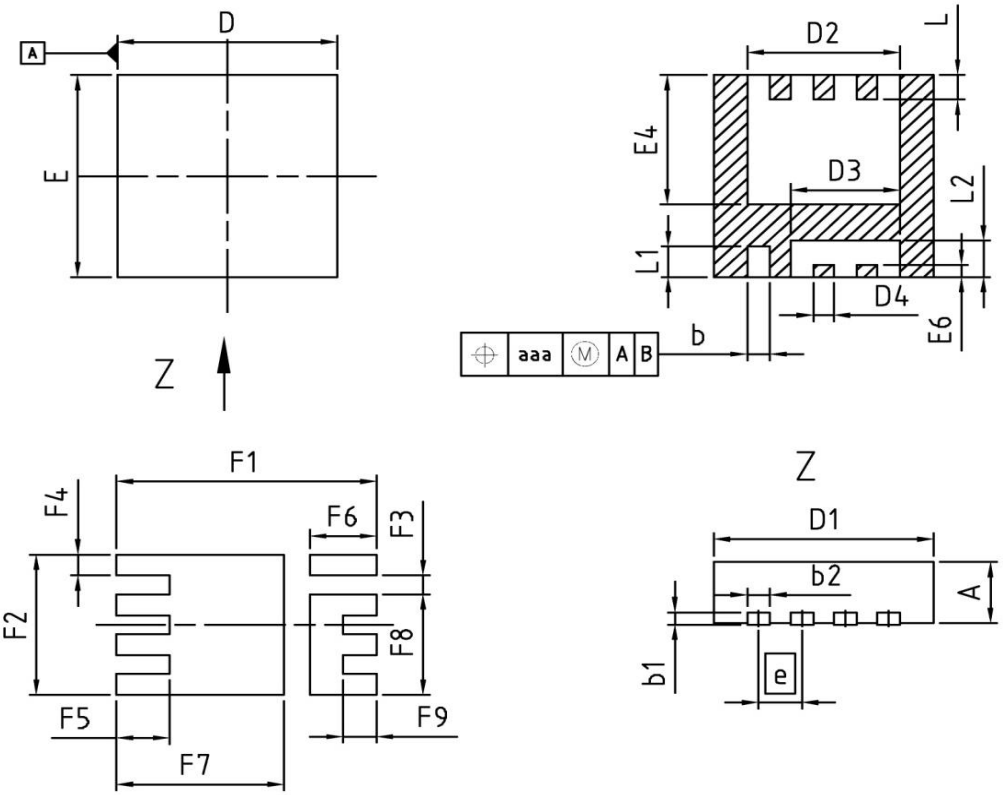
$V_{BR(DSS)}$=f(T_j); I_D=1 mA



16 Gate charge waveforms



Package Outline **PG-TSDSON-8 (fused leads)**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.24	0.44	0.009	0.017
b1	0.10	0.30	0.004	0.012
b2	0.24	0.44	0.009	0.017
D=D1	3.20	3.40	0.126	0.134
D2	2.19	2.39	0.086	0.094
D3	1.54	1.74	0.061	0.069
D4	0.21	0.41	0.008	0.016
E	3.20	3.40	0.126	0.134
E4	2.01	2.21	0.079	0.087
E6	0.10	0.30	0.004	0.012
e	0.65 (BSC)		0.026 (BSC)	
N	8		8	
L	0.30	0.51	0.012	0.020
L1	0.40	0.70	0.016	0.028
L2	0.50	0.70	0.020	0.028
aaa	0.25		0.010	
F1	3.90		0.154	
F2	2.29		0.090	
F3	0.31		0.012	
F4	0.34		0.013	
F5	0.80		0.031	
F6	1.00		0.039	
F7	2.51		0.099	
F8	1.64		0.065	
F9	0.50		0.020	

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