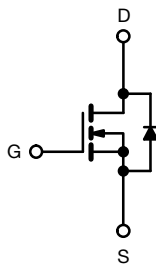
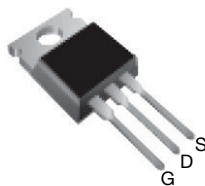


E Series Power MOSFET

TO-220AB


N-Channel MOSFET

FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Computing
 - PC silver box / ATX power supplies
- Lighting
 - Two stage LED lighting
- Consumer electronics
- Applications using hard switched topologies
 - Power factor correction (PFC)
 - Two switch forward converter
 - Flyback converter
- Switch mode power supplies (SMPS)

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	550	
$R_{DS(on)}$ max. at 25 °C (Ω)	$V_{GS} = 10$ V	0.380
Q_g max. (nC)	50	
Q_{gs} (nC)	6	
Q_{gd} (nC)	10	
Configuration	Single	

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free and halogen-free	SiHP12N50E-BE3 ^a
	SiHP12N50E-GE3

Note

a. "-BE3" denotes alternate manufacturing location

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	500	V
Gate-source voltage	V_{GS}	± 30	
Continuous drain current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed drain current ^a	I_{DM}	21	
Linear derating factor		0.91	W/°C
Single pulse avalanche energy ^b	E_{AS}	103	mJ
Maximum power dissipation	P_D	114	W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Drain-source voltage slope	dV/dt	70	V/ns
Reverse diode dV/dt ^d		27	
Soldering recommendations (peak temperature) ^c	For 10 s	300	°C

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature
 b. $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 2.7$ A
 c. 1.6 mm from case
 d. $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C

**THERMAL RESISTANCE RATINGS**

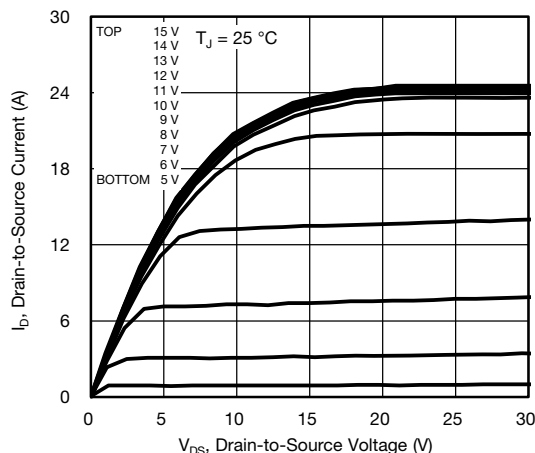
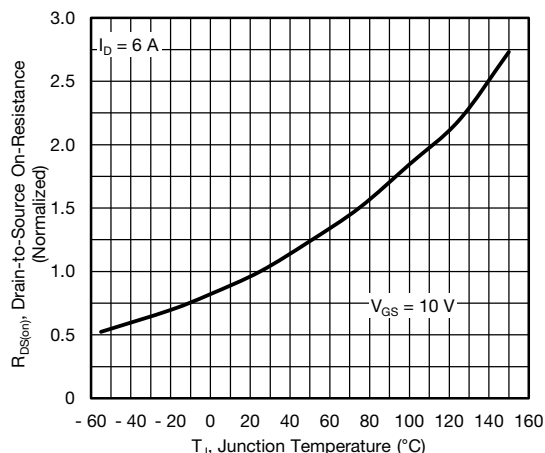
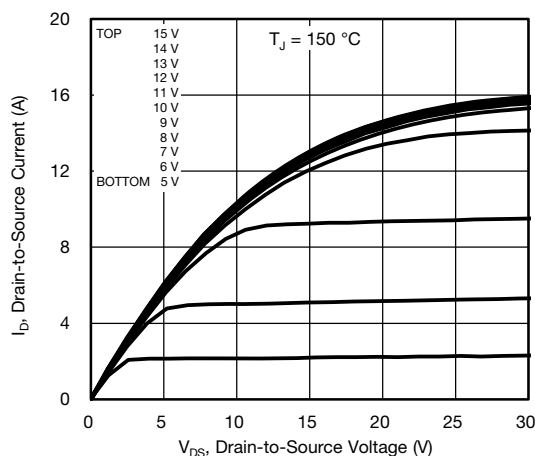
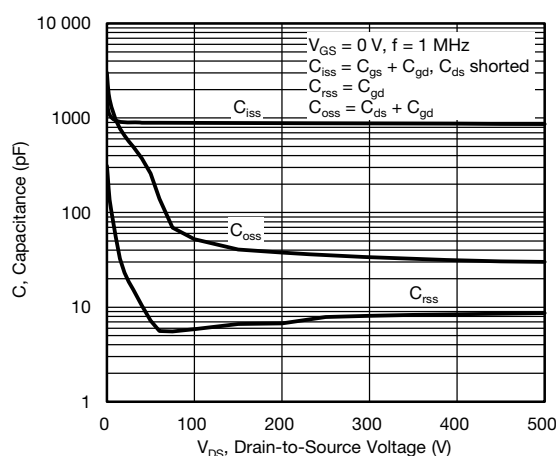
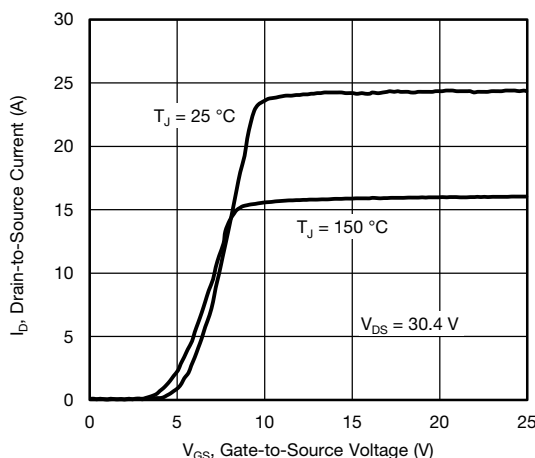
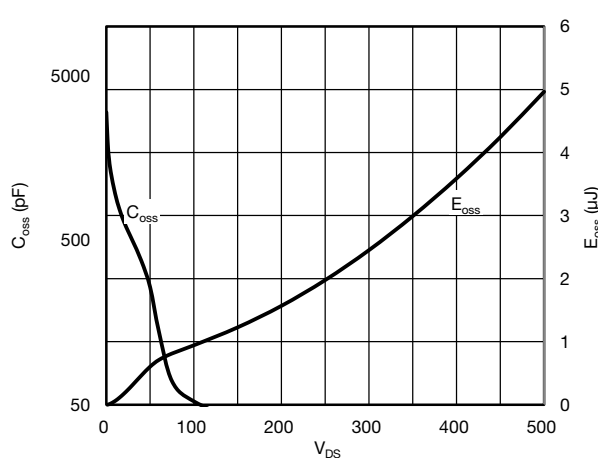
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	1.1	

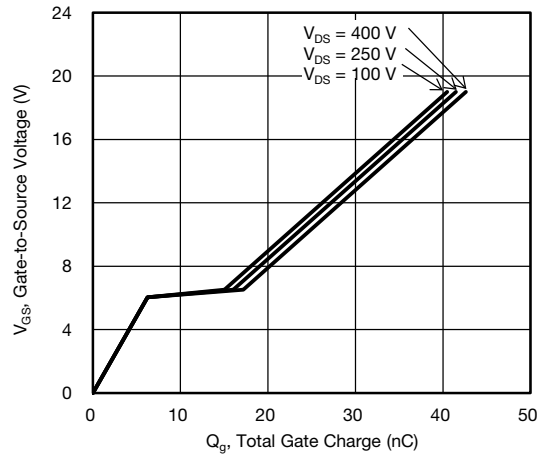
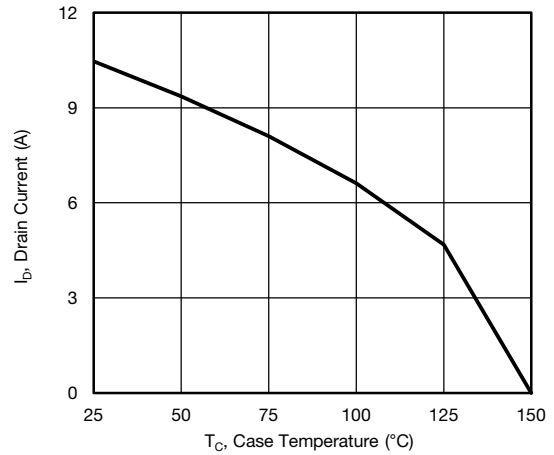
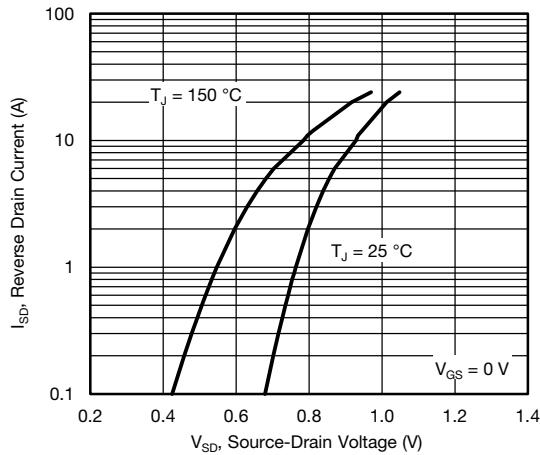
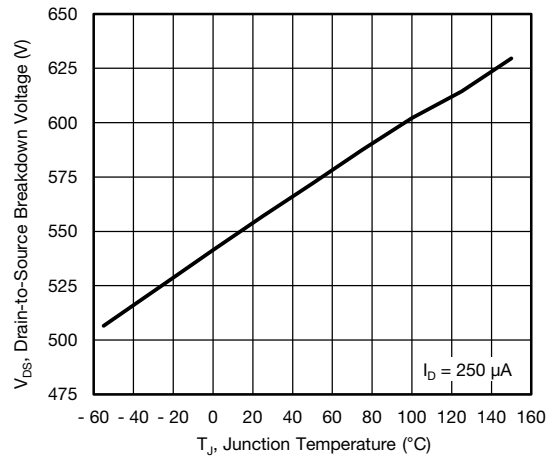
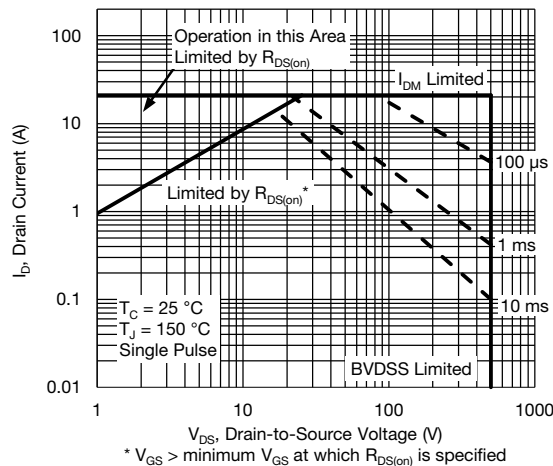
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

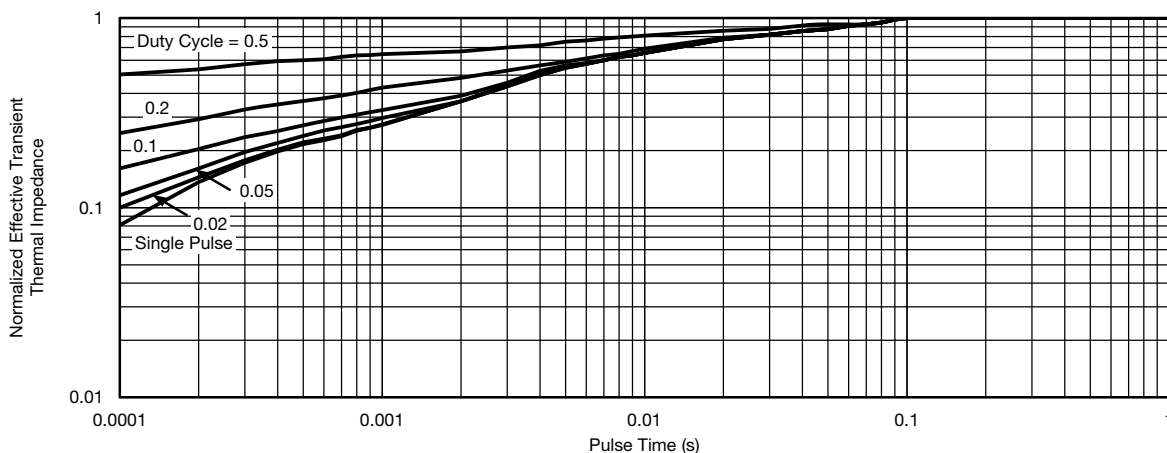
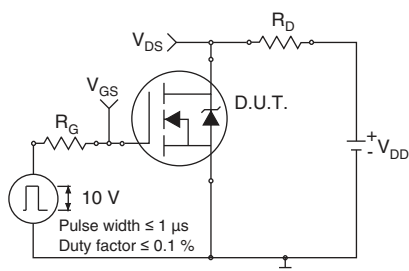
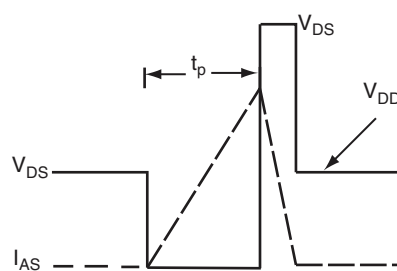
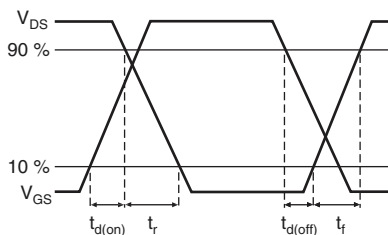
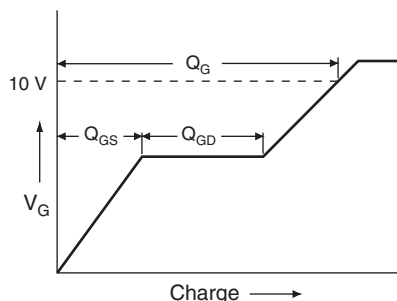
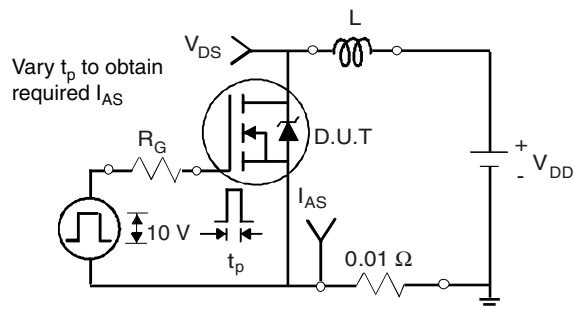
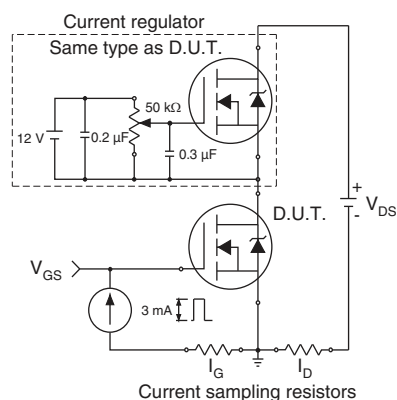
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		500	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.60	-	V/°C
Gate-source threshold Voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
		V _{GS} = ± 30 V		-	-	± 1	μA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V		-	-	1	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C		-	-	10	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 6 A	-	0.330	0.380	Ω
Forward transconductance	g _{fs}	V _{DS} = 30 V, I _D = 6 A		-	3.1	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz		-	886	-	pF
Output capacitance	C _{oss}			-	52	-	
Reverse transfer capacitance	C _{rss}			-	6	-	
Effective output capacitance, energy related ^a	C _{o(er)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		-	45	-	
Effective output capacitance, time related ^b	C _{o(tr)}			-	131	-	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 6 A, V _{DS} = 400 V	-	25	50	nC
Gate-source charge	Q _{gs}			-	6	-	
Gate-drain charge	Q _{gd}			-	10	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 400 V, I _D = 6 A, V _{GS} = 10 V, R _g = 9.1 Ω		-	13	26	ns
Rise time	t _r			-	16	32	
Turn-off delay time	t _{d(off)}			-	29	58	
Fall time	t _f			-	12	24	
Gate input resistance	R _g	f = 1 MHz, open drain		-	0.92	-	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	10.5	A
Pulsed diode forward current	I _{SM}			-	-	21	
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 7.5 A, V _{GS} = 0 V		-	-	1.2	V
Reverse recovery time	t _{rr}	T _J = 25 °C, I _F = I _S = 6 A, dI/dt = 100 A/μs, V _R = 25 V		-	244	-	ns
Reverse recovery charge	Q _{rr}			-	2.5	-	μC
Reverse recovery current	I _{RRM}			-	19	-	A

Notes

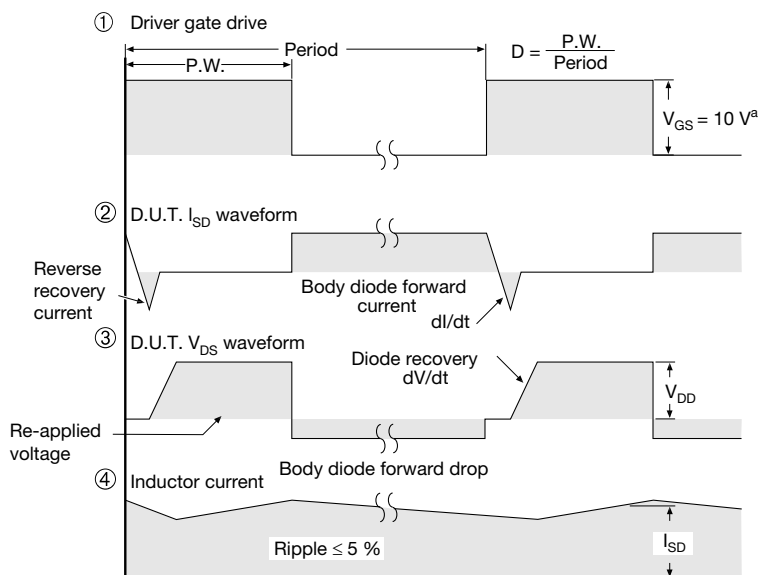
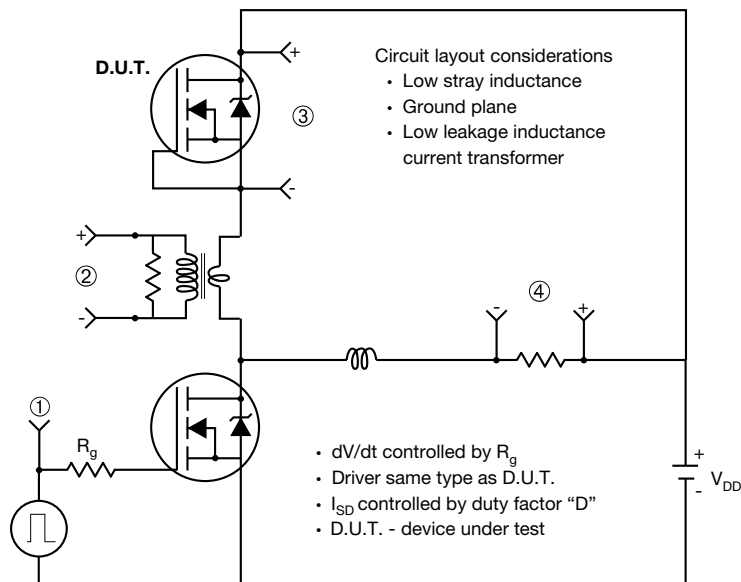
- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - C_{OSS} and E_{OSS} vs. V_{DS}


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 10 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Typical Source-Drain Diode Forward Voltage

Fig. 11 - Temperature vs. Drain-to-Source Voltage

Fig. 9 - Maximum Safe Operating Area


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

Fig. 13 - Switching Time Test Circuit

Fig. 16 - Unclamped Inductive Waveforms

Fig. 14 - Switching Time Waveforms

Fig. 17 - Basic Gate Charge Waveform

Fig. 15 - Unclamped Inductive Test Circuit

Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 \text{ V}$ for logic level devices

Fig. 19 - For N-Channel

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