

IRF7341QPbF

HEXFET® Power MOSFET

Typical Applications

- Anti-lock Braking Systems (ABS)
- Electronic Fuel Injection
- Air bag

Benefits

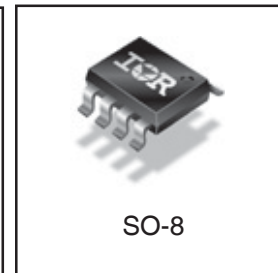
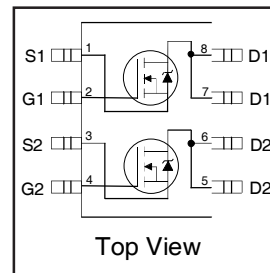
- Advanced Process Technology
- Dual N-Channel MOSFET
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Repetitive Avalanche Allowed up to T_{jmax}
- Automotive [Q101] Qualified
- Lead-Free

Description

Specifically designed for Automotive applications, these HEXFET® Power MOSFET's in a Dual SO-8 package utilize the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of these Automotive qualified HEXFET Power MOSFET's are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

The 175°C rating for the SO-8 package provides improved thermal performance with increased safe operating area and dual MOSFET die capability make it ideal in a variety of power applications. This dual, surface mount SO-8 can dramatically reduce board space and is also available in Tape & Reel.

V_{DS}	$R_{DS(on)}$ max	I_D
55V	0.050 @ $V_{GS} = 10V$	5.1A
	0.065 @ $V_{GS} = 4.5V$	4.42A



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-Source Voltage	55	V
I_D @ $T_A = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	5.1	A
I_D @ $T_A = 70^\circ C$	Continuous Drain Current, V_{GS} @ 10V	4.2	
I_{DM}	Pulsed Drain Current ^①	42	
P_D @ $T_A = 25^\circ C$	Maximum Power Dissipation ^③	2.4	W
P_D @ $T_A = 70^\circ C$	Maximum Power Dissipation ^③	1.7	W
	Linear Derating Factor	16	mW/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ^②	140	mJ
I_{AR}	Avalanche Current ^①	5.1	A
E_{AR}	Repetitive Avalanche Energy	See Fig. 14, 15, 16	mJ
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 175	°C

Thermal Resistance

	Parameter	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ^③	62.5	°C/W

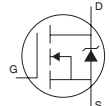
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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0V$, $I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.052	—	$V/^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.043	0.050	Ω	$V_{GS} = 10V$, $I_D = 5.1A$ ②
		—	0.056	0.065		$V_{GS} = 4.5V$, $I_D = 4.42A$ ②
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	—	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
g_{fs}	Forward Transconductance	10.4	—	—	S	$V_{DS} = 10V$, $I_D = 5.2A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	2.0	μA	$V_{DS} = 44V$, $V_{GS} = 0V$
		—	—	25		$V_{DS} = 44V$, $V_{GS} = 0V$, $T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	29	44	nC	$I_D = 5.2A$
Q_{gs}	Gate-to-Source Charge	—	2.9	4.4		$V_{DS} = 44V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	7.3	11		$V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	9.2	—	ns	$V_{DD} = 28V$
t_r	Rise Time	—	7.7	—		$I_D = 1.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	31	—		$R_G = 6.0\Omega$
t_f	Fall Time	—	12.5	—		$V_{GS} = 10V$ ②
C_{iss}	Input Capacitance	—	780	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	190	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	66	—		$f = 1.0\text{MHz}$

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2.4	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	42		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}$, $I_S = 2.6A$, $V_{GS} = 0V$ ②
t_{rr}	Reverse Recovery Time	—	51	77	ns	$T_J = 25^\circ\text{C}$, $I_F = 2.6A$
Q_{rr}	Reverse Recovery Charge	—	76	114	nC	$di/dt = 100A/\mu s$ ②

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

③ Surface mounted on FR-4 board, $t \leq 10\text{sec}$.

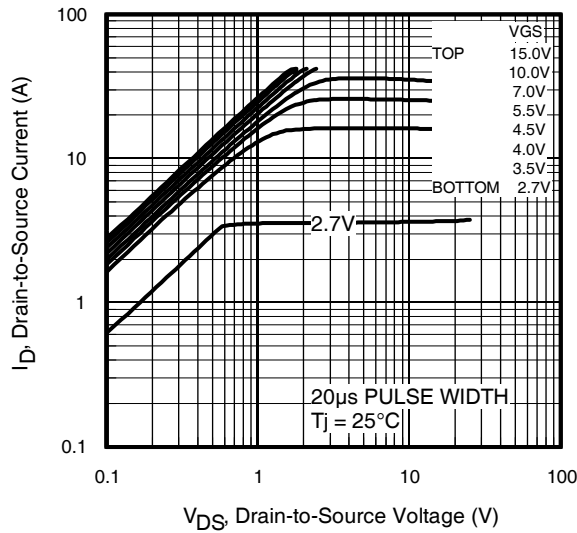


Fig 1. Typical Output Characteristics

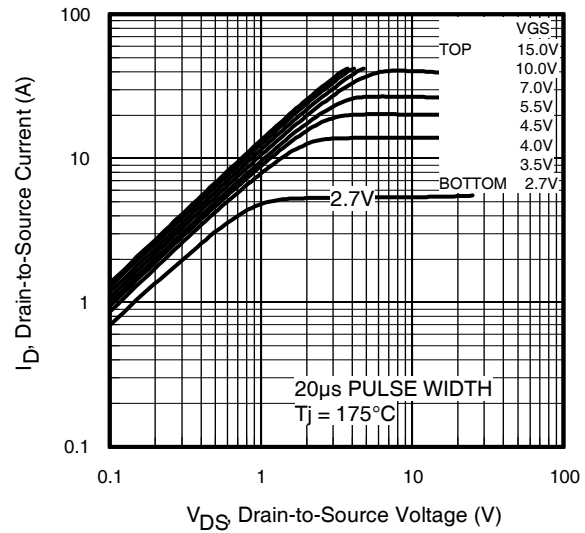


Fig 2. Typical Output Characteristics

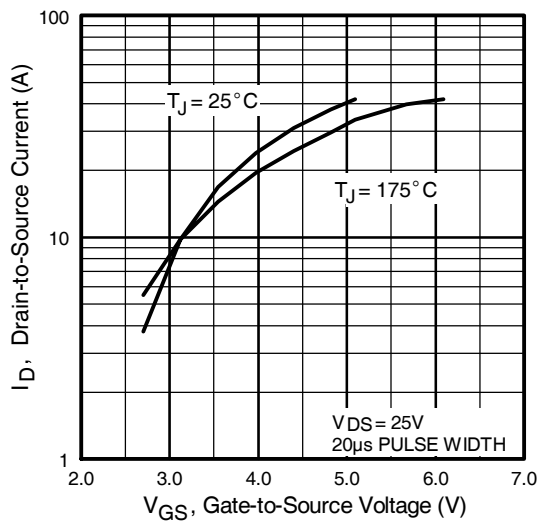


Fig 3. Typical Transfer Characteristics

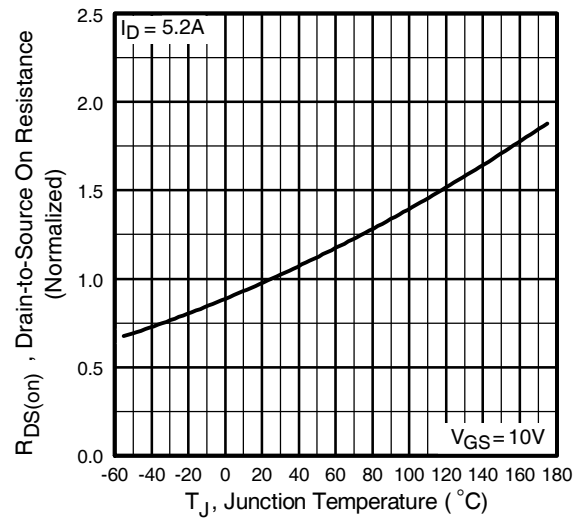
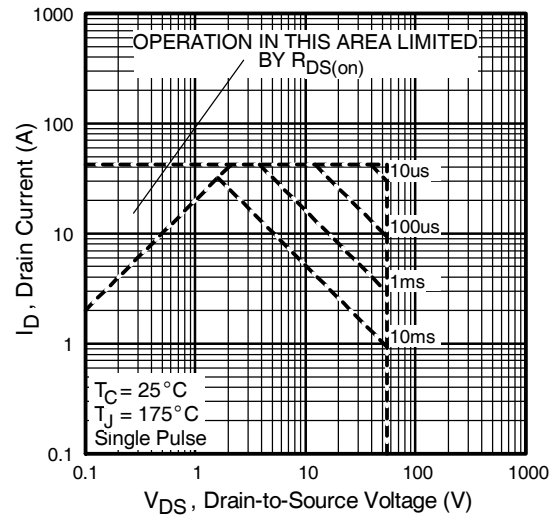
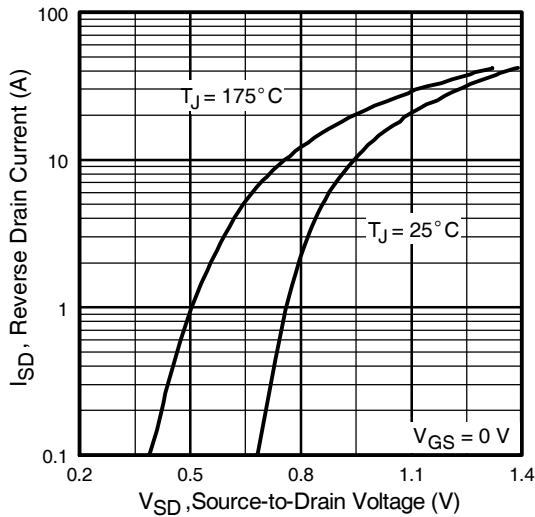
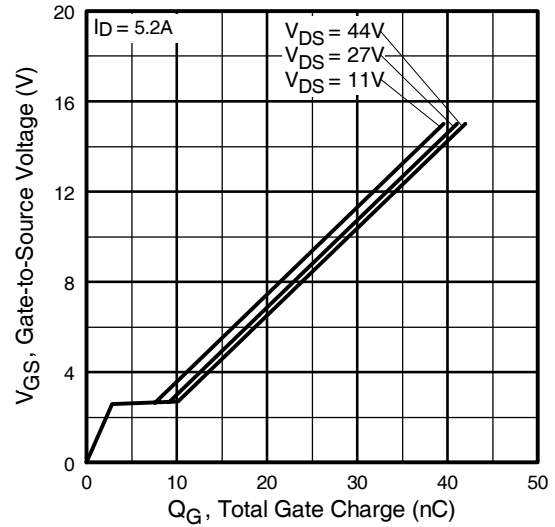
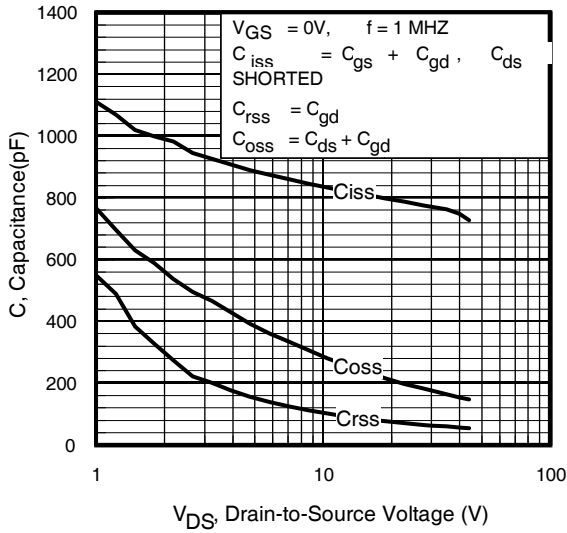


Fig 4. Normalized On-Resistance
Vs. Temperature

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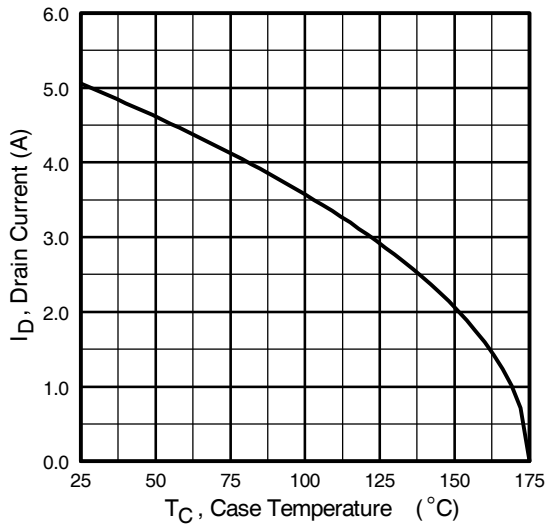


Fig 9. Maximum Drain Current Vs. Case Temperature

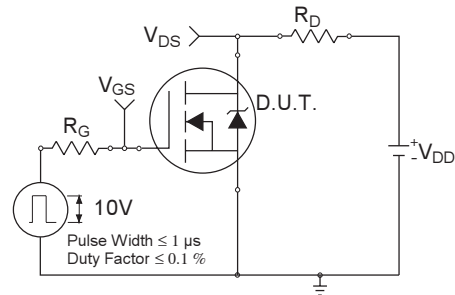


Fig 10a. Switching Time Test Circuit

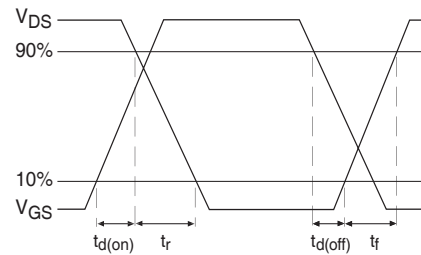


Fig 10b. Switching Time Waveforms

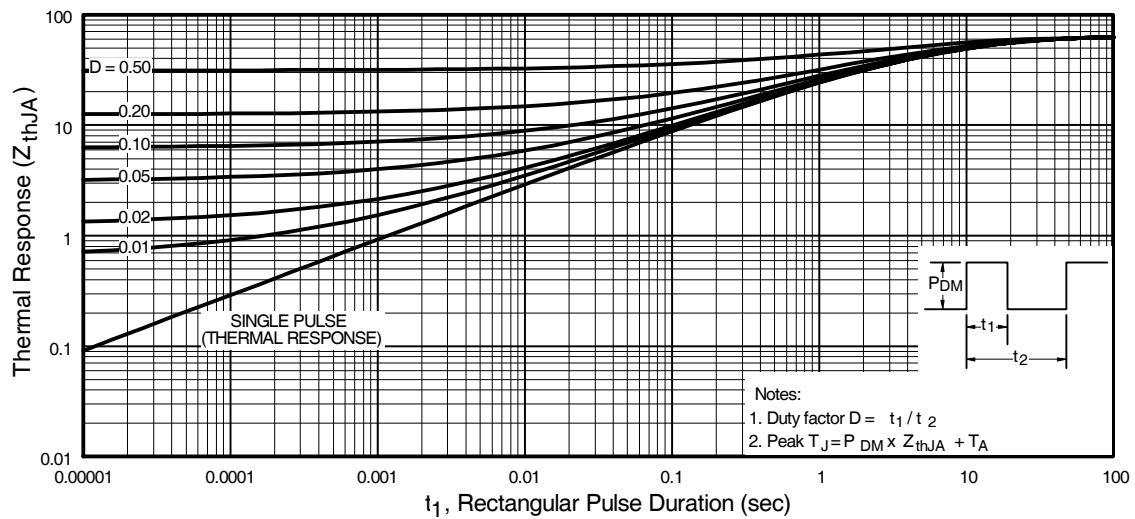


Fig 10. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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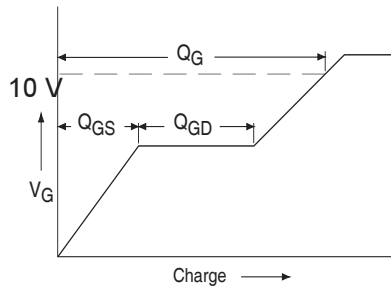
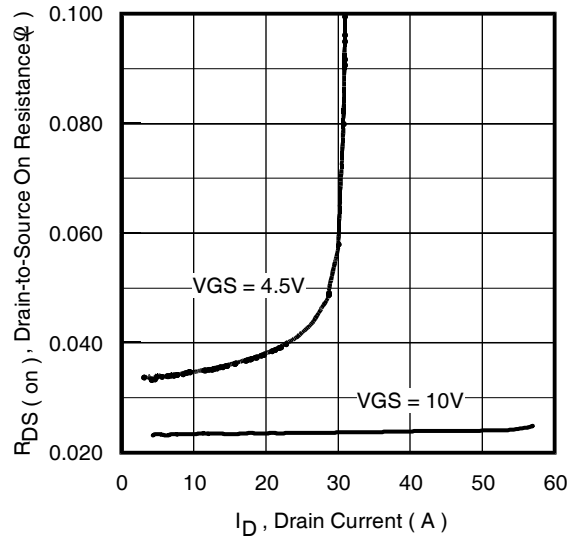
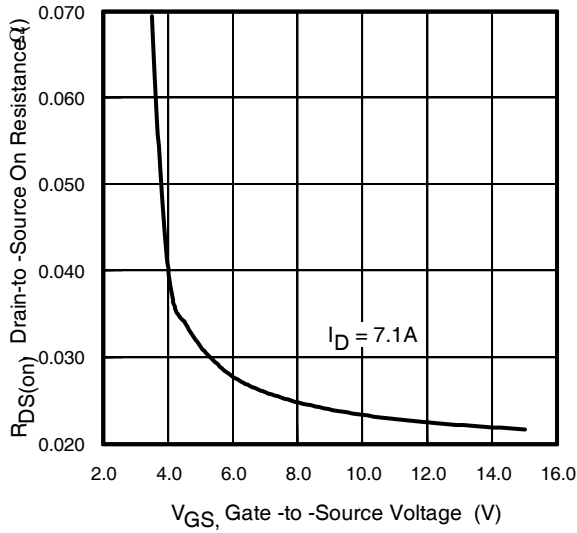


Fig 13a. Basic Gate Charge Waveform

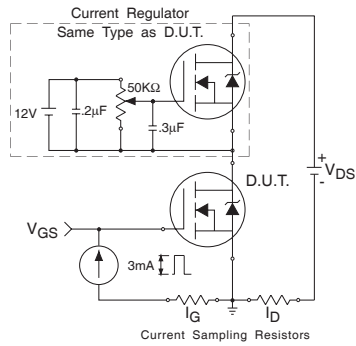


Fig 13b. Gate Charge Test Circuit

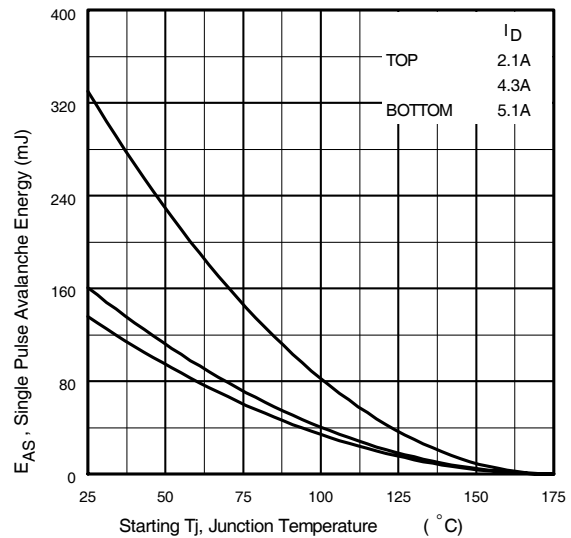


Fig 14. Maximum Avalanche Energy Vs. Drain Current

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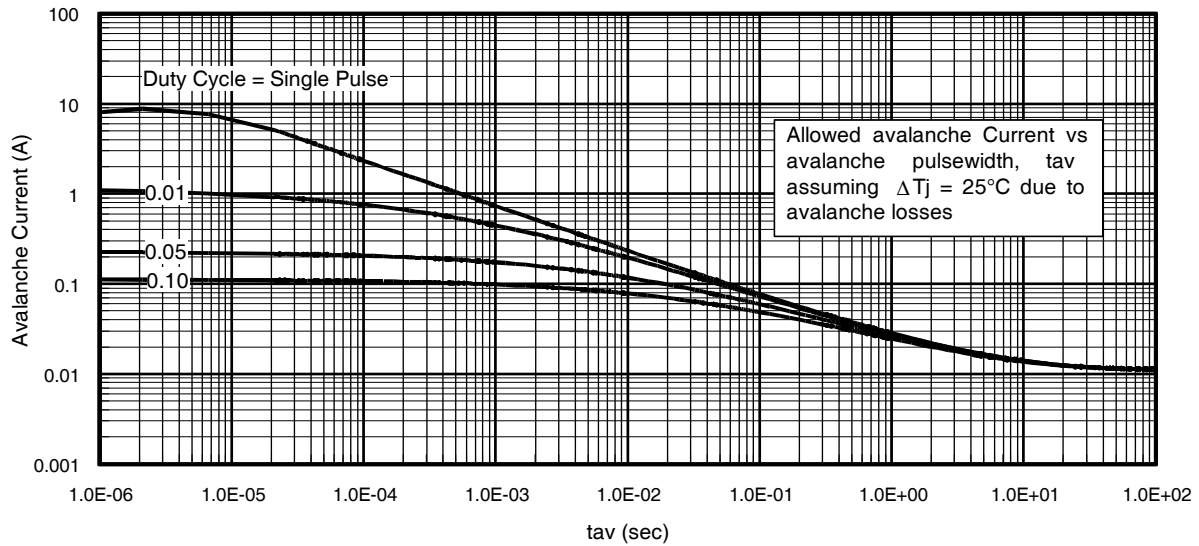


Fig 15. Typical Avalanche Current Vs. Pulsewidth

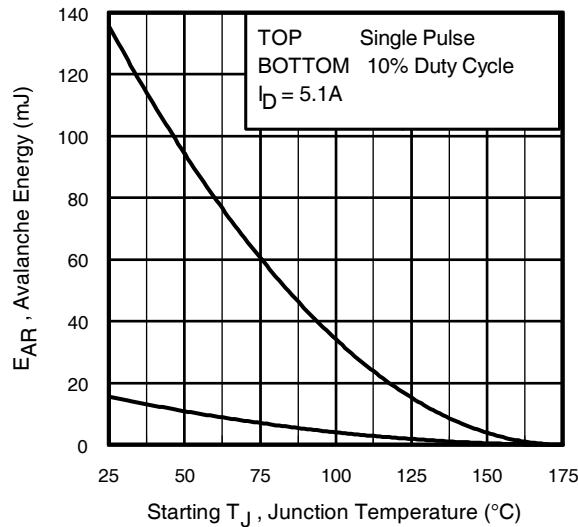


Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

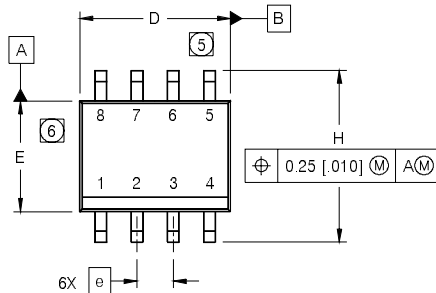
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

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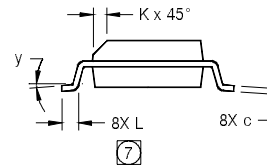
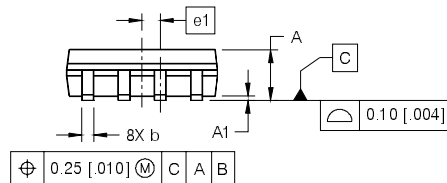
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SO-8 Package Outline

Dimensions are shown in millimeters (inches)



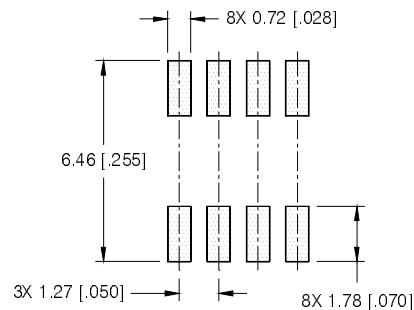
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



NOTES:

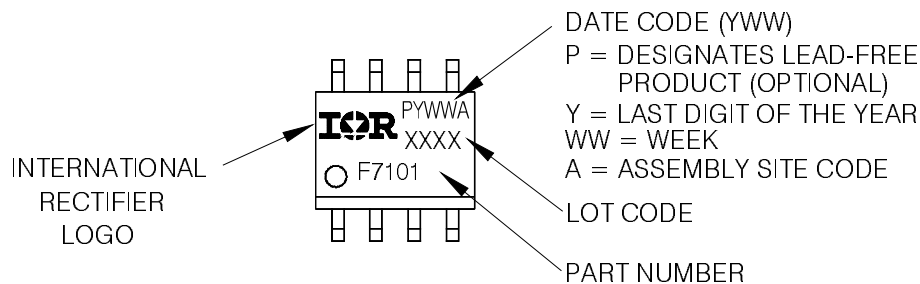
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- ⑤ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [0.006].
- ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [0.010].
- ⑦ DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT



SO-8 Part Marking

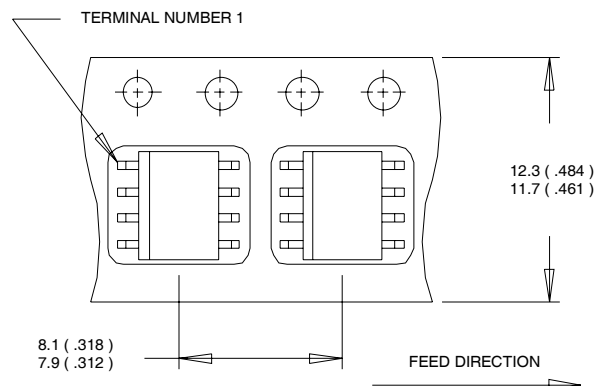
EXAMPLE: THIS IS AN IRF7101 (MOSFET)



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

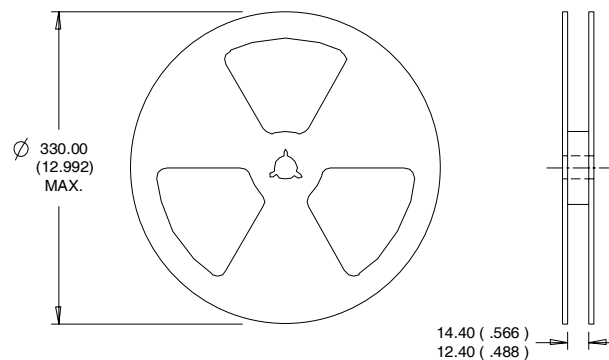
SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.

This product has been designed and qualified for the Automotive [Q101] market.

Qualification Standards can be found on IR's Web site.