

swissbit®

Product data sheet

Industrial CFast™ Card

F-240 Series

SATA II, UDMA6, TRIM, low power

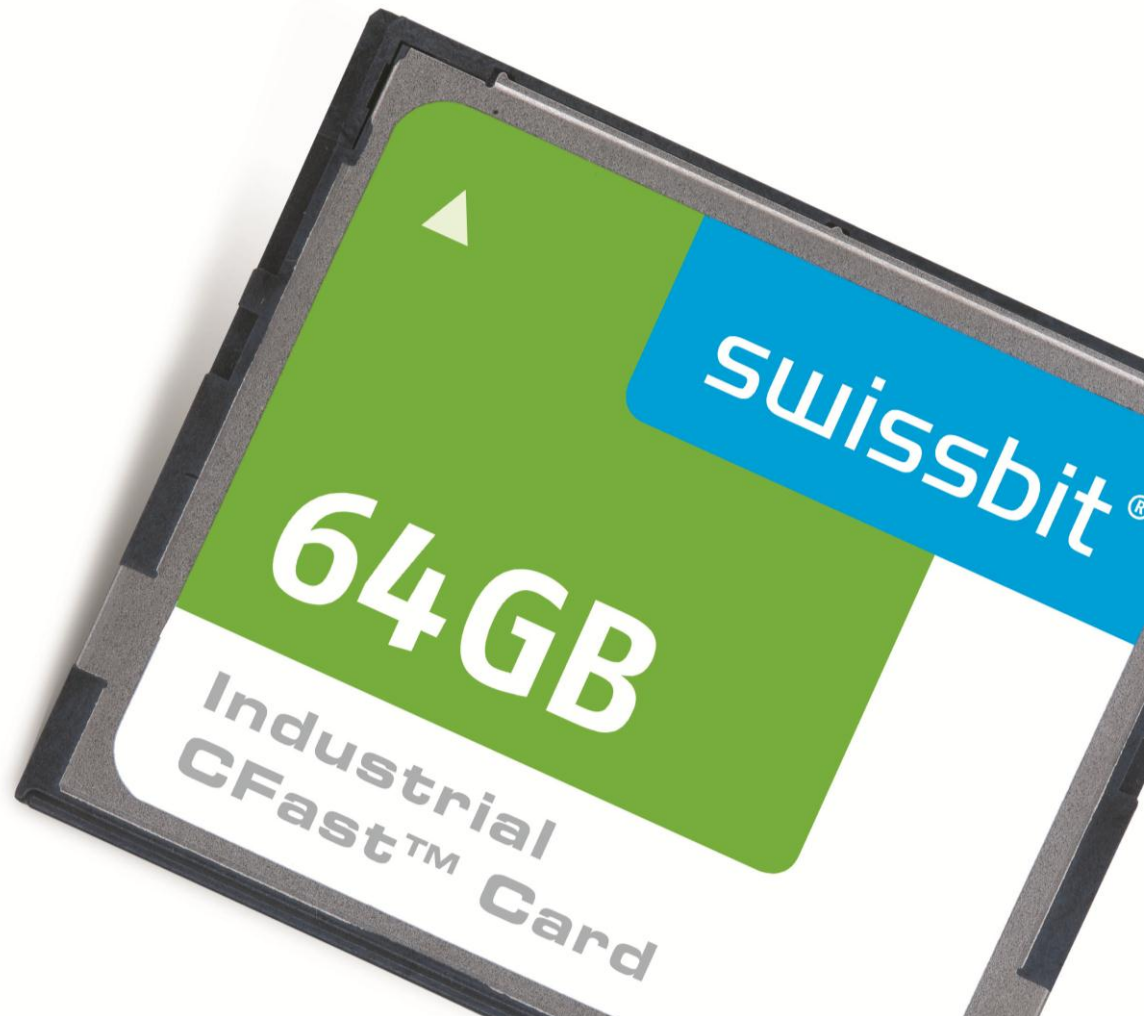
Standard and industrial
temperature grade

BU: Swissbit Group

Date: July 04, 2013

Revision: 1.21

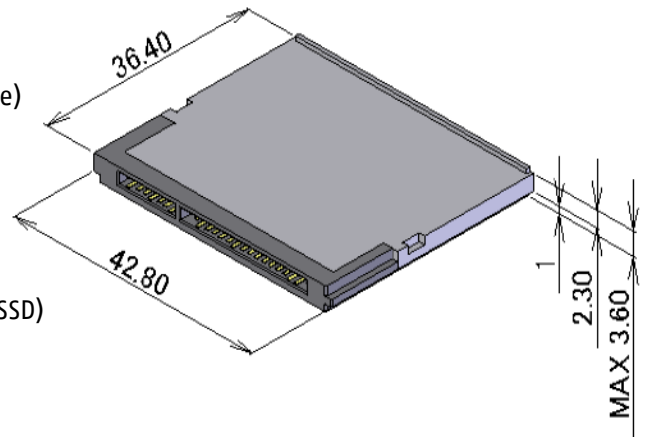
F-240_data_sheet_CA-HxBV_Rev121.doc



F-240 SERIES – INDUSTRIAL CFAST™ CARD WITH SATA INTERFACE

1 Features

- Highly-integrated memory controller
 - SATA Rev 2.6 – 3Gbit/s (1.5Gbit/s compatible)
 - max. UDMA6 MDMA2, PIO4, supported
 - Hardware BCH-code ECC (24bit correction per double sector or 6bit per sector)
 - Fix drive configuration
- Small form factor:
 - CompactFlash card sized Solid State Drive (SSD) with SATA interface
 - 42.8mm x 36.4mm x 3.3mm (max. 3.6mm)
- 7+17 pin (SATA+power) CFast connector
- 3.3V ± 5% power supply
- Very low Power, typical 250mA in transfer operation (CFAST Power level 0)
- CFast PHYSLP supported (<20 mA)
- Activity and SATAlink LED output at LED1 and LED2 pin
- write protect at connector IO1 pin
- Special features
 - S.M.A.R.T. support with additional vendor information, interpretation with Swissbit life time monitoring tool
 - TRIM command
 - NCQ queue depth 32
 - HPA (Host protected area)
 - Security mode feature set
 - LBA48 command set
 - host initiated power management requests
 - write protection with vendor command
- Wear Leveling: active wear leveling of static and dynamic data
The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. With that the maximum write endurance of the device is guaranteed.
- Read disturb management (refresh data when flash often read)
- High reliability
 - Best available SLC NAND Flash technology
 - Designed for embedded market
 - MTBF > 2,500,000 hours
 - Data reliability: < 1 non-recoverable error per 10¹⁴ bits read
 - Number of connector insertions/removals: >10,000
- High performance
 - Up to 300MB/s burst transfer rate in SATA II – 3.0Gb/sec
 - Sustained Write performance: up to 120MB/s (4channel)
 - Sustained Read Performance: up to 120MB/s (4channel)
- Available densities
 - 2GByte up to 64GByte (SLC NAND Flash)
- 2 Temperature ranges
 - Commercial Temperature range 0 ... +70°C
 - Industrial Temperature range -40 ... +85°C
- Life Cycle Management
- Controlled BOM
- RoHS compatible



2 Table of Content

| | |
|--|-----------|
| 1 FEATURES | 2 |
| 2 TABLE OF CONTENT | 3 |
| 3 ORDER INFORMATION | 5 |
| 3.1 AVAILABLE STANDARD PART NUMBERS | 5 |
| 3.2 OFFERED OEM OPTIONS | 5 |
| 4 PRODUCT SPECIFICATION | 6 |
| 4.1 PHYSICAL DESCRIPTION | 6 |
| 4.2 SYSTEM PERFORMANCE | 7 |
| 4.3 ENVIRONMENTAL SPECIFICATIONS | 8 |
| 4.4 PHYSICAL DIMENSIONS | 8 |
| 4.5 RELIABILITY | 8 |
| 4.6 DRIVE GEOMETRY / CHS PARAMETER | 8 |
| 5 ELECTRICAL INTERFACE | 9 |
| 5.1 ELECTRICAL DESCRIPTION | 9 |
| 5.2 ELECTRICAL SPECIFICATION | 10 |
| 5.3 LED AND IO-PINS..... | 10 |
| 5.4 CARD DETECTION AND PHYSLP FUNCTIONS WITH CDI AND CDO PIN | 11 |
| 5.5 POWER MANAGEMENT..... | 13 |
| 6 ATA COMMAND DESCRIPTION | 14 |
| 6.1 CHECK POWER MODE (98H OR E5H) | 16 |
| 6.2 DATA SET MANAGEMENT (06H) TRIM | 16 |
| 6.3 EXECUTE DRIVE DIAGNOSTIC (90H)..... | 16 |
| 6.4 FLUSH CACHE (E7H)..... | 17 |
| 6.5 FLUSH CACHE EXT (EAH) 48BIT LBA | 17 |
| 6.6 FORMAT TRACK (50H)..... | 17 |
| 6.7 IDENTIFY DEVICE (ECH)..... | 18 |
| 6.8 IDLE (97H OR E3H)..... | 26 |
| 6.9 IDLE IMMEDIATE (95H OR E1H) | 26 |
| 6.10 MEDIA LOCK/MEDIA UNLOCK (DEH/DFH) | 26 |
| 6.11 NOP (00H)..... | 26 |
| 6.12 READ BUFFER (E4H) | 27 |
| 6.13 READ DMA (C8H)..... | 27 |
| 6.14 READ DMA EXT (25H) 48BIT LBA | 27 |
| 6.15 READ FPDMA QUEUED (60H) (IF NCQ FEATURE SET SUPPORTED) | 28 |
| 6.16 READ MULTIPLE (C4H) | 28 |
| 6.17 READ MULTIPLE EXT (29H) 48BIT LBA..... | 29 |
| 6.18 READ NATIVE MAX ADDRESS (F8H) | 30 |
| 6.19 READ NATIVE MAX ADDRESS EXT (27H) | 30 |
| 6.20 READ SECTOR(S) (20H) | 31 |
| 6.21 READ SECTORS EXT (24H) 48BIT LBA..... | 31 |
| 6.22 READ VERIFY SECTOR(S) (40H OR 41H) | 31 |
| 6.23 READ VERIFY EXT (42H) 48BIT LBA | 32 |
| 6.24 RECALIBRATE (1XH)..... | 32 |
| 6.25 SECURITY DISABLE PASSWORD (F6H) | 32 |
| 6.26 SECURITY ERASE PREPARE (F3H)..... | 33 |
| 6.27 SECURITY ERASE UNIT (F4H)..... | 33 |
| 6.28 SECURITY FREEZE LOCK (F5H)..... | 33 |
| 6.29 SECURITY SET PASSWORD (F1H)..... | 34 |
| 6.30 SECURITY UNLOCK (F2H)..... | 34 |
| 6.31 SEEK (7XH)..... | 35 |
| 6.32 SET FEATURES (EFH) | 35 |
| 6.33 SET MAX ADDRESS (F9H) | 37 |
| 6.34 SET MAX ADDRESS EXT (37H) 48BIT LBA..... | 38 |
| 6.35 SET MULTIPLE MODE (C6H) | 38 |

| | |
|--|-----------|
| 6.36 SET SLEEP MODE (E6H OR 99H) | 39 |
| 6.37 S.M.A.R.T. (BOH) | 39 |
| 6.38 STANDBY (96H OR E2) | 39 |
| 6.39 STANDBY IMMEDIATE (94H OR E0H) | 40 |
| 6.40 TRANSLATE SECTOR (87H) | 40 |
| 6.41 WRITE BUFFER (E8H) | 40 |
| 6.42 WRITE DMA (CAH, CBH) | 40 |
| 6.43 WRITE DMA EXT (35H) 48BIT LBA | 41 |
| 6.44 WRITE FPDMA QUEUED (61H) (IF NCQ FEATURE SET SUPPORTED) | 41 |
| 6.45 WRITE MULTIPLE COMMAND (C5H) | 42 |
| 6.46 WRITE MULTIPLE EXT (39H) 48BIT LBA | 42 |
| 6.47 WRITE SECTOR(S) (30H) | 43 |
| 6.48 WRITE SECTOR(S) EXT (34H) 48BIT LBA | 43 |
| 6.49 WRITE VERIFY (3CH) | 44 |
| 7 S.M.A.R.T FUNCTIONALITY | 45 |
| 7.1 S.M.A.R.T. ENABLE / DISABLE OPERATIONS | 45 |
| 7.2 S.M.A.R.T. ENABLE / DISABLE ATTRIBUTE AUTOSAVE | 45 |
| 7.3 S.M.A.R.T. READ DATA | 45 |
| 7.4 S.M.A.R.T. READ ATTRIBUTE THRESHOLDS | 50 |
| 7.5 S.M.A.R.T. RETURN STATUS | 51 |
| 8 PACKAGE MECHANICAL | 52 |
| 9 DECLARATION OF CONFORMITY | 54 |
| 10 ROHS AND WEEE UPDATE FROM SWISSBIT | 55 |
| 11 PART NUMBER DECODER | 57 |
| 11.1 MANUFACTURER | 57 |
| 11.2 MEMORY TYPE | 57 |
| 11.3 PRODUCT TYPE | 57 |
| 11.4 DENSITY | 57 |
| 11.5 PLATFORM | 57 |
| 11.6 PRODUCT GENERATION | 57 |
| 11.7 MEMORY ORGANIZATION | 57 |
| 11.8 TECHNOLOGY | 57 |
| 11.9 NUMBER OF FLASH CHIP | 57 |
| 11.10 FLASH CODE | 57 |
| 11.11 TEMP. OPTION | 58 |
| 11.12 DIE CLASSIFICATION | 58 |
| 11.13 PIN MODE | 58 |
| 11.14 DRIVE CONFIGURATION XYZ | 58 |
| 11.15 OPTION | 58 |
| 12 SWISSBIT CFAST MARKING SPECIFICATION | 59 |
| 12.1 TOP VIEW | 59 |
| 12.2 BOTTOM VIEW | 59 |
| REVISION HISTORY | 60 |

3 Order Information

3.1 Available Standard part numbers

FIX / SATA III/ UDMA6, MDMA2, PIO4

| Density | Part Number |
|--------------------------------|------------------------------|
| F-240 Series CFast Card | |
| 2GB | SFCA2048HgBV4TO-t-MS-2y6-STD |
| 4GB | SFCA4096HgBV4TO-t-MS-2y6-STD |
| 8GB | SFCA8192HgBV4TO-t-DT-2y6-STD |
| 16GB | SFCA16GBHgBV4TO-t-QT-2y6-STD |
| 32GB | SFCA32GBHgBV4TO-t-QT-2y6-STD |
| 64GB | SFCA64GBHgBV4TO-t-NU-2y6-STD |

Table 1: Standard temperature product list

g= depends on product generation

t= Temperature "C" commercial (0°C – +70°C) "I" industrial (-40°C – +85°C)

y= depends on firmware generation

3.2 Offered OEM options

- Customer specified drive size and drive geometry (C/H/S – cylinder/head/sector)
- Customer specified drive ID (Strings)
- Preload service (also drive images with any file system)
- ...

4 Product Specification

The CFAST™ card is a small form factor non-volatile memory drive which provides high capacity data storage. It has a standard CFAST connector with SATA and power/control part. The card works at a supply voltage of 3.3V. The drive with the SATA interface operates in Mode 2.0 (1.5 or 3.0 Gb/s burst).

With an adapter (e.g. Swissbit CFAST Adapter) the drive behaves as a standard SATA disk drive.

The adapter can be mounted in Swissbit 2.5" SSD housing.

The drive has an internal **intelligent controller** which manages interface protocols, data storage and retrieval as well as hardware BCH-code **Error Correction Code (ECC), defect handling, diagnostics and clock control.**

The **wear leveling** mechanism assures an equal usage of the Flash memory cells to extend the life time.

The hardware BCH-code ECC allows to detect and correct **24 random bits per double sector or 6 random bits per sector (depending on the flash type).**

The drive has a **voltage detector** and a powerful **power-loss management feature** to prevent data corruption after power-down.

The specification has been realized and approved by the ATA/ATAPI-8 specification.

The system highlights are shown in Table 2 ...Table 9.

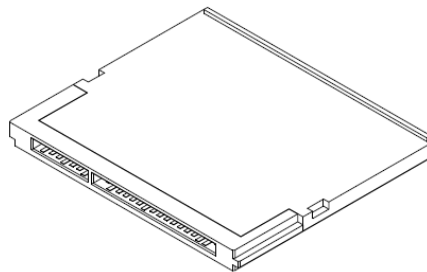
Related Documentation

- CFAST specification 1.1 (www.compactflash.org)
- Serial ATA International Organization: Serial ATA Revision 2.6 (www.serialata.org)
- Serial Transport Protocols and Physical Interconnect (ATA/ATAPI-8 to ATA/ATAPI-5) (www.t13.org)
- Electronic Industries Alliance (www.eia.org)

4.1 Physical description

The CFAST™ card contains a flash controller and Flash memory modules. The controller interfaces with a host system allowing data to be written to and read from the Flash memory modules.

The CFAST™ card is offered in a Compact Flash size package with a standard CFAST connector with a 7-pin SATA connector and a 17-pin power and control connector with 15 pins. Figure 6 and Figure 7 show CFAST™ card dimensions and connector location.



4.2 System Performance

Table 2: System Performance

| System Performance | | Typ. | Max. | Unit |
|---|-----------|------------|------|------|
| Data transfer Rate (SATA burst (1.5 or 3.0Gb/s)) | | 150 or 300 | 300 | MB/s |
| Sustained Sequential Read 128kB Block size ⁽¹⁾ | 2GB | 94 | 100 | MB/s |
| | 4...16GB | 108 | 115 | |
| | 32...64GB | 116 | 120 | |
| Sustained Sequential Write 128kB Block size ⁽¹⁾ | 2GB | 57 | 65 | |
| | 4...16GB | 86 | 95 | |
| | 32...64GB | 111 | 120 | |
| Sustained Sequential Read 4kB Block size ⁽¹⁾ | 2GB | 42 | 50 | MB/s |
| | 4...16GB | 46 | 50 | |
| | 32...64GB | 46 | 50 | |
| Sustained Sequential Write 4kB Block size ⁽¹⁾ | 2GB | 36 | 40 | |
| | 4...16GB | 40 | 45 | |
| | 32...64GB | 40 | 45 | |
| Sustained Random Read 4kB Block size ⁽¹⁾ | 2GB | 13 | 15 | MB/s |
| | 4...16GB | 11.8 | 14 | |
| | 32...64GB | 11.2 | 13 | |
| Sustained Random Write 4kB Block size ^{(1) (2)} | 2GB | 0.31 | 0.37 | |
| | 4...16GB | 0.28 | 0.35 | |
| | 32...64GB | 0.21 | 0.30 | |
| Trimmed Random Write ^{(1) (2)} 4kB Block size | 2GB | 1.3 | 1.5 | MB/s |
| | 4...16GB | 1.0 | 1.2 | |
| | 32...64GB | 0.95 | 1.1 | |

1. All values refer to Toshiba Flash chips in UDMA6 mode (SATA 3.0Gbit/s) with Sequential write/read test (256 sectors multiple commands) and sequential and random write/read test (8 sectors multiple commands) without NCQ. With NCQ transfer the speed is even faster. Sustained Speed depends on flash type and number, file/cluster size, and burst speed.
2. The typical random write speed values are really random access across the whole drive. Random write speed values in file systems are much larger.

4.3 Environmental Specifications

4.3.1 Recommended Operating Conditions

Table 3: Recommended Operating Conditions

| Parameter | Value |
|----------------------------------|---------------|
| Commercial Operating Temperature | 0°C to 70°C |
| Industrial Operating Temperature | -40°C to 85°C |
| Power Supply VCC Voltage | 3.3V ±5% |

Table 4: Current consumption (1)

| Current Consumption (type) | 3.3V | Unit |
|----------------------------|---------|------|
| Read (typ/max) | 170/200 | mA |
| Write (typ/max) | 180/200 | |
| Idle Mode (typ/max) | 85/100 | |
| PHYSLP mode | <20 | |

1. All values are typical at 25° C and nominal supply voltage and refer to 8GByte CFAST card at SATA II interface.

4.3.2 Recommended Storage Conditions

Table 5: Recommended Storage Conditions

| Parameter | Value |
|---------------------|----------------|
| Storage Temperature | -50°C to 100°C |

4.3.3 Shock, Vibration, and Humidity

Table 6: Shock, Vibration, and Humidity

| Parameter | Value |
|---------------------------|---|
| Humidity (non-condensing) | 85% RH 85°C, 1000 hrs (JEDEC JESD22, method A101-B) |
| Vibration | 20G Peak, 10...2000Hz |
| Shock | 1500G, 0.5ms duration, half sine wave |

4.4 Physical Dimensions

Table 7: Physical Dimensions

| Physical Dimensions | Value | Unit |
|---------------------|----------|------|
| Length | 36.4±0.1 | mm |
| Width | 42.8±0.1 | |
| Thickness | 3.6±0.1 | |
| Weight (typ.) | 10 | g |

4.5 Reliability

Table 8: System Reliability and Maintenance (1)

| Parameter | Value |
|---------------------|--|
| MTBF (at 25°C) | > 2,500,000 hours |
| Insertions/Removals | > 10,000 |
| Data Reliability | < 1 Non-Recoverable Error per 10 ¹⁴ bits Read |
| Data Retention | 10 year (JESD47) |

1. Dependent on final system qualification data.

4.6 Drive geometry / CHS parameter

Table 9: CFAST card capacity specification

| Capacity | Default_cylinders | Default_heads | Default_sectors _track | Sectors_drive | Total addressable capacity (Byte) |
|---------------------|-------------------|---------------|---------------------------|---------------|--------------------------------------|
| F-240 Series | | | | | |
| 2GB | 3,866 | 16 | 63 | 3,896,928 | 1,995,227,136 |
| 4GB | 7,732 | 16 | 63 | 7,793,856 | 3,990,454,272 |
| 8GB | 15,498 | 16 | 63 | 15,621,984 | 7,998,455,808 |
| 16GB | 16,383*) | 16 | 63 | 30,788,352 | 15,763,636,224 |
| 32GB | 16,383*) | 16 | 63 | 61,608,960 | 31,543,787,520 |
| 64GB | 16,383*) | 16 | 63 | 125,304,832 | 64,156,073,984 |

*) The CHS access is limited to about 8GB. Above 8GB the drive must be addressed in LBA mode.

5 Electrical interface

5.1 Electrical description

The CFAST CARD is connected with a standard 7 pin SATA connector and a standard 15 pin SATA power connector.

The signal/pin assignments and descriptions are listed in Table 10.

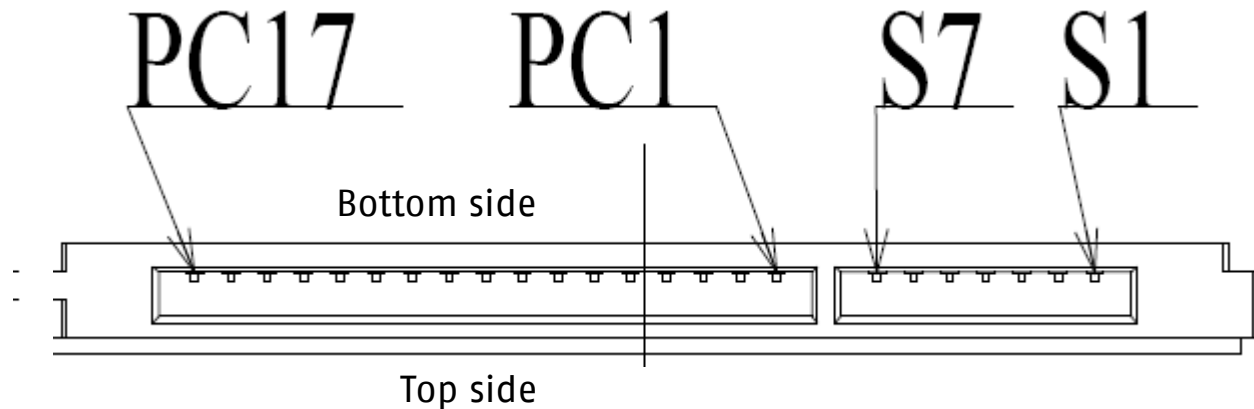


Table 10: Pin Assignment, name, and description

| Pin | Signal Name | Description |
|-------------|-------------|--|
| S1 | SGround | Signal Ground |
| S2 | A+ | + Differential Device Receive signal |
| S3 | A- | - Differential Device Receive signal |
| S4 | SGround | Signal Ground |
| S5 | B- | - Differential Device Transmit signal |
| S6 | B+ | + Differential Device Transmit signal |
| S7 | SGround | Signal Ground |
| PC1 | CDI *) | Card detect in |
| PC2 | PGround | Power Ground |
| PC3...PC6 | reserved | not used |
| PC7 | PGround | Power Ground |
| PC8 | LED1 | LED output for device activity (driven low) |
| PC9 | LED2 | LED output for SATA link indication (driven low) |
| PC10 | IO1 | Write protect input (low active) |
| PC11...PC12 | IO2...3 | not used |
| PC13...PC14 | 3.3V | Device power 3.3V |
| PC15...PC16 | PGround | Power Ground |
| PC17 | CDO *) | Card detect out |

*) CDI This pin is connected to CDO and to the card controller.
 If CDI is not driven by the host, it should be connected to GND (see section 5.4)
 It can be used for PHYSLP functionality (see section 5.4)

5.2 Electrical Specification

Table 11 and Table 12 define the DC Characteristics of the CFAST card. Unless otherwise stated, conditions are:

- $V_{CC} = 3.3V \pm 5\%$
- $0^{\circ}C$ to $+70^{\circ}C$

The current is measured by connecting an amp meter in series with the Vcc supply. The meter should be set to the 2A scale range, and have a fast current probe with an RC filter with a time constant of 0.1ms. Current measurements are taken while looping on a data transfer command with a sector count of 128. Current consumption values for both read and write commands are not to exceed the Maximum Average RMS Current specified in Table 12.

Table 11: Absolute Maximum Conditions

| Parameter | Symbol | Conditions |
|-------------|--------|---------------|
| Input Power | VCC | -0.3V to 3.6V |

Table 12: Input Power write and read

| Mode | Maximum Average RMS Current | Conditions |
|---------|-----------------------------|---------------|
| SATA II | 250mA | -40... +85 °C |
| SATA I | 220mA | |

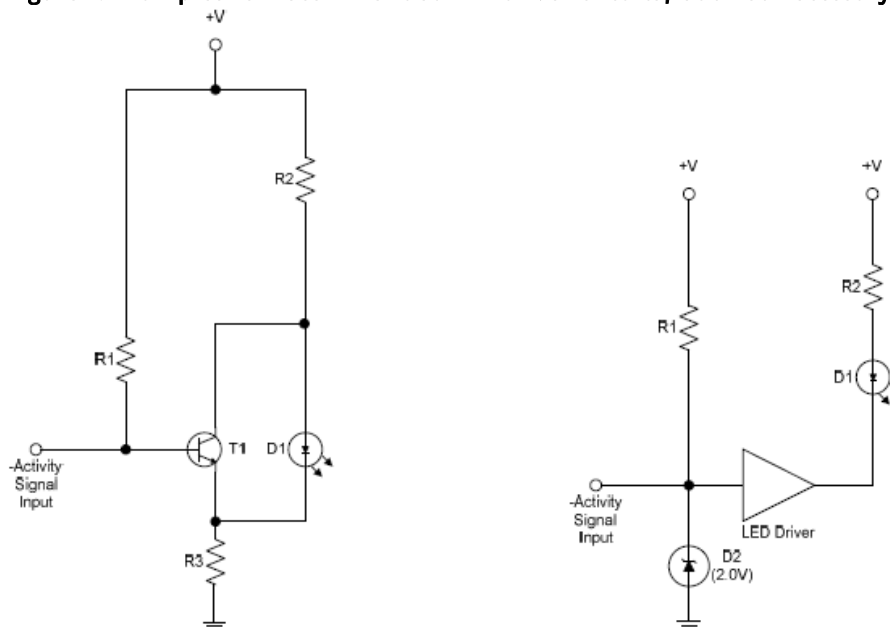
5.3 LED and IO-pins

LED1 is the DASP signal and is held low for every command and is not driven in idle mode.

LED2 is the SATA link indicator and is driven low, if the SATA is connected and active.

LED1 and LED2 pin is driven low and only pulled up weakly. So this pin can be tied low by the host without accidental current through these pins. The LED pins can be used to display the function of the card. The LED1 and LED2 pins could drive up to 10mA directly for an LED with serial resistance to 3.3V. It is recommended to use an LED driver circuit.

Figure 1: Examples for recommended LED driver circuits, but not necessary



IO1 pin is the write protect pin.

If this pin tied low, the card is write protected and rejects all write commands.

5.4 Card detection and PHYSLP functions with CDI and CDO pin

5.4.1 General

The CFast card connector contains two signals, CDI and CDO. These signals enable two functions:

- Card Detect. This function enables the host to detect when the card is fully inserted. For example, the host may wish to power up the card only after it is inserted, or turn on an LED when the card is properly inserted.
- PHYSLP. This function is a CFast power management protocol which may be invoked when the SATA connection is in Slumber mode. Please see the CFast specifications for a complete description. The purpose of this function is to enable the device to turn off the SATA PHY completely, saving power. The host may turn off its own PHY when invoking this function.

Swissbit F-2x0 support Card detect and PHYSLP functionality

This section explains recommended methods for the host to interface with the card so that the card will not be damaged, and to ensure compatibility between the card and the host regarding the above described functions.

5.4.2 Connection when the host uses the Card Detect functionality only

The host needs to take into account the following restrictions:

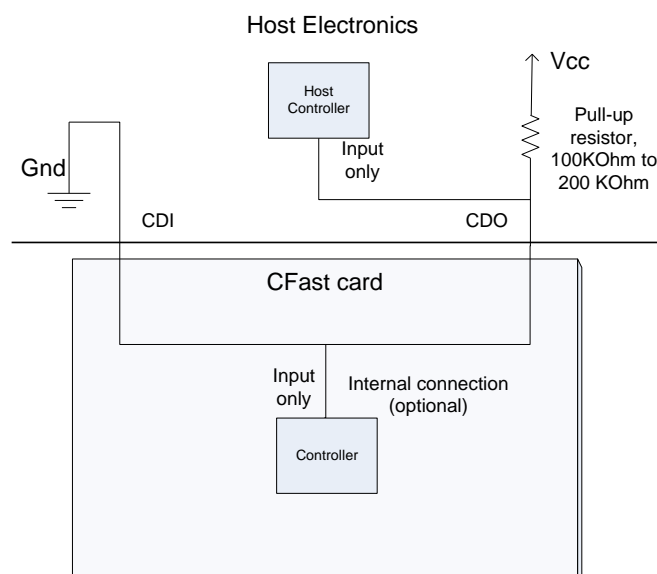
- CDI and CDO are shorted together on the CFast card.
- The card may not have Vcc connected directly to CDI or to CDO.
(The newest F-2x0 cards have a serial resistor between CDI and controller)
- The CDI – CDO signal on the F-2x0 card is connected to a card controller input pin.
- The card doesn't actively drive the CDI or CDO signals.

Based on the above, the following is recommended:

- CDI will be connected to Gnd.
- CDO will be connected to an input port on the host controller.
- CDO will be connected to a pull-up resistor on the host. The value of the resistor is calculated so that the voltage drop across the resistor when the card CDO is connected and CDI is not connected will not exceed 0.4V. The leakage current of the card controller is up to 1 μ A. As an example, if the host controller leakage is also 1 μ A, the pull-up resistor may have a value of up to 200K Ω . It is recommended that the pull-up resistor value will be as high as possible in order to have no effect on the card controller and to conserve power.

See Figure 2

Figure 2: CFast connection for Card Detect functionality only



5.4.3 Connection when the card uses the Card Detect functionality and the PHYSLP functionality

The circuit is modified when PHYSLP is intended to be used. CDI is connected to an active LVCMOS level output port on the host controller.

The same restrictions as in the previous section apply.

Based on the above, the following is recommended:

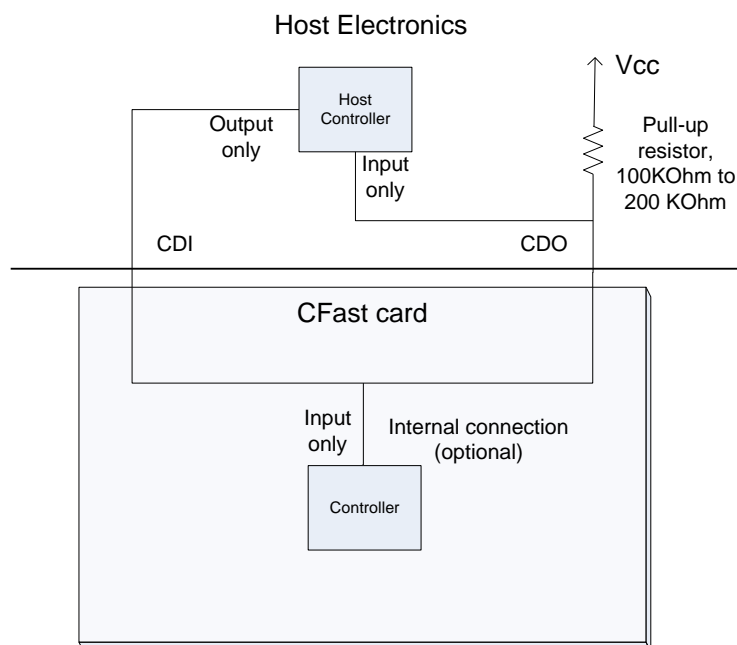
- a. CDI will be connected to a host controller output port.
- b. CDO will be connected to an input port on the host controller.
- c. CDO will be connected to a pull-up resistor on the host. The value of the resistor is calculated so that the voltage drop across the resistor when the card CDO is connected and CDI is not connected will not exceed 0.4V. The leakage current of the card controller is up to 1µA. As an example, if the host controller leakage is also 1µA, the pull-up resistor may have a value of up to 200KΩ . It is recommended that the pull-up resistor value will be as high as possible in order to have no effect on the card controller and to conserve power.
- d. During normal operation CDI will, by default, be driven by the host controller to a logic LOW level. This enables Card Detect functionality, the same as in section 5.4.2 .

When a card supports the PHYSLP functionality, SATA is in Slumber mode, and the host wants to put the card into PHYSLP mode, the host will

1. Disregard the CDO input port.
 2. Drive CDI to a logic HIGH level
- e. In case the Card Detect functionality is required while in the PHYSLP power mode, there is a mechanism described in the CFast specification. This mechanism consists of pulsing CDI to logic LOW for a period of less than 2 milliseconds, and sampling CDO while CDI is at logic LOW. The CFast specification specifies that a CDI pulse going to logic LOW of less than 2 milliseconds will not affect the device PHYSLP state.

See Figure 3.

Figure 3 – CFast connection for Card Detect and PHYSLP functionality



5.5 Power Management

See the SATA specification for more information on SATA PHY power modes.

SATA PHY power modes affect only the SATA PHY, not the device power status. PHYSLP mode can be used by the host to relatively quickly minimize (and restore) PHY power. It may also be used to further reduce CFast device power after the host has sent commands to put the CFast device in a low power device state.

A device's ability to support PHYSLP mode is indicated in Identify Drive Word 161 (CFast Specific Support).

5.5.1 PHYSLP protocol overview

If the host and device support PHYSLP mode the following protocols shall be used to enter and exit PHYSLP mode.

To enter PHYSLP mode the protocol is:

- The host shall send a request for the card to enter the SATA PHY Slumber mode. See the SATA specification for more information.
- After the CFast PHY has gone into Slumber power mode, the host shall deassert CDI.
- The host and the device shall power down their respective PHYs retaining calibration information.
- After deasserting CDI and entering PHYSLP mode, the host may assert CDI for a period of less than one millisecond to check for device presence.

To exit PHYSLP mode the protocol is:

- The host shall assert CDI. The CFast card shall not respond to CDI assertions of less than two milliseconds.
- The host and the device shall power up their respective PHYs into SATA PHY Slumber mode.

The device shall send a SATA COMWAKE signal to begin the SATA defined slumber to PHYRDY sequence (see section "Power-On Sequence State Machine" in the SATA specification).

Figure 4: PHYSLP entry timing diagram

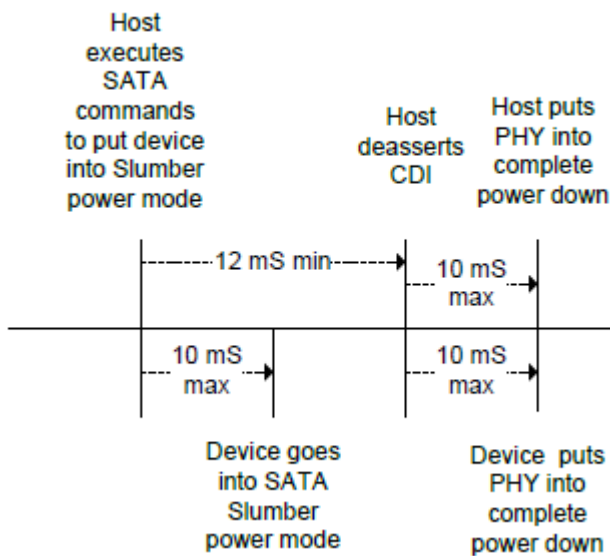
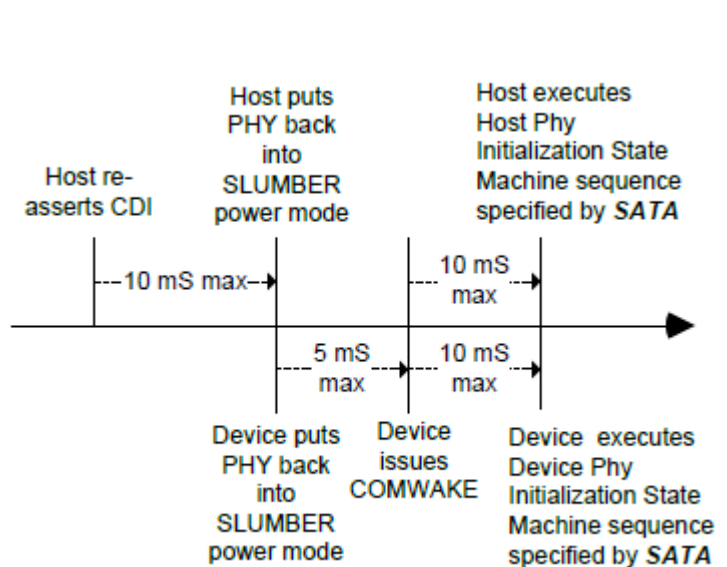


Figure 5: PHYSLP exit timing diagram



6 ATA command description

This section provides information on the ATA commands supported by the CFAST card. The commands are issued to the ATA by loading the required registers in the command block with the supplied parameter, and then writing the command code to the register.

ATA Command Flow

- DDMAIo: DMA_in State** This state is activated when the device receives a DMA data-in command or the transmission of one or more data FIS is required to complete the command. When in this state, the device shall prepare the data for transfer of a data FIS to the host.
- Transition DDMAIo:1 When the device has the data ready to transfer a data FIS, the device shall transition to the DDMAI1: Send_data state. Transition DDMAIo:2 When the device has transferred all of the data requested by this command or has encountered an error that causes the command to abort before completing the transfer of the requested data, then the device shall transition to the DDMAI2: Send_status state.
- DDMAI1: Send_data** This state is activated when the device has the data ready to transfer a data FIS to the host. When in this state, the device shall request that the Transport layer transmit a data FIS containing the data. The device command layer shall request a Data FIS size of no more than 2,048 Dwords (8KB).
- Transition DDMAI1:1 When the data FIS has been transferred, the device shall transition to the DMAOIo: DMA_in state.
- DDMAI2: Send_status** This state is activated when the device has transferred all of the data requested by the command or has encountered an error that causes the command to abort before completing the transfer of the requested data. When in this state, the device shall request that the Transport layer transmit a Register FIS with the register content as described in the command description in the ATA/ATAPI-6 standard and the I bit set to one.
- Transition DDMAI2:1 When the FIS has been transmitted, the device shall transition to the DIo: Device_idle state.

For reasons of backward compatibility some commands are implemented as 'no operation' NOP.
Table 13 summarizes the Drive command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 13: ATA Command Set⁽¹⁾

| Command | Code | FR(1) | SC(2) | SN(3) | CY(5:4) | DH(6) | LBA(5:3) |
|-----------------------------|------------|-------|-------|-------|---------|-------|----------|
| Check Power Mode | E5h or 98h | | | | | D | |
| Data Set Management | 06h | | YY | | | D | YY |
| Execute Drive Diagnostic | 90h | | | | | D | |
| Flush cache | E7h | | | | | D | |
| Flush cache Ext | EAh | | | | | D | |
| Format track | 50h | | Y | | Y | Y | Y |
| Identify Drive | ECh | | | | | D | |
| Idle | E3h or 97h | | Y | | | D | |
| Idle Immediate | E1h or 95h | | | | | D | |
| Media Lock | DEh | | | | | D | |
| Media Unlock | DFh | | | | | D | |
| NOP | 00h | | | | | D | |
| Read Buffer | E4h | | | | | D | |
| Read DMA | C8 | | Y | Y | Y | Y | Y |
| Read DMA Ext | 25h | | YY | | | D | YY |
| Read FPDMA Queued | 60h | Y | Y | Y | Y | D | Y |
| Read Multiple | C4h | | Y | Y | Y | Y | Y |
| Read Multiple Ext | 29h | | YY | | | D | YY |
| Read native max address | F8h | | | | | D | |
| Read native max address Ext | 27h | | | | | D | |
| Read Sector(s) | 20h | | Y | Y | Y | Y | Y |
| Read Sector(s) Ext 2) | 24h | | YY | YY | YY | D | YY |
| Read Verify Sector(s) | 40h or 41h | | Y | Y | Y | Y | Y |
| Read Verify Sector(s) Ext | 42h | | YY | YY | YY | D | YY |
| Recalibrate | 1Xh | | | | | D | |
| Security Disable Password | F6h | | | | | D | |
| Security Erase Prepare | F3h | | | | | D | |
| Security Erase Unit | F4h | | | | | D | |
| Security Freeze Lock | F5h | | | | | D | |
| Security Set Password | F1h | | | | | D | |
| Security Unlock | F2h | | | | | D | |
| Seek | 7Xh | | | Y | Y | Y | Y |
| Set Features | EFh | Y | | | | D | |
| Set max address | F9h | | Y | Y | Y | Y | Y |
| Set max address Ext | 37h | | YY | YY | YY | D | YY |
| Set Multiple Mode | C6h | | Y | | | D | |
| Set Sleep Mode | E6h or 99h | | | | | D | |
| S.M.A.R.T. | Boh | Y | Y | | Y | D | |
| Stand By | E2h or 96h | | | | | D | |
| Stand By Immediate | E0h or 94h | | | | | D | |
| Write Buffer | E8h | | | | | D | |
| Write DMA | CAh or CBh | | Y | Y | Y | Y | Y |
| Write DMA Ext | 35h | | YY | YY | YY | D | YY |
| Write FPDMA Queued | 61h | | Y | Y | Y | D | Y |
| Write Multiple | C5h | | Y | Y | Y | Y | Y |
| Write Multiple Ext | 39h | | YY | YY | YY | D | YY |
| Write Sector(s) | 30h | | Y | Y | Y | Y | Y |
| Write Sector(s) Ext | 34h | | YY | YY | YY | D | YY |
| Write Verify | 3Ch | | Y | Y | Y | Y | Y |

- FR = Features Register (1), SC = Sector Count Register (2), SN = Sector Number Register (3), CY = Cylinder Registers (5:4),
DH = Drive/Head Register (6), LBA = Logical Block Address Mode Supported (see command descriptions for use),
Y – The register contains a valid parameter for this command. For the Drive/Head Register Y means both the Drive and head parameters are used.
YY – registers must be written twice for 48bit LBA commands
D – only the Drive parameter is valid and not the head parameter C – the register contains command specific data (see command descriptors for use).
- To read out the higher and lower byte of the 16bit registers bit7 of the Device Control Register (write to Alternate status register) must be set to 1 or 0, respectively.

6.1 Check Power Mode (98h or E5h)

This command checks the power mode.

Issuing the command while the Drive is in Standby mode, is about to enter Standby, or is exiting Standby, the command will set BSY, set the Sector Count Register to 00h, clear BSY and generate an interrupt.

Issuing the command when the Drive is in Idle mode will set BSY, set the Sector Count Register to FFh, clear BSY and generate an interrupt.

Table 14 defines the Byte sequence of the Check Power Mode command.

Table 14: Check Power Mode

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|------------|----|----|---|----|---|---|---|
| COMMAND | 98h or E5h | | | | | | | |
| DRIVE/HEAD | nu | nu | nu | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

6.2 Data Set Management (06h) TRIM

This 48-bit command is optional for ATA devices. The DATA SETMANAGEMENT command is not part of any feature set.

The DATA SET MANAGEMENT command provides information for device optimization (e.g., file system information).

See Table 15 for the DATA SET MANAGEMENT command inputs.

Table 15: Data Set Management

| register write | previous | current | | | | | | | |
|--------------------|----------|---|---|----|---------------------|----------|---|---|------|
| Task File Register | 15:8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMMAND | nu | 06h | | | | | | | |
| DRIVE/HEAD | nu | nu | L | nu | Transport dependent | Reserved | | | |
| LBA High | Reserved | | | | | | | | |
| LBA Mid | Reserved | | | | | | | | |
| LBA Low | Reserved | | | | | | | | |
| SECTOR COUNT | 15:8 | 7:0 Number of 512-byte blocks to be transferred; the value of zero is reserved. | | | | | | | |
| FEATURES | Reserved | | | | | | | | TRIM |

Currently this command is specified only for the TRIM command.

Currently only one 512-byte block can be transferred with one command (see Identify Device word 169).

Detailed information about the TRIM command is available in the ATA/ATAPI Command Set-2 (ACS-2) at

www.t13.org

6.3 Execute Drive Diagnostic (90h)

This command performs the internal diagnostic tests implemented by the Drive.

The Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with the status for both devices.

Table 16 defines the Execute Drive Diagnostic command Byte sequence. The Diagnostic codes shown in Table 17 are returned in the Error Register at the end of the command.

Table 16: Execute Drive Diagnostic

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|----|----|---|----|---|---|---|
| COMMAND | 90h | | | | | | | |
| DRIVE/HEAD | nu | nu | nu | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

Table 17: Diagnostic Codes

| Code | Error Type |
|------|----------------------------------|
| 01h | No Error Detected |
| 02h | Formatter Device Error |
| 03h | Sector Buffer Error |
| 04h | ECC Circuitry Error |
| 05h | Controlling Microprocessor Error |

6.4 Flush Cache (E7h)

This command causes the drive to complete writing data from its cache. The drive returns status with RDY=1 and DSC=1 after the data in the write cache buffer is written to the media. If the drive does not support the Flush Cache command, the drive shall return command aborted.

Table 18: Flush Cache

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|----|----|---|----|---|---|---|
| COMMAND | E7h | | | | | | | |
| DRIVE/HEAD | nu | nu | nu | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

6.5 Flush Cache Ext (EAh) 48bit LBA

This command causes the card to complete writing data from its volatile cache into non-volatile memory. The BSY bit shall remain set to one until all data has been successfully written or an error occurs. The card returns status with RDY=1 and DSC=1 after the data in the write cache buffer is written to the media. If the Compact Flash Storage Card does not support the Flush Cache Ext command, the Compact Flash Storage Card shall return command aborted. See Table 19 for the DATA SET MANAGEMENT command inputs.

Table 19: Flush cache Ext

| register write | previous | current | | | | | | | |
|--------------------|----------|---------|---|---|-------|----------|---|---|---|
| Task File Register | 15:8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMMAND | - | EAh | | | | | | | |
| DRIVE/HEAD | - | 1 | 1 | 1 | Drive | Reserved | | | |
| LBA High | nu | nu | | | | | | | |
| LBA Mid | nu | nu | | | | | | | |
| LBA Low | nu | nu | | | | | | | |
| SECTOR COUNT | nu | nu | | | | | | | |
| FEATURES | nu | nu | | | | | | | |

An unrecoverable error encountered while writing data results in aborting the command and the Command Block registers contain the 48-bit sector address of the sector where the first unrecoverable error occurred. Subsequent FLUSH CACHE EXT commands continue the process of flushing the cache starting with the first sector after the sector in error.

This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

6.6 Format track (50h)

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h). To remain host backward compatible, the CompactFlash™ Storage Card expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the CompactFlash™ Storage Card. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256). The use of this command is not recommended.

Table 20: Format track

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|--|---|----|---|---|---|---|---|
| COMMAND | 50h | | | | | | | |
| DRIVE/HEAD | nu | L | nu | D | H[3:0] or LBA[27:24] of the starting sector/LBA | | | |
| CYLINDER HI | Cylinder[15:8] or LBA[23:16] of the first sector/LBA | | | | | | | |
| CYLINDER LOW | Cylinder[7:0] or LBA[15:8] of the first sector/LBA | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | Sector Count (LBA only) | | | | | | | |
| FEATURES | nu | | | | | | | |

6.7 Identify Device (ECh)

The Identify Device command enables the host to receive parameter information from the Drive. This command has the same protocol as the Read Sector(s) command. Table 21 defines the Identify Device command Byte sequence. All reserved bits or Words are zero.

Table 22 shows the definition of each field in the Identify Drive Information.

Table 21: Identify Device

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|----|----|---|----|---|---|---|
| COMMAND | ECh | | | | | | | |
| DRIVE/HEAD | nu | nu | nu | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

Table 22: Identify Device Information

| Word Address | Default Value | Total Bytes | Data Field Type Information |
|--------------|---------------|-------------|---|
| 0 | 045Ah* | 2 | Standard Configuration FIX (optional 848Ah for removable) |
| 1 | XXXXh | 2 | Default number of cylinders (obsolete) |
| 2 | 0000h | 2 | Reserved |
| 3 | 00XXh | 2 | Default number of heads (obsolete) |
| 4 | 0000h | 2 | Obsolete |
| 5 | 0200h | 2 | Obsolete |
| 6 | XXXXh | 2 | Default number of sectors per track (obsolete) |
| 7-8 | XXXXh | 4 | Number of sectors per Drive (Word 7 = MSW, Word 8 = LSW) |
| 9 | 0000h | 2 | Obsolete |
| 10-19 | aaaa | 20 | Serial number in ASCII (right justified) |
| 20 | 0002h | 2 | Buffer type (dual ported multi-sector) retired |
| 21 | 0001h | 2 | Buffer Size in 512byte increment (obsolete) |
| 22 | 0004h | 2 | Reserved |
| 23-26 | YYYY* | 8 | Firmware revision in ASCII. Big Endian Byte Order in Word |
| 27-46 | YYYY* | 40 | Model number in ASCII (right justified ("SFCAxxxxHxBVxxx-x-xx-xxx-xxx")) |
| 47 | 8001h | 2 | Maximum number of sectors on Read/Write Multiple command |
| 48 | 0000h | 2 | Double word not supported |
| 49 | oF00h* | 2 | Capabilities with DMA, LBA, IORDY supported |
| 50 | 4001h | 2 | Capabilities |
| 51 | 0200h | 2 | PIO data transfer cycle timing mode 2 |
| 52 | 0000h | 2 | Obsolete |
| 53 | 0007h | 2 | Field validity (Bytes 54-58, 64-70, 88) |
| 54 | XXXXh | 2 | Current numbers of cylinders (obsolete) |
| 55 | XXXXh | 2 | Current numbers of heads (obsolete) |
| 56 | XXXXh | 2 | Current sectors per track (obsolete) |
| 57-58 | XXXXh | 4 | Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW) (obsolete) |
| 59 | 010Xh* | 2 | Multiple sector setting (can be changed by host). |
| 60-61 | XXXXh | 4 | Total number of sectors addressable in LBA Mode |
| 62 | 0000h | 2 | Single Word DMA transfer not implemented |

| Word Address | Default Value | Total Bytes | Data Field Type Information |
|--------------|----------------------------|-------------|---|
| 63 | 0X07h* 0000h* | 2 | Multi-Word DMA transfer support and selection (can changed by host). no multi-word DMA |
| 64 | 0003h | 2 | Advanced PIO modes 3 and 4 supported |
| 65 | 0078h* | 2 | Minimum Multi-Word DMA transfer cycle time per Word. |
| 66 | 0078h* | 2 | Recommended Multi-Word DMA transfer cycle time. |
| 67 | 0078h* | 2 | Minimum PIO transfer cycle time without flow control |
| 68 | 0078h* | 2 | Minimum PIO transfer cycle time with IORDY flow control |
| 69 | 8000h | 2 | CFast specification supported |
| 70-74 | 0000h | 10 | Reserved |
| 75 | 001Fh* | 2 | Queue depth 32 for NCQ, if supported |
| 76 | 0306h* 0206h* | 2 | SATA Capabilities (Bit 8 for NCQ) |
| 77 | 0000h | 2 | Reserved |
| 78 | 0000h* | 2 | SATA Feature support |
| 79 | 0000h* | | SATA Features enabled (can be changed by host) |
| 80-81 | 01E0h FFFFh | 4 | ATA version 5 to ATA version 8 |
| 82-84 | 742Bh* 7401h* 4020h* | 6 | Features/command sets supported |
| 85-87 | 7409h* B401h* 4020h* | 6 | Features/command sets enabled (can change in operation) |
| 88 | XX7F* | 2 | UDMA Mode Supported 0 to 6 and Selected (changes in operation) |
| 89 | 0000h* | 2 | Time for security erase unit completion |
| 90 | 0000h* | 2 | Time for enhanced security erase unit completion |
| 91 | 0000h | 2 | Reserved |
| 92 | FFFE* | 2 | Master Password Revision Code |
| 93-99 | 0000h* | 14 | Reserved |
| 100-103 | XXXXh* | 8 | Total number of sectors addressable in LBA48 mode |
| 104 | 0000h | 2 | Reserved |
| 105 | 0001h | 2 | Number of sectors per Data Set management command (TRIM) |
| 106-107 | 0000h | 4 | Reserved |
| 108-111 | 0000h* | 8 | World Wide Name |
| 112-118 | 0000h | 14 | Reserved |
| 119 | 4000h | 2 | Command set/feature set supported extension |
| 120 | 4000h* | 2 | Command set/feature set enabled extension |
| 121-127 | 0000h | 14 | Reserved |
| 128 | 0009h* | 2 | Security Status (changes in operation) |
| 129 | XX00h* | 2 | Write Protect Status (Vendor specific) |
| 130-159 | XXXXh | 60 | Vendor specific |
| 160 | 80FAh* | 2 | CFA Max. current (e.g. 250mA) |
| 161 | 8001h* | 2 | CFast PHYSLP mode supported |
| 162-168 | 0000h | 14 | Reserved |
| 169 | 0001h | 2 | Trim bit in Data Set Management supported |
| 170-216 | 0000h | 94 | Reserved |
| 217 | 0001h | 2 | Nominal Media Rotation Rate: Solid State Device |
| 218-221 | 0000h | 8 | Reserved |
| 222 | 101fh | 2 | Transport major version: Serial transport, SATA rev 2.6 |
| 223 | FFFFh | 2 | Transport minor version: not supported |
| 224-254 | 0000h | 62 | Reserved |
| 255 | XXA5h | 2 | Integrity word |

* Standard values, depending on configuration

XXXX Depending on drive capacity and drive geometry

YYYY Depending on drive configuration

6.7.1 Word 0: General Configuration

This field indicates the general characteristics of the device.

The default value for Word 0 is set to **045Ah**.

Some operating systems require Bit 6 of Word 0 to be set to '1' (Non-removable device) to use the drive as the root storage device.

6.7.2 Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

6.7.3 Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

6.7.4 Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

6.7.5 Word 7–8: Number of Sectors per Drive

This field contains the number of sectors per Drive. This double Word value is also the first invalid address in LBA translation mode.

6.7.6 Word 10–19: Memory Drive Serial Number

The contents of this field are right justified and padded without spaces (20h).

6.7.7 Word 23–26: Firmware Revision

This field contains the revision of the firmware for this product.

6.7.8 Word 27–46: Model Number

This field contains the model number for this product and is left justified and padded with spaces (20h).

6.7.9 Word 47: Read/Write Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read Multiple or Write Multiple commands.

6.7.10 Word 49: Capabilities

- Bit 13 Standby Timer: is set to '0' to indicate that the Standby timer operation is defined by the manufacturer.
- Bit 11: IORDY Supported
 - If bit 11 is set to 1 then this drive supports IORDY operation.
 - If bit 11 is set to 0 then this drive may support IORDY operation.
- Bit 10: IORDY may be disabled
 - If bit 10 is set to 1 then IODRDY may be disabled.
- Bit 9 LBA support: drive support LBA mode addressing.
- Bit 8 DMA Support: Read/Write DMA commands are supported.

6.7.11 Word 50: Capabilities

- Bit 0 shall be set to one to indicate a vendor specific Standby timer value minimum.

6.7.12 Word 51: PIO Data Transfer Cycle Timing Mode

This field defines the mode for PIO data transfer. For backward compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51, the highest original PIO mode it can support (PIO mode 0, 1 or 2). Bits 15:8 are set to 02H.

6.7.13 Word 53: Translation Parameter Valid

- Bit 0: is set to '1' to indicate that Words 54 to 58 are valid
- Bit 1: is set to '1' to indicate that Words 64 to 70 are valid

- Bit 2 shall be set to 1 indicating that word 88 is valid and reflects the supported UDMA

6.7.14 Word 54–56: Current Number of Cylinders, Heads, Sectors/Track

These fields contain the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

6.7.15 Word 57–58: Current Capacity

This field contains the product of the current cylinders, heads and sectors.

6.7.16 Word 59: Multiple Sector Setting

- Bits 15–9 are reserved and must be set to '0'.
- Bit 8 is set to '1', to indicate that the Multiple Sector Setting is valid.
- Bits 7:0 are the current setting for the number of sectors to be transferred for every interrupt, on Read/Write Multiple commands; the only values returned are '00h' or '01h'.

6.7.17 Word 60–61: Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the Drive in LBA mode only.

6.7.18 Word 63: Multi-Word DMA transfer

Bits 15 through 8 of word 63 of the Identify Device parameter information is defined as the Multiword DMA mode selected field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Only one of bits may be set to one in this field by the drive to indicate the multiword DMA mode which is currently selected.

Of these bits, bits 15 through 11 are reserved. Bit 8, if set to one, indicates that Multiword DMA mode 0 has been selected. Bit 9, if set to one, indicates that Multiword DMA mode 1 has been selected. Bit 10, if set to one, indicates that Multiword DMA mode 2 has been selected.

Selection of Multiword DMA modes 3 and above are specific to Drive are as described in Word 163.

Bits 7 through 0 of word 63 of the Identify Device parameter information is defined as the Multiword DMA data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the drive to indicate the Multiword DMA modes it is capable of supporting.

Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the drive supports Multiword DMA mode 0. Bit 1, if set to one, indicates that the drive supports Multiword DMA modes 1 and 0. Bit 2, if set to one, indicates that the Drive supports Multiword DMA modes 2, 1 and 0.

Support for Multiword DMA modes 3 and above are specific to Drive are reported in word 163 as described in Word 163.

6.7.19 Word 64: Advanced PIO transfer modes supported

This field is bit significant. Any number of bits may be set to '1' in this field by the drive to indicate the advanced PIO modes it is capable of supporting.

- Bits 7–2 are reserved for future advanced PIO modes.
- Bit 1 is set to '1', indicates that the Drive supports PIO mode 4.
- Bit 0 is set to '1' to indicate that the Drive supports PIO mode 3.

Support for PIO modes 5 and above are specific to Drive are reported in word 163 as described in Word 163.

6.7.20 Word 65: Minimum Multi-Word DMA transfer cycle time

Word 65 of the parameter information of the Identify Device command is defined as the minimum Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the Drive guarantees data integrity during the transfer.

If this field is supported, bit 1 of word 53 shall be set to one. The value in word 65 shall not be less than the minimum cycle time for the fastest DMA mode supported by the device. This field shall be supported by all Drives supporting DMA modes 1 and above. If bit 1 of word 53 is set to one, but this field is not supported, the Drive shall return a value of zero in this field.

6.7.21 Word 66: Recommended Multi-Word DMA transfer cycle time

Word 66 of the parameter information of the Identify Device command is defined as the recommended Multiword DMA transfer cycle time. This field defines, in nanoseconds, the cycle time that, if used by the host, may optimize the data transfer from by reducing the probability that the Drive will need to negate the DMARQ signal during the transfer of a sector.

If this field is supported, bit 1 of word 53 shall be set to one. The value in word 66 shall not be less than the value in word 65. This field shall be supported by all Drives supporting DMA modes 1 and above. If bit 1 of word 53 is set to one, but this field is not supported, the Drive shall return a value of zero in this field.

6.7.22 Word 67: Minimum PIO transfer cycle time without flow control

Word 67 of the parameter information of the Identify Device command is defined as the minimum PIO transfer without flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the Drive guarantees data integrity during the transfer without utilization of flow control.

If this field is supported, Bit 1 of word 53 shall be set to one.

Any Drive that supports PIO mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68.

If bit 1 of word 53 is set to one because a Drive supports a field in words 64–70 other than this field and the Drive does not support this field, the Drive shall return a value of zero in this field.

6.7.23 Word 68: Minimum PIO transfer cycle time with IORDY

Word 68 of the parameter information of the Identify Device command is defined as the minimum PIO transfer with IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that the Drive supports while performing data transfers while utilizing IORDY flow control.

If this field is supported, Bit 1 of word 53 shall be set to one.

Any Drive that supports PIO mode 3 or above shall support this field, and the value in word 68 shall be the fastest defined PIO mode supported by the Drive.

If bit 1 of word 53 is set to one because a Drive supports a field in words 64–70 other than this field and the Drive does not support this field, the Drive shall return a value of zero in this field.

6.7.24 Word 69: CFAST Specification

- Bit 15 is set to '1' to indicate that CFAST specification is supported.

6.7.25 Word 75: Queue depth for NCQ

- Bit 15:5 Reserved
- Bit 4:0 Maximum queue depth -1

6.7.26 Word 76: Serial ATA Capabilities

- Bit 15:11 Reserved
- Bit 10 1 = Supports Phy Event Counters
- Bit 9 1 = Supports receipt of host initiated power management requests
- Bit 8 1 = Supports native Command Queuing
- Bit 7:3 Reserved for future SATA signaling speed grades
- Bit 2 1 = Supports SATA Gen2 Signaling Speed (3.0Gb/s)
- Bit 1 1 = Supports SATA Gen1 Signaling Speed (1.5Gb/s)
- Bit 0 Shall be cleared to zero

6.7.27 Word 78: SATA Feature support

- Bit 15–7 Reserved
- Bit 6 1 = Supports software settings preservation
- Bit 5 1 = Supports asynchronous notification
- Bit 4 1 = Supports in-order data delivery
- Bit 3 1 = Device supports initiating interface power management
- Bit 2 1 = Supports DMA Setup Auto-Activate optimization
- Bit 1 1 = Supports non-zero buffer offsets
- Bit 0 Shall be cleared to zero

6.7.28 Word 79: SATA Features enabled

- Bit 15–7 Reserved
- Bit 6 1 = Supports software settings preservation enabled
- Bit 5 1 = Supports asynchronous notification enabled
- Bit 4 1 = Supports in-order data delivery enabled
- Bit 3 1 = Device supports initiating interface power management enabled
- Bit 2 1 = Supports DMA Setup Auto-Activate optimization enabled

- Bit 1 1 = Supports non-zero buffer offsets enabled
- Bit 0 Shall be cleared to zero

6.7.29 Words 82–84: Features/command sets supported

Words 82, 83, and 84 shall indicate features/command sets supported. The value 0000h or FFFFh was placed in each of these words by Drives prior to ATA-3 and shall be interpreted by the host as meaning that features/command sets supported are not indicated. Bits 1 through 13 of word 83 and bits 0 through 13 of word 84 are reserved. Bit 14 of word 83 and word 84 shall be set to one and bit 15 of word 83 and word 84 shall be cleared to zero to provide indication that the features/command sets supported words are valid. The values in these words should not be depended on by host implementers.

Word 82

- Bit15 Obsolete
- Bit14 1 = NOP command supported
- Bit13 1 = READ BUFFER command supported
- Bit12 1 = WRITE BUFFER command supported
- X 11 Obsolete
- Bit10 1 = Host Protected Area feature set supported
- Bit9 1 = DEVICE RESET command supported
- Bit8 1 = SERVICE interrupt supported
- Bit7 1 = release interrupt supported
- Bit6 1 = look-ahead supported
- Bit5 1 = write cache supported
- Bit4 Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.
- Bit3 1 = mandatory Power Management feature set supported
- Bit2 1 = Removable Media feature set supported
- Bit1 1 = Security Mode feature set supported
- Bit0 1 = SMART feature set supported

Word 83

- Bit15 Shall be cleared to zero
- Bit14 Shall be set to one
- Bit13 1 = FLUSH CACHE EXT command supported
- Bit12 1 = mandatory FLUSH CACHE command supported
- Bit11 1 = Device Configuration Overlay feature set supported
- Bit10 1 = 48-bit Address feature set supported
- Bit9 1 = Automatic Acoustic Management feature set supported
- Bit8 1 = SET MAX security extension supported
- Bit7 See Address Offset Reserved Area Boot, INCITS TR27:2001
- Bit6 1 = SET FEATURES subcommand required to spinup after power-up
- Bit5 1 = Power-Up In Standby feature set supported
- Bit4 1 = Removable Media Status Notification feature set supported
- Bit3 1 = Advanced Power Management feature set supported
- Bit2 1 = CFA feature set supported
- Bit1 1 = READ/WRITE DMA QUEUED supported
- Bit0 1 = DOWNLOAD MICROCODE command supported

Word 84

- Bit15 Shall be cleared to zero
- Bit14 Shall be set to one
- Bit13 1 = IDLE IMMEDIATE with UNLOAD FEATURE supported
- Bit12 Reserved for technical report
- Bit11 Reserved for technical report
- Bit10 1 = URG bit supported for WRITE STREAM DMA EXT and WRITE STREAM EXT
- Bit9 1 = URG bit supported for READ STREAM DMA EXT and READ STREAM EXT
- Bit8 1 = 64-bit World wide name supported
- Bit7 1 = WRITE DMA QUEUED FUA EXT command supported
- Bit6 1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported
- Bit5 1 = General Purpose Logging feature set supported
- Bit4 1 = Streaming feature set supported

- Bit3 1 = Media Card Pass Through Command feature set supported
- Bit2 1 = Media serial number supported
- Bit1 1 = SMART self-test supported
- Bit0 1 = SMART error logging supported

6.7.30 Words 85–87: Features/command sets enabled

Words 85, 86, and 87 shall indicate features/command sets enabled. The value 0000h or FFFFh was placed in each of these words by Drives prior to ATA-4 and shall be interpreted by the host as meaning that features/command sets enabled are not indicated. Bits 1 through 15 of word 86 are reserved. Bits 0–13 of word 87 are reserved. Bit 14 of word 87 shall be set to one and bit 15 of word 87 shall be cleared to zero to provide indication that the features/command sets enabled words are valid. The values in these words should not be depended on by host implementers.

Word85

- Bit15 Obsolete
- Bit14 1 = NOP command enabled
- Bit13 1 = READ BUFFER command enabled
- Bit12 1 = WRITE BUFFER command enabled
- Bit11 Obsolete
- Bit10 1 = Host Protected Area feature set enabled
- Bit9 1 = DEVICE RESET command enabled
- Bit8 1 = SERVICE interrupt enabled
- Bit7 1 = release interrupt enabled
- Bit6 1 = look-ahead enabled
- Bit5 1 = write cache enabled
- Bit4 Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.
- Bit3 1 = Power Management feature set enabled
- Bit2 1 = Removable Media feature set enabled
- Bit1 1 = Security Mode feature set enabled
- Bit0 1 = SMART feature set enabled

Word86

- Bit15–14 Reserved
- Bit13 1 = FLUSH CACHE EXT command supported
- Bit12 1 = FLUSH CACHE command supported
- Bit11 1 = Device Configuration Overlay supported
- Bit10 1 = 48-bit Address features set supported
- Bit 9 1 = Automatic Acoustic Management feature set enabled
- Bit8 1 = SET MAX security extension enabled by SET MAX SET PASSWORD
- Bit7 See Address Offset Reserved Area Boot, INCITS TR27:2001
- Bit6 1 = SET FEATURES subcommand required to spin-up after power-up
- Bit5 1 = Power-Up In Standby feature set enabled
- Bit4 1 = Removable Media Status Notification feature set enabled
- Bit3 1 = Advanced Power Management feature set enabled
- Bit2 1 = CFA feature set enabled
- Bit1 1 = READ/WRITE DMA QUEUED command supported
- Bit0 1 = DOWNLOAD MICROCODE command supported

Word87

- Bit15 Shall be cleared to zero
- Bit14 Shall be set to one
- Bit13 1 = IDLE IMMEDIATE with UNLOAD FEATURE supported
- Bit12 Reserved for technical report-
- Bit11 Reserved for technical report-
- Bit10 1 = URG bit supported for WRITE STREAM DMA EXT and WRITE STREAM EXT
- Bit9 1 = URG bit supported for READ STREAM DMA EXT and READ STREAM EXT
- Bit8 1 = 64 bit World wide name supported
- Bit7 1 = WRITE DMA QUEUED FUA EXT command supported
- Bit6 1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported
- Bit5 1 = General Purpose Logging feature set supported
- Bit4 1 = Valid CONFIGURE STREAM command has been executed
- Bit3 1 = Media Card Pass Through Command feature set enabled

- Bit2 1 = Media serial number is valid
- Bit1 1 = SMART self-test supported
- Bit0 1 = SMART error logging supported

6.7.31 Word 88: Ultra DMA Modes Supported and Selected

Word 88 identifies the Ultra DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is selected, then no Multiword DMA mode shall be selected. If a Multiword DMA mode is selected, then no Ultra DMA mode shall be selected. Support of this word is mandatory if Ultra DMA is supported. Word 88 shall return a value of 0 if the device does not support UDMA.

- Bit 15 Reserved
- Bit 14 1 = Ultra DMA mode 6 is selected 0 = Ultra DMA mode 6 is not selected
- Bit 13 1 = Ultra DMA mode 5 is selected 0 = Ultra DMA mode 5 is not selected
- Bit 12 1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected
- Bit 11 1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected
- Bit 10 1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected
- Bit 9 1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected
- Bit 8 1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected
- Bit 7 Reserved
- Bit 6 1 = Ultra DMA mode 6 and below are supported. Bits 5:0 shall be set to 1.
- Bit 5 1 = Ultra DMA mode 5 and below are supported. Bits 4:0 shall be set to 1.
- Bit 4 1 = Ultra DMA mode 4 and below are supported. Bits 3:0 shall be set to 1.
- Bit 3 1 = Ultra DMA mode 3 and below are supported, Bits 2:0 shall be set to 1.
- Bit 2 1 = Ultra DMA mode 2 and below are supported. Bits 1:0 shall be set to 1.
- Bit 1 1 = Ultra DMA mode 1 and below are supported. Bit 0 shall be set to 1.
- Bit 0 1 = Ultra DMA mode 0 is supported

6.7.32 Word 89: Time required for Security erase unit completion

Word 89 specifies the time required for the SECURITY ERASE UNIT command to complete. Support of this word is mandatory if the Security feature set is supported.

Required Time= (Value*2) minutes

6.7.33 Word 92: Master Password Revision Code

Word 92 contains the value of the Master Password Revision Code set when the Master Password was last changed. Valid values are 000h through FFEh. A value of 000h or FFFh indicates that the Master Password Revision is not supported. Support of this word is mandatory if the Security feature set is supported.

6.7.34 Word 128: Security status

Support of this word is mandatory if the Security feature set is supported.

Bit 8 of word 128 indicates the security level. If security mode is enabled and the security level is high, bit 8 shall be cleared to zero. If security mode is enabled and the security level is maximum, bit 8 shall be set to one. When security mode is disabled, bit 8 shall be cleared to zero.

Bit 5 of word 128 indicates the Enhanced security erase unit feature is supported. If bit 5 is set to one, the Enhanced security erase unit feature set is supported.

Bit 4 of word 128 indicates that the security count has expired. If bit 4 is set to one, the security count is expired and SECURITY UNLOCK and SECURITY ERASE UNIT are command aborted until a power-on reset or hardware reset.

Bit 3 of word 128 indicates security frozen. If bit 3 is set to one, the security is frozen.

Bit 2 of word 128 indicates security locked. If bit 2 is set to one, the security is locked.

Bit 1 of word 128 indicates security enabled. If bit 1 is set to one, the security is enabled.

Bit 0 of word 128 indicates the Security Mode feature set supported. If bit 0 is set to one, security is supported.

6.7.35 Word 129: Write protect Status (Vendor information)

Word 129 identifies the Vendor Specific Write Status.

- Bit 15 = permanent write protect, out of spare blocks
- Bit 14 = permanent write protect due to table corruption
- Bit 13 = read protection due to table corruption
- Bit 9 = permanent write protect from vendor command
- Bit 8 = temporary write protect from vendor command

6.8 Idle (97h or E3h)

This command causes the Drive to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count (each count is 5ms) and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5ms) is different from the ATA specification. Table 23 defines the Byte sequence of the Idle command.

Table 23: Idle

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|------------------------------|----|----|---|----|---|---|---|
| COMMAND | 97h or E3h | | | | | | | |
| DRIVE/HEAD | nu | nu | nu | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | Timer Count (5ms increments) | | | | | | | |
| FEATURES | nu | | | | | | | |

6.9 Idle Immediate (95h or E1h)

This command causes the Drive to set BSY, enter the Idle mode, clear BSY and generate an interrupt. Table 24 defines the Idle Immediate command Byte sequence.

Table 24: Idle Immediate

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|------------|----|----|---|----|---|---|---|
| COMMAND | 95h or E1h | | | | | | | |
| DRIVE/HEAD | nu | nu | nu | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

6.10 Media Lock/Media Unlock (DEh/DFh)

This command is effective an NOP command and always fails with the Drive returning command aborted. Table 25 defines the Byte sequence of the commands.

Table 25: Media Lock/Media Unlock

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|---------|----|----|---|----|---|---|---|
| COMMAND | DEh/DFh | | | | | | | |
| DRIVE/HEAD | nu | nu | nu | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

6.11 NOP (00h)

This command always fails with the Drive returning command aborted. Table 26 defines the Byte sequence of the NOP command.

Table 26: NOP

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|----|----|---|----|---|---|---|
| COMMAND | 00h | | | | | | | |
| DRIVE/HEAD | nu | nu | nu | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

6.12 Read Buffer (E4h)

The Read Buffer command enables the host to read the current contents of the Drive's sector buffer. This command has the same protocol as the Read Sector(s) command. Table 27 defines the Read Buffer command Byte sequence.

Table 27: Read buffer

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|----|----|---|----|---|---|---|
| COMMAND | E4h | | | | | | | |
| DRIVE/HEAD | nu | nu | nu | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

6.13 Read DMA (C8h)

This command uses DMA mode to read from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the Drive sets BSY, puts all or part of the sector of data in the buffer. The Drive is then permitted, although not required, to set DRQ, clear BSY. The Drive asserts DMAREQ while data is available to be transferred. The host then reads the (512 * sector-count) bytes of data from the Drive using DMA. While DMAREQ is asserted by the Drive, the Host asserts -DMACK while it is ready to transfer data by DMA and asserts -IORD once for each 16 bit word to be transferred to the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The amount of data transferred is indeterminate.

Table 28: Read DMA

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|--------------------------|---|---|---|------------------|---|---|---|
| COMMAND | C8h | | | | | | | |
| DRIVE/HEAD | LBA | | | D | Head (LBA 27:24) | | | |
| CYLINDER HI | Cylinder High (LBA23:16) | | | | | | | |
| CYLINDER LOW | Cylinder Low (LBA15:8) | | | | | | | |
| SECTOR NUM | Sector Number (LBA7:0) | | | | | | | |
| SECTOR COUNT | Sector Count | | | | | | | |
| FEATURES | nu | | | | | | | |

6.14 Read DMA Ext (25h) 48bit LBA

This command uses DMA mode to read from 1 to 65536 sectors as specified in the Sector Count Register. A sector count of 0 requests 65536 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the CompactFlash™ Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, clear BSY. The Card asserts DMARQ while data is available to be transferred. The Card asserts DMARQ while data is available to be transferred. The

host then reads the (512 * sector-count) bytes of data from the Card using DMA. While DMARQ is asserted by the Card, the Host asserts -DMACK while it is ready to transfer data by DMA and asserts -IORD once for each 16 bit word to be transferred to the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error.

At command completion, the Command Block Registers contain the LBA of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the LBA of the sector where the error occurred. The amount of data transferred is indeterminate.

When a Read DMA Ext command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

Table 29: Read DMA Ext

| register write | previous | current | | | | | | | |
|--------------------|-------------|-------------|---|---|-------|----------|---|---|---|
| Task File Register | 15:8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMMAND | - | 25h | | | | | | | |
| DRIVE/HEAD | - | 1 | 1 | 1 | Drive | Reserved | | | |
| LBA High | LBA (47:40) | LBA (23:16) | | | | | | | |
| LBA Mid | LBA (39:32) | LBA (15:8) | | | | | | | |
| LBA Low | LBA (31:24) | LBA (7:0) | | | | | | | |
| SECTOR COUNT | 15:8 | 7:0 | | | | | | | |
| FEATURES | nu | nu | | | | | | | |

6.15 Read FPDMA Queued (60h) (if NCQ feature set supported)

This command is mandatory for devices implementing the NCQ feature set (see feature set reference).

This command requests that data to be transferred from the device to the host.

When the Forced Unit Access (FUA) bit is set to one the device shall retrieve the data from the card regardless of whether the device holds the requested information in its volatile cache. If the device holds a modified copy of the requested data as a result of having volatile cached writes, the modified data shall be written to the non-volatile media before being retrieved from the non-volatile media as part of this operation. When the FUA bit is cleared to zero the data shall be retrieved either from the device's non-volatile media or cache.

Table 30: Read FPDMA queued

| Task File Register | 15:8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|--------------------|--|----------|---|----|---|----|---|----|---|--|
| COMMAND | - | 61h | | | | | | | | |
| DRIVE/HEAD | - | FUA | 1 | nu | 0 | nu | | | | |
| CYLINDER HI | LBA (47:40) | LBA23:16 | | | | | | | | |
| CYLINDER LOW | LBA (39:32) | LBA15:8 | | | | | | | | |
| SECTOR NUM | LBA (31:24) | LBA7:0 | | | | | | | | |
| SECTOR COUNT | nu | NCQ Tag | | | | | | nu | | |
| FEATURES | The number of logical sectors to be transferred. A value of 0000h indicates that 65,536 logical sectors are to be transferred. | | | | | | | | | |

For further details see the ATA8 specification.

6.16 Read Multiple (C4h)

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

$$n = (\text{sector count}) \text{ module } (\text{block count}).$$

If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands is disabled, the Read Multiple operation is rejected with an Aborted Command error.

Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data are pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.

Table 31 defines the Read Multiple command Byte sequence.

Table 31: Read Multiple

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|--------------------------|-----|---|---|------------------|---|---|---|
| COMMAND | C4h | | | | | | | |
| DRIVE/HEAD | 1 | LBA | 1 | D | Head (LBA 27:24) | | | |
| CYLINDER HI | Cylinder High (LBA23:16) | | | | | | | |
| CYLINDER LOW | Cylinder Low (LBA15:8) | | | | | | | |
| SECTOR NUM | Sector Number (LBA7:0) | | | | | | | |
| SECTOR COUNT | Sector Count | | | | | | | |
| FEATURES | nu | | | | | | | |

6.17 Read Multiple Ext (29h) 48bit LBA

The Read Multiple Ext command performs similarly to the Read Sectors Ext command. Interrupts are not generated on every sector, but on the transfer of a block, which contains the number of sectors defined by a Set Multiple command.

Command execution is identical to the Read Sectors Ext operation except that the number of sectors defined by a Set Multiple command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which shall be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where $n = (\text{sector count}) \bmod (\text{block count})$.

If the Read Multiple Ext command is attempted before the Set Multiple Mode command has been executed, or when Read Multiple Ext command is disabled, the Read Multiple Ext operation is rejected with an Aborted Command error. Disk errors encountered during a Read Multiple Ext command are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer shall take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 65536 sectors as specified in the Sector Count Register. A sector count of 0 requests 65536 sectors. The transfer begins at the sector specified in the Sector Number Register.

At command completion, the Command Block Registers contain the LBA of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the LBA of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block that contained the error.

Table 32: Read Multiple Ext

| register write | previous | current | | | | | | | |
|--------------------|-------------|-------------|---|---|-------|----------|---|---|---|
| Task File Register | 15:8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMMAND | - | 29h | | | | | | | |
| DRIVE/HEAD | - | 1 | 1 | 1 | Drive | Reserved | | | |
| LBA High | LBA (47:40) | LBA (23:16) | | | | | | | |
| LBA Mid | LBA (39:32) | LBA (15:8) | | | | | | | |
| LBA Low | LBA (31:24) | LBA (7:0) | | | | | | | |
| SECTOR COUNT | 15:8 | 7:0 | | | | | | | |
| FEATURES | nu | nu | | | | | | | |

Note: This specification requires that CompactFlash™ Cards support a multiple block count of 1 and permits larger values to be supported.

6.18 Read Native max address (F8h)

The Read Native max address command reads the max native address of the drive. It is related to the Host protected Area feature set. Table 33 defines the Read max native address command Byte sequence.

Table 33: Read native max address

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|-----|----|---|----|---|---|---|
| COMMAND | F8h | | | | | | | |
| DRIVE/HEAD | nu | LBA | nu | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

The LBA bit shall be set to one to specify the address is an LBA. DEV shall specify the selected device. The native drive size is given in Drive/Head, Cyl Hi, Cyl Low and Sector num register as LBA value.

6.19 Read Native max address Ext (27h)

The Read Native max address Ext command reads the max native address of the drive. It is related to the Host protected Area feature set and 48-bit address feature set. Table 34 defines the Read max native address command Byte sequence.

Table 34: Read native max address

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|-----|----|---|----|---|---|---|
| COMMAND | 27h | | | | | | | |
| DRIVE/HEAD | nu | LBA | nu | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

The LBA bit shall be set to one to specify the address is an LBA. DEV shall specify the selected device. The native drive size is given in 16bit LBA High, Mid and Low register as 48bit LBA value.

To read out the higher and lower byte of the 16bit registers bit7 of the Device Control Register (HOB=High Order Bit, write to Alternate status register) must be set to 1 or 0, respectively.

Table 35: Readout native max address Ext in 48bit mode

| register read | HOB=1 | HOB=0 | | | | | | | |
|--------------------|-------------|-------------|------|----|-------|----------|----|----|-----|
| Task File Register | 15:8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STATUS | as HOB=0 | BSY | DRDR | DF | nu | DRQ | nu | nu | ERR |
| DRIVE/HEAD | as HOB=0 | 1 | 1 | 1 | Drive | Reserved | | | |
| LBA High | LBA (47:40) | LBA (23:16) | | | | | | | |
| LBA Mid | LBA (39:32) | LBA (15:8) | | | | | | | |
| LBA Low | LBA (31:24) | LBA (7:0) | | | | | | | |
| SECTOR COUNT | nu | nu | | | | | | | |
| FEATURES | nu | nu | | | | | | | |

6.20 Read Sector(s) (20h)

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the Drive sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 Bytes of data from the buffer.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data are pending in the sector buffer. Table 36 defines the Read Sector command Byte sequence.

Table 36: Read sector(s)

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|--------------------------|-----|---|---|------------------|---|---|---|
| COMMAND | 20h | | | | | | | |
| DRIVE/HEAD | 1 | LBA | 1 | D | Head (LBA 27:24) | | | |
| CYLINDER HI | Cylinder High (LBA23:16) | | | | | | | |
| CYLINDER LOW | Cylinder Low (LBA15:8) | | | | | | | |
| SECTOR NUM | Sector Number (LBA7:0) | | | | | | | |
| SECTOR COUNT | Sector Count | | | | | | | |
| FEATURES | nu | | | | | | | |

6.21 Read Sectors Ext (24h) 48bit LBA

This command reads from 1 to 65536 sectors as specified in the Sector Count Register. A sector count of 0 requests 65536 sectors. The transfer begins at the specified LBA. When this command is issued and after each sector of data (except the last one) has been read by the host, the CompactFlash™ Storage Card sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

At command completion, the Command Block Registers contain the LBA of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the LBA of the sector where the error occurred. The flawed data is pending in the sector buffer.

Table 37: Read Multiple Ext

| register write | previous | current | | | | | | | |
|--------------------|-------------|-------------|---|---|-------|----------|---|---|---|
| Task File Register | 15:8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMMAND | - | 24h | | | | | | | |
| DRIVE/HEAD | - | 1 | 1 | 1 | Drive | Reserved | | | |
| LBA High | LBA (47:40) | LBA (23:16) | | | | | | | |
| LBA Mid | LBA (39:32) | LBA (15:8) | | | | | | | |
| LBA Low | LBA (31:24) | LBA (7:0) | | | | | | | |
| SECTOR COUNT | 15:8 | 7:0 | | | | | | | |
| FEATURES | nu | nu | | | | | | | |

6.22 Read Verify Sector(s) (40h or 41h)

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the Drive sets BSY. When the requested sectors have been verified, the Drive clears BSY and generates an interrupt.

If an error occurs, the verify terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

Table 38 defines the Read Verify Sector command Byte sequence.

Table 38: Read Verify Sector(s)

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|--------------------------|-----|---|---|------------------|---|---|---|
| COMMAND | 40h or 41h | | | | | | | |
| DRIVE/HEAD | 1 | LBA | 1 | D | Head (LBA 27:24) | | | |
| CYLINDER HI | Cylinder High (LBA23:16) | | | | | | | |
| CYLINDER LOW | Cylinder Low (LBA15:8) | | | | | | | |
| SECTOR NUM | Sector Number (LBA7:0) | | | | | | | |
| SECTOR COUNT | Sector Count | | | | | | | |
| FEATURES | nu | | | | | | | |

6.23 Read Verify Ext (42h) 48bit LBA

This command is identical to the Read Sector(s) Ext command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the CompactFlash™ Storage Card sets BSY. When the requested sectors have been verified, the CompactFlash™ Storage Card clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the LBA of the last sector verified. If an error occurs, the Read Verify Command terminates at the sector where the error occurs. The Command Block Registers contain the LBA of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

Table 39: Read Multiple Ext

| register write | previous | current | | | | | | | |
|--------------------|-------------|-------------|---|---|-------|----------|---|---|---|
| Task File Register | 15:8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMMAND | - | 42h | | | | | | | |
| DRIVE/HEAD | - | 1 | 1 | 1 | Drive | Reserved | | | |
| LBA High | LBA (47:40) | LBA (23:16) | | | | | | | |
| LBA Mid | LBA (39:32) | LBA (15:8) | | | | | | | |
| LBA Low | LBA (31:24) | LBA (7:0) | | | | | | | |
| SECTOR COUNT | 15:8 | 7:0 | | | | | | | |
| FEATURES | nu | nu | | | | | | | |

6.24 Recalibrate (1Xh)

This command is effectively a NOP command to the Card and is provided for compatibility purposes. Table 40 defines the Recalibrate command Byte sequence.

Table 40: Recalibrate

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|-----|---|---|----|---|---|---|
| COMMAND | 1Xh | | | | | | | |
| DRIVE/HEAD | 1 | LBA | 1 | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

6.25 Security Disable Password (F6h)

This command requests a transfer of a single sector of data from the host. Table 41 defines the content of this sector of information. If the password selected by word 0 matches the password previously saved by the device, the device disables the lock mode. This command does not change the Master password that may be reactivated later by setting a User password.

Table 41: Security Disable Password

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|-----|---|---|----|---|---|---|
| COMMAND | F6h | | | | | | | |
| DRIVE/HEAD | 1 | LBA | 1 | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

Table 42: Security Password Data Content

| Word | Content |
|--------|---|
| 0 | Control word Bit 0: identifier 0=compare User password 1=compare Master password Bit 1-15: Reserved |
| 1-16 | Password (32 bytes) |
| 17-255 | Reserved |

6.26 Security Erase Prepare (F3h)

This command shall be issued immediately before the Security Erase Unit command to enable device erasing and unlocking. This command prevents accidental erase of the CFAST card.

Table 43: Security Erase Prepare

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|-----|---|---|----|---|---|---|
| COMMAND | F3h | | | | | | | |
| DRIVE/HEAD | 1 | LBA | 1 | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

6.27 Security Erase Unit (F4h)

This command requests transfer of a single sector of data from the host. Table 42 defines the content of this sector of information. If the password does not match the password previously saved by the CFAST card, the CFAST card rejects the command with command aborted. The Security Erase Prepare command shall be completed immediately prior to the Security Erase Unit command. If the CFAST Card receives a Security Erase Unit command without an immediately prior Security Erase Prepare command, the CFAST card aborts the Security Erase Unit command.

Table 44: Security Erase Unit

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|-----|---|---|----|---|---|---|
| COMMAND | F4h | | | | | | | |
| DRIVE/HEAD | 1 | LBA | 1 | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

6.28 Security Freeze Lock (F5h)

The Security Freeze Lock command sets the CFAST card to Frozen mode. After command completion, any other commands that update the CFAST card Lock mode are rejected. Frozen mode is disabled by power off or hardware reset. If Security Freeze Lock is issued when the CFAST card is in Frozen mode, the command executes and the CFAST card remains in Frozen mode. After command completion, the Sector Count Register shall be set to 0.

Commands disabled by Security Freeze Lock are:

- Security Set Password
- Security Unlock
- Security Disable Password
- Security Erase Unit

If security mode feature set is not supported, this command shall be handled as Wear Level command.

Table 45: Security Freeze Lock

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|-----|---|---|----|---|---|---|
| COMMAND | F5h | | | | | | | |
| DRIVE/HEAD | 1 | LBA | 1 | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

6.29 Security Set Password (F1h)

This command requests a transfer of a single sector of data from the host. Table 47 defines the content of the sector of information. The data transferred controls the function of this command.

Table 48 defines the interaction of the identifier and security level bits.

Table 46: Security Set Password

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|-----|---|---|----|---|---|---|
| COMMAND | F1h | | | | | | | |
| DRIVE/HEAD | 1 | LBA | 1 | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

Table 47: Security Set Password Data Content

| Word | Content |
|--------|---|
| 0 | Control word Bit 0: identifier 0=set User password 1=set Master password Bit 1-7: Reserved Bit 8: Security level 0=High 1=Maximum Bits 9-15: Reserved |
| 1-16 | Password (32 bytes) |
| 17-255 | Reserved |

Table 48: Identifier and Security Level Bit Interaction

| Identifier | Level | Command result |
|------------|-----------------|---|
| User | High | The password supplied with the command shall be saved as the new User password. The lock mode shall be enabled from the next power-on or hardware reset. The CFAST card shall then be unlocked by either the User password or the previously set Master password. |
| User | Maximum | The password supplied with the command shall be saved as the new User password. The lock mode shall be enabled from the next power-on or hardware reset. The CFAST card shall then be unlocked by only the User password. The Master password previously set is still stored in the CFAST card shall not be used to unlock the CFAST card. |
| Master | High or Maximum | This combination shall set a Master password but shall not enable or disable the Lock mode. The security level is not changed. |

6.30 Security Unlock (F2h)

This command requests transfer of a single sector of data from the host. Table 42 defines the content of this sector of information. If the identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in the maximum security level, then the unlock command shall be rejected. If the identifier bit is set to user, then the device compares the supplied password with the stored User password. If the password compare fails then the device returns command aborted to the host and decrements the unlock counter. This counter is initially set to five and is decremented for each password mismatch when Security Unlock is issued and the device is locked. Once this

counter reaches zero, the Security Unlock and Security Erase Unit commands are command aborted until after a power-on reset or a hardware reset is received. Security Unlock commands issued when the device is unlocked have no effect on the unlock counter.

Table 49: Security Unlock

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|-----|---|---|----|---|---|---|
| COMMAND | F2h | | | | | | | |
| DRIVE/HEAD | 1 | LBA | 1 | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

6.31 Seek (7Xh)

This command is effectively a NOP command to the Drive although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range. Table 50 shows the Seek command Byte sequence.

Table 50: Seek

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|--------------------------|-----|---|---|------------------|---|---|---|
| COMMAND | 7Xh | | | | | | | |
| DRIVE/HEAD | 1 | LBA | 1 | D | Head (LBA 27:24) | | | |
| CYLINDER HI | Cylinder High (LBA23:16) | | | | | | | |
| CYLINDER LOW | Cylinder Low (LBA15:8) | | | | | | | |
| SECTOR NUM | nu (LBA7:0) | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

6.32 Set Features (EFh)

This command is used by the host to establish or select certain features. If any subcommand input value is not supported or is invalid, the CFAST card returns command aborted.

Table 51: Set Features

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|---------|---|---|---|----|---|---|---|
| COMMAND | EFh | | | | | | | |
| DRIVE/HEAD | nu | | | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | Config | | | | | | | |
| FEATURES | Feature | | | | | | | |

Table 52: Features Supported

| Feature | Operation |
|---------|---|
| 01h/81h | Enable/Disable 8-bit data transfers. |
| 02h/82h | Enable/Disable write cache. |
| 03h | Set transfer mode based on value in Sector Count register. |
| 05h/85h | Enable/Disable advance power management. |
| 09h/89h | Enable/Disable extended power operations. |
| 0Ah/8Ah | Enable/Disable power level 1 commands. |
| 55h/AAh | Disable/Enable Read Look Ahead. |
| 66h/CCh | Disable/Enable Power On Reset (POR) established of defaults at Soft Reset. |
| 69h | NOP Accepted for backward compatibility. |
| 96h | NOP Accepted for backward compatibility. |
| 97h | Accepted for backward compatibility. Use of this Feature is not recommended. |
| 9Ah | Set the host current source capability. Allows trade-off between current drawn and read/write speed. |
| BBh | 4 bytes of data apply on Read/Write Long commands |

Features 01h and 81h are used to enable and clear 8 bit data transfer modes in True IDE Mode. If the 01h feature command is issued all data transfers shall occur on the low order D[7:0] data bus and the -IOIS16 signal shall not be asserted for data register accesses. The host shall not enable this feature for DMA transfers. Features 02h and 82h allow the host to enable or disable write cache in CFAST card that implement write cache. When the subcommand disable write cache is issued, the CFAST card shall initiate the sequence to flush cache to non-volatile memory before command completion. Feature 03h allows the host to select the PIO or Multiword DMA transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode shall be selected at all times. For Cards which support DMA, one DMA mode shall be selected at all times. The host may change the selected modes by the Set Features command.

Table 53: Transfer Mode Values

| Mode | Bits (7:3) | Bits (2:0) |
|---------------------------------|------------|---------------------|
| PIO default mode | 00000b | 000b |
| PIO default mode, disable IORDY | 00000b | 001b |
| PIO flow control transfer mode | 00001b | Mode ⁽¹⁾ |
| Reserved | 00010b | N/A |
| Multi-Word DMA mode | 00100b | Mode ⁽¹⁾ |
| Ultra DMA mode | 01000b | Mode ⁽¹⁾ |
| Reserved | 1000b | N/A |

(1)Mode = transfer mode number

Notes: Multiword DMA is not permitted for devices configured in the PC Card Memory or the PC Card I/O interface mode.

If a CFAST card supports PIO modes greater than 0 and receives a Set Features command with a Set Transfer Mode parameter and a Sector Count register value of "0000000b", it shall set its default PIO mode. If the value is "0000001b" and the CFAST card supports disabling of IORDY, then the CFAST card shall set its default PIO mode and disable IORDY. A CFAST card shall support all PIO modes below the highest mode supported, e.g., if PIO mode is supported PIO mode 0 shall be supported.

Support of IORDY is mandatory when PIO mode 3 or above is the current mode of operation.

A CFAST card reporting support for Multiword DMA modes shall support all Multiword DMA modes below the highest mode supported. For example, if Multiword DMA mode 2 support is reported, then modes 1 and 0 shall also be supported. Note that Multiword DMA shall not be supported while PC Card interface modes are selected. A CFAST card reporting support for Ultra DMA modes shall support all Ultra DMA modes below the highest mode supported. For example, if Ultra DMA mode 2 support is reported then modes 1 and 0 shall also be supported. If an Ultra DMA mode is enabled, any previously enabled Multiword DMA mode shall be disabled by the device. If a Multiword DMA mode is enabled any previously enabled Ultra DMA mode shall be disabled by the device.

Feature 05h allows the host to enable Advanced Power Management. To enable Advanced Power Management, the host writes the Sector Count register with the desired advanced power management level and then executes a Set Features command with subcommand code 05h. The power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of FEh.

Table 54 shows these values.

Table 54: Advanced power management levels

| Level | Sector Count Value |
|--|--------------------|
| Maximum performance | FEh |
| Intermediate power management levels without Standby | 81h-FDh |
| Minimum power consumption without Standby | 80h |
| Intermediate power management levels with Standby | 02h-7Fh |
| Minimum power consumption with Standby | 01h |
| Reserved | FFh |
| Reserved | 00h |

In the current version the advanced power management levels are accepted, but don't influence performance and power consumption.

Device performance may increase with increasing power management levels. Device power consumption may increase with increasing power management levels. The power management levels may contain discrete bands. For example, a device may implement one power management method from 80h to A0h and a higher

performance, higher power consumption method from level A1h to FEh. Advanced power management levels 80h and higher do not permit the device to spin down to save power. Feature 85h disables Advanced Power Management. Subcommand 85h may not be implemented on all devices that implement Set Features subcommand 05h.

Features 0Ah and 8Ah are used to enable and disable Power Level 1 commands. Feature 0Ah is the default feature for the CFAST card with extended power as they require Power Level 1 to perform their full set of functions.

Power Enhanced CFAST cards are required to power up and execute all supported commands and protocols in Power Level 0, their default feature shall be 8Ah: Disable Power Level 1 Commands. No commands are actually excluded for such cards in Power Level 0 because no commands require Power Level 1. Features 55h and BBh are the default features for the CFAST card; thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons.

Feature code 9Ah enables the host to configure the card to best meet the host system's power requirements. The host sets a value in the Sector Count register that is equal to one-fourth of the desired maximum average current (in mA) that the card should consume. For example, if the Sector Count register were set to 6, the card would be configured to provide the best possible performance without exceeding 24 mA. Upon completion of the command, the card responds to the host with the range of values supported by the card. The minimum value is set in the Cylinder Low register, and the maximum value is set in the Cylinder Hi register. The default value, after a power on reset, is to operate at the highest performance and therefore the highest current mode. The card shall accept values outside this programmable range, but shall operate at either the lowest power or highest performance as appropriate.

Features 66h and CCh can be used to enable and disable whether the Power On Reset (POR) Defaults shall be set when a soft reset occurs. The default setting is to revert to the POR defaults when a soft reset occurs.

6.33 Set max address (F9h)

The Set max address command sets the max address of the drive. It is related to the Host protected Area feature set. Table 55 defines the Set max address command Byte sequence.

Table 55: Read native max address

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|---------------------|-----|----|---|---------------------|---|---|----|
| COMMAND | F9h | | | | | | | |
| DRIVE/HEAD | nu | LBA | nu | D | Set max LBA (27:24) | | | |
| CYLINDER HI | Set max LBA (23:16) | | | | | | | |
| CYLINDER LOW | Set max LBA (15:8) | | | | | | | |
| SECTOR NUM | Set max LBA (7:0) | | | | | | | |
| SECTOR COUNT | nu | | | | | | | VV |
| FEATURES | Feature | | | | | | | |

The LBA bit shall be set to one to specify the address is an LBA. DEV shall specify the selected device.

Prerequisites

DRDY set to one. A successful READ NATIVE MAX ADDRESS command shall immediately precede a SET MAX ADDRESS command.

VV =Value volatile. If bit 0 is set to one, the device shall preserve the maximum values over power-up or hardware reset. If bit 0 is cleared to zero, the device shall revert to the most recent nonvolatile maximum address value setting over power-up or hardware reset.

The set max address can be locked/unlocked and secured by password with following features:

Table 56: Set max features

| Feature register | Command |
|------------------|----------------------|
| 00h | Obsolete |
| 01h | SET MAX SET PASSWORD |
| 02h | SET MAX LOCK |
| 03h | SET MAX UNLOCK |
| 04h | SET MAX FREEZE LOCK |
| 05-FFh | Reserved |

Typical use of the Set max address (F9h) and Read native max address (F8h) commands would be:

On reset

BIOS receives control after a system reset;

1. BIOS issues a READ NATIVE MAX ADDRESS command to find the max capacity of the device;
2. BIOS issues a SET MAX ADDRESS command to the values returned by READ NATIVE MAX ADDRESS;
3. BIOS reads configuration data from the highest area on the disk;
4. BIOS issues a READ NATIVE MAX ADDRESS command followed by a SET MAX ADDRESS command to reset the device to the size of the file system.

On save to disk

1. BIOS receives control prior to shut down;
2. BIOS issues a READ NATIVE MAX ADDRESS command to find the max capacity of the device;
3. BIOS issues a volatile SET MAX ADDRESS command to the values returned by READ NATIVE MAX ADDRESS;
4. Memory is copied to the reserved area;
5. Shut down completes;
6. On power-on or hardware reset the device max address returns to the last non-volatile setting.

These commands are intended for use only by system BIOS or other low-level boot time process. Using these commands outside BIOS controlled boot or shutdown may result in damage to file systems on the device. Devices should return command aborted if a subsequent non-volatile SET MAX ADDRESS command is received after a power-on or hardware reset.

6.34 Set max address Ext (37h) 48bit LBA

The Set Max Address Ext command sets the max address of the drive in 48bit LBA mode. It is related to the Host protected Area feature set and 48bit feature set. Table 55 defines the Set max address command Byte sequence.

Table 57: Read native max address

| register write | previous | current | | | | | | | |
|--------------------|-------------|-------------|---|---|-------|----------|---|---|---|
| Task File Register | 15:8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMMAND | - | 37h | | | | | | | |
| DRIVE/HEAD | - | 1 | 1 | 1 | Drive | Reserved | | | |
| LBA High | LBA (47:40) | LBA (23:16) | | | | | | | |
| LBA Mid | LBA (39:32) | LBA (15:8) | | | | | | | |
| LBA Low | LBA (31:24) | LBA (7:0) | | | | | | | |
| SECTOR COUNT | nu | nu | | | | | | | W |
| FEATURES | nu | nu | | | | | | | |

The LBA bit shall be set to one to specify the address is an LBA. DEV shall specify the selected device.

Prerequisites

DRDY set to one. A successful READ NATIVE MAX ADDRESS command shall immediately precede a SET MAX ADDRESS command.

WV=Value volatile. If bit 0 is set to one, the device shall preserve the maximum values over power-up or hardware reset. If bit 0 is cleared to zero, the device shall revert to the most recent nonvolatile maximum address value setting over power-up or hardware reset.

The output is the same as for Readout Native max address Ext (see Table 35).

6.35 Set Multiple Mode (C6h)

This command enables the Drive to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the Drive sets BSY and checks the Sector Count Register.

If the Sector Count Register contains a valid value and the block count is supported, the value is loaded for all subsequent Read Multiple and Write Multiple commands and execution is enabled. If a block count is not supported, an Aborted Command error is posted, and Read Multiple and Write Multiple commands are disabled. If the Sector Count Register contains '0' when the command is issued, Read and Write Multiple commands are disabled. At power on the default mode is Read and Write Multiple disabled, unless it is disabled by a Set Feature command. Table 58 defines the Set Multiple Mode command Byte sequence.

Table 58: Set Multiple Mode

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|--------------|---|---|---|----|---|---|---|
| COMMAND | C6h | | | | | | | |
| DRIVE/HEAD | nu | | | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | Sector Count | | | | | | | |
| FEATURES | nu | | | | | | | |

6.36 Set Sleep Mode (E6h or 99h)

This command causes the Drive to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command. Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 5 milliseconds. Note that this time base (5ms) is different from the ATA Specification. Table 59 defines the Set Sleep Mode command Byte sequence.

Table 59: Set Sleep Mode

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|------------|---|---|---|----|---|---|---|
| COMMAND | E6h or 99h | | | | | | | |
| DRIVE/HEAD | nu | | | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

6.37 S.M.A.R.T. (Boh)

The intent of self-monitoring, analysis, and reporting technology (the SMART feature set) is to protect user data and minimize the likelihood of unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, SMART feature set devices attempt to predict the likelihood of near-term degradation or fault condition. Providing the host system the knowledge of a negative reliability condition allows the host system to warn the user of the impending risk of a data loss and advise the user of appropriate action. Support of this feature set is indicated in the IDENTIFY DEVICE data (Word 82 bit 0).

Table 60: S.M.A.R.T. Features

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|---------|---|---|---|----|---|---|---|
| COMMAND | Boh | | | | | | | |
| DRIVE/HEAD | 1 | 1 | 1 | D | nu | | | |
| CYLINDER HI | C2h | | | | | | | |
| CYLINDER LOW | 4Fh | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | XXh | | | | | | | |
| FEATURES | Feature | | | | | | | |

Details of S.M.A.R.T. features are described in Section 7.

6.38 Standby (96h or E2)

This command causes the Drive to set BSY, enter the Sleep mode (which corresponds to the ATA 'Standby' Mode), clear BSY and return the interrupt immediately. Recovery from Sleep mode is accomplished by issuing another command. Table 61 defines the Standby command Byte sequence.

Table 61: Standby

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|------------|---|---|---|----|---|---|---|
| COMMAND | 96h or E2h | | | | | | | |
| DRIVE/HEAD | nu | | | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |

| | |
|--------------|----|
| CYLINDER LOW | nu |
| SECTOR NUM | nu |
| SECTOR COUNT | nu |
| FEATURES | nu |

6.39 Standby Immediate (94h or Eoh)

This command causes the Drive to set BSY, enter the Sleep mode (which corresponds to the ATA Standby Mode), clear BSY and return the interrupt immediately. Recovery from Sleep mode is accomplished by issuing another command. Table 62 defines the Standby Immediate Byte sequence.

Table 62: Standby Immediate

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|------------|---|---|---|----|---|---|---|
| COMMAND | 94h or Eoh | | | | | | | |
| DRIVE/HEAD | nu | | | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

6.40 Translate Sector (87h)

This command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with a 'ooh' indicating Translate Sector is not needed. Table 63 defines the Translate Sector command Byte sequence.

Table 63: Translate Sector

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|--------------------------|-----|---|---|------------------|---|---|---|
| COMMAND | 87h | | | | | | | |
| DRIVE/HEAD | 1 | LBA | 1 | D | Head (LBA 27:24) | | | |
| CYLINDER HI | Cylinder High (LBA23:16) | | | | | | | |
| CYLINDER LOW | Cylinder Low (LBA15:8) | | | | | | | |
| SECTOR NUM | nu (LBA7:0) | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

6.41 Write Buffer (E8h)

The Write Buffer command enables the host to overwrite contents of the Drive's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 Bytes. Table 64 defines the Write Buffer command Byte sequence.

Table 64: Write Buffer

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|---|---|---|----|---|---|---|
| COMMAND | E8h | | | | | | | |
| DRIVE/HEAD | nu | | | D | nu | | | |
| CYLINDER HI | nu | | | | | | | |
| CYLINDER LOW | nu | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | nu | | | | | | | |

6.42 Write DMA (CAh, CBh)

This command uses DMA mode to write from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the Drive sets BSY, puts all or part of the sector of data in the buffer. The Drive is then permitted, although not required, to set DRQ, clear BSY. The Drive asserts DMAREQ while data is available to be transferred. The host then writes the (512 * sector-count) bytes of data to the Drive using DMA. While DMAREQ is

asserted by the Drive, the Host asserts -DMACK while it is ready to transfer data by DMA and asserts -IOWR once for each 16 bit word to be transferred from the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector written. If an error occurs, the write terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The amount of data transferred is indeterminate.

When a Write DMA command is received by the Drive and 8 bit transfer mode has been enabled by the Set Features command, the Drive shall return the Aborted error.

Table 65: Write DMA

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|--------------------------|---|---|---|------------------|---|---|---|
| COMMAND | CAh or CBh | | | | | | | |
| DRIVE/HEAD | LBA | | | D | Head (LBA 27:24) | | | |
| CYLINDER HI | Cylinder High (LBA23:16) | | | | | | | |
| CYLINDER LOW | Cylinder Low (LBA15:8) | | | | | | | |
| SECTOR NUM | Sector number (LBA7:0) | | | | | | | |
| SECTOR COUNT | Sector Count | | | | | | | |
| FEATURES | nu | | | | | | | |

6.43 Write DMA Ext (35h) 48bit LBA

This command uses DMA mode to write from 1 to 65536 sectors as specified in the Sector Count Register. A sector count of 0 requests 65536 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the CompactFlash™ Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, clear BSY. The Card asserts DMARQ while data is available to be transferred. The host then writes the (512 * sector-count) bytes of data to the Card using the DMA protocol. While DMARQ is asserted by the Card, the Host asserts -DMACK while it is ready to transfer data by DMA and asserts -IOWR once for each 16 bit word to be transferred from the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error.

At command completion, the Command Block Registers contain the LBA of the last sector written. If an error occurs, the write terminates at the sector where the error occurred. The Command Block Registers contain the LBA of the sector where the error occurred. The amount of data transferred is indeterminate.

When a Write DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

Table 66: Write DMA Ext

| register write | previous | current | | | | | | | |
|--------------------|-------------|-------------|---|---|-------|----------|---|---|---|
| Task File Register | 15:8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMMAND | - | 35h | | | | | | | |
| DRIVE/HEAD | - | 1 | 1 | 1 | Drive | Reserved | | | |
| LBA High | LBA (47:40) | LBA (23:16) | | | | | | | |
| LBA Mid | LBA (39:32) | LBA (15:8) | | | | | | | |
| LBA Low | LBA (31:24) | LBA (7:0) | | | | | | | |
| SECTOR COUNT | 15:8 | 7:0 | | | | | | | |
| FEATURES | nu | nu | | | | | | | |

6.44 Write FPDMA Queued (61h) (if NCQ feature set supported)

This command is mandatory for devices implementing the NCQ feature set (see feature set reference).

This command causes data to be transferred from the host to the device.

When the Forced Unit Access (FUA) bit is set to one regardless of whether volatile and/or non-volatile write caching in the device is enabled or not, the user data shall be written to non-volatile media before command completion is reported. When the FUA bit is cleared to zero the device may return command completion before the data is written to the media.

Table 67: Write FPDMA queued

| Task File Register | 15:8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|--|----------|---|----|---|----|---|----|---|
| COMMAND | - | 61h | | | | | | | |
| DRIVE/HEAD | - | FUA | 1 | nu | 0 | nu | | | |
| CYLINDER HI | LBA (47:40) | LBA23:16 | | | | | | | |
| CYLINDER LOW | LBA (39:32) | LBA15:8 | | | | | | | |
| SECTOR NUM | LBA (31:24) | LBA7:0 | | | | | | | |
| SECTOR COUNT | nu | NCQ Tag | | | | | | nu | |
| FEATURES | The number of logical sectors to be transferred. A value of 0000h indicates that 65,536 logical sectors are to be transferred. | | | | | | | | |

For further details see the ATA8 specification.

6.45 Write Multiple Command (C5h)

This command is similar to the Write Sectors command. The Drive sets BSY within 400ns of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set Multiple. Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Write Multiple command.

When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the sector/block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

$n = (\text{sector count}) \bmod (\text{block count})$.

If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write Multiple commands are disabled, the Write Multiple operation will be rejected with an aborted command error.

Errors encountered during Write Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count Register contains the residual number of sectors that need to be transferred for successful completion of the command. For example, each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count Register contains 6 and the address is that of the third sector.

Note: The current revision of the Drive only supports a block count of 1 as indicated in the Identify Drive Command information. The Write Multiple command is provided for compatibility with future products which may support a larger block count.

Table 68 defines the Write Multiple command Byte sequence.

Table 68: Write Multiple

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|--------------------------|-----|---|---|------------------|---|---|---|
| COMMAND | C5h | | | | | | | |
| DRIVE/HEAD | 1 | LBA | 1 | D | Head (LBA 27:24) | | | |
| CYLINDER HI | Cylinder High (LBA23:16) | | | | | | | |
| CYLINDER LOW | Cylinder Low (LBA15:8) | | | | | | | |
| SECTOR NUM | Sector number (LBA7:0) | | | | | | | |
| SECTOR COUNT | Sector Count | | | | | | | |
| FEATURES | nu | | | | | | | |

6.46 Write Multiple Ext (39h) 48bit LBA

The Write Multiple Ext command is similar to the Write Multiple command, except that LBA addressing is mandatory, the LBA associated with this command is a 48 bit address, and the sector count field is a 16 bit field. The second (lower in the table) part of each 16 bit field can be written to or read from by setting the HOB bit of the Device Control Register to 1 before reading or writing the field. Reading or writing the task file shall reset the HOA bit to 0.

Error handling is similar to the Write Multiple command, except that the error sector address is always returned as a 48 bit address, and the sector count is a 16 bit number.

Table 69: Write Multiple Ext

| register write | previous | current | | | | | | | |
|--------------------|-------------|-------------|---|---|-------|----------|---|---|---|
| Task File Register | 15:8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMMAND | - | 39h | | | | | | | |
| DRIVE/HEAD | - | 1 | 1 | 1 | Drive | Reserved | | | |
| LBA High | LBA (47:40) | LBA (23:16) | | | | | | | |
| LBA Mid | LBA (39:32) | LBA (15:8) | | | | | | | |
| LBA Low | LBA (31:24) | LBA (7:0) | | | | | | | |
| SECTOR COUNT | 15:8 | 7:0 | | | | | | | |
| FEATURES | nu | nu | | | | | | | |

6.47 Write Sector(s) (30h)

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the Drive sets BSY, sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated. If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector. Table 70 defines the Write Sector(s) command Byte sequence.

Table 70: Write Sector(s)

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|--------------------------|-----|---|---|------------------|---|---|---|
| COMMAND | 30h | | | | | | | |
| DRIVE/HEAD | 1 | LBA | 1 | D | Head (LBA 27:24) | | | |
| CYLINDER HI | Cylinder High (LBA23:16) | | | | | | | |
| CYLINDER LOW | Cylinder Low (LBA15:8) | | | | | | | |
| SECTOR NUM | Sector number (LBA7:0) | | | | | | | |
| SECTOR COUNT | Sector Count | | | | | | | |
| FEATURES | nu | | | | | | | |

6.48 Write Sector(s) Ext (34h) 48bit LBA

This is the 48-bit address version of the Write Sector(s) command.

This command writes from 1 to 65,536 sectors as specified in the Sector Count Register. A sector count value of 0000h requests 65,536 sectors. The device shall interrupt for each DRQ block transferred.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the 48-bit LBA of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

Table 71: Write Sector(s) Ext

| register write | previous | current | | | | | | | |
|--------------------|-------------|-------------|---|---|-------|----------|---|---|---|
| Task File Register | 15:8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMMAND | - | 34h | | | | | | | |
| DRIVE/HEAD | - | 1 | 1 | 1 | Drive | Reserved | | | |
| LBA High | LBA (47:40) | LBA (23:16) | | | | | | | |
| LBA Mid | LBA (39:32) | LBA (15:8) | | | | | | | |
| LBA Low | LBA (31:24) | LBA (7:0) | | | | | | | |
| SECTOR COUNT | 15:8 | 7:0 | | | | | | | |
| FEATURES | nu | nu | | | | | | | |

6.49 Write Verify (3Ch)

This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write Sector(s) command. Table 72 defines the Write Verify command Byte sequence.

Table 72: Write Verify

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|--------------------------|-----|---|---|------------------|---|---|---|
| COMMAND | 3Ch | | | | | | | |
| DRIVE/HEAD | 1 | LBA | 1 | D | Head (LBA 27:24) | | | |
| CYLINDER HI | Cylinder High (LBA23:16) | | | | | | | |
| CYLINDER LOW | Cylinder Low (LBA15:8) | | | | | | | |
| SECTOR NUM | Sector number (LBA7:0) | | | | | | | |
| SECTOR COUNT | Sector Count | | | | | | | |
| FEATURES | nu | | | | | | | |

7 S.M.A.R.T Functionality

The F-2x0 CF cards support the following SMART commands, determined by the Feature Register value.

Table 73: S.M.A.R.T. Features Supported

| Feature | Operation |
|---------|-----------------------------------|
| D0h | SMART Read Data |
| D1h | SMART Read Attribute Thresholds |
| D2h | SMART Enable/Disable Attribute |
| D8h | SMART Enable Operations |
| D9h | Autosave SMART Disable Operations |
| DAh | SMART Return Status |

SMART commands with Feature Register values not mentioned in the above table are not supported, and will be aborted.

7.1 S.M.A.R.T. Enable / Disable operations

This command enables / disables access to the SMART capabilities of the CF card. The state of SMART (enabled or disabled) is preserved across power cycles.

Table 74: S.M.A.R.T. Enable / Disable operations (Feature D8h / D9h)

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----------|---|---|---|----|---|---|---|
| COMMAND | Boh | | | | | | | |
| DRIVE/HEAD | 1 | 1 | 1 | D | nu | | | |
| CYLINDER HI | C2h | | | | | | | |
| CYLINDER LOW | 4Fh | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | D8h / D9h | | | | | | | |

7.2 S.M.A.R.T. Enable / Disable Attribute Autosave

This command is effectively a no-operation as the data for the SMART functionality is always available and kept current in the CF card.

Table 75: S.M.A.R.T. Enable / Disable Attribute Autosave (Feature D2h)

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|------------|---|---|---|----|---|---|---|
| COMMAND | Boh | | | | | | | |
| DRIVE/HEAD | 1 | 1 | 1 | D | nu | | | |
| CYLINDER HI | C2h | | | | | | | |
| CYLINDER LOW | 4Fh | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | 00h or F1h | | | | | | | |
| FEATURES | D2h | | | | | | | |

7.3 S.M.A.R.T. Read data

This command returns one sector of SMART data.

Table 76: S.M.A.R.T. read data (Feature D0h)

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|---|---|---|----|---|---|---|
| COMMAND | Boh | | | | | | | |
| DRIVE/HEAD | 1 | 1 | 1 | D | nu | | | |
| CYLINDER HI | C2h | | | | | | | |
| CYLINDER LOW | 4Fh | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | D0h | | | | | | | |

The data structure returned is:

Table 77: S.M.A.R.T. Data Structure

| Offset | Value | Description |
|-----------|-------|---|
| 0..1 | 0010h | SMART structure version for firmware "1" |
| 2..361 | | Attribute entries 1 to 30 (12 bytes each) |
| 362 | 00h | Off-line data collection status (no off-line data collection) |
| 363 | 00h | Self-test execution status byte (self-test completed) |
| 364..365 | 0000h | Total time to complete off-line data collection |
| 366 | 00h | - |
| 367 | 00h | Off-line data collection capability (no off-line data collection) |
| 368..369 | 0003h | SMART capabilities |
| 370 | 00h | Error logging capability (no error logging) |
| 371 | 00h | - |
| 372 | 00h | Short self-test routine recommended polling time |
| 373 | 00h | Extended self-test routine recommended polling time |
| 374..385 | 00h | Reserved |
| 386..387 | 0004h | SMART Swissbit Structure Version for SMART for firmware "1" |
| 388..391 | | "Commit" counter |
| 392..395 | | Wear Level Threshold |
| 396 | | Global Bad Block Management active |
| 397 | | Global Wear Leveling active |
| 398..401 | | Average Flash Block Erase Count |
| 402..405 | | Number of Flash Blocks involved into the Wear Leveling |
| 406..409 | | Number of total ECC errors during firmware initialization |
| 410.. 413 | | Number of correctable ECC errors during firmware initialization |
| 414..510 | 00h | - |
| 511 | | Data structure checksum |

The byte order for the multi-byte values is little Endian (least significant byte first), unless specified otherwise.

There are 12 attributes that are defined in the CF card. These return their data in the attribute section of the SMART data, using a 12 byte data field.

The field at offset 386 gives a version number for the contents of the SMART data structure.

The byte at offset 396 is 0 if the bad block management is still working chip local, and 1 if the global bad block management has started. This happens when one of the flash chips runs out of spare blocks, in this case spare blocks from different flash chips are used.

The byte at offset 397 is 0 if the wear leveling has not yet started its global operation and 1 if the global wear leveling has started. This happens when the most used chip has reached the erase count threshold defined in the Erase Count Attribute.

In the following sections the Attributes for different SMART structure versions (Byte 0...1) are specified that may depend on the firmware.

7.3.1 SMART Attributes for SMART structure version 0010h

7.3.1.1 Spare Block Count Attribute

This attribute gives information about the amount of available spare blocks.

Table 78: Spare Block Count Attribute for SMART structure version 0010h

| Offset | Value | Description |
|--------|-------|--|
| 0 | c4h | Attribute ID – Reallocation Count |
| 1..2 | 0003h | Flags – Pre-fail type, value is updated during normal operation |
| 3 | | Attribute value. The value returned here is the minimum percentage of remaining spare blocks over all flash chips, i.e. min over all chips (100 × current spare blocks / initial spare blocks) |
| 4 | | Attribute value (worst value) |
| 5..7 | | sum of initial number of spare blocks for all flash chips |
| 8..10 | | sum of the current number of spare blocks for all flash chips |
| 11 | 00h | Reserved |

This attribute is used for the SMART Return Status command. If the attribute value field is less than the spare block threshold, the SMART Return Status command will indicate a threshold exceeded condition.

7.3.1.2 Spare Block Count Worst Chip Attribute Threshold

This attribute gives information about the amount of available spare blocks on the flash chip that has the lowest current number of spare blocks.

Table 79: Spare Block Count Attribute for SMART structure version 0010h

| Offset | Value | Description |
|--------|-------|---|
| 0 | D5h | Attribute ID – Reallocation Count |
| 1..2 | 0003h | Flags – Pre-fail type, value is updated during normal operation |
| 3 | 64h | Attribute value. This value is fixed at 100. |
| 4 | 64h | Attribute value (worst value) |
| 5..7 | | Initial number of spare blocks of the flash chip with the lowest current number of spare blocks |
| 8..10 | | Current number of spare blocks of the flash chip with the lowest current number of spare blocks |
| 11 | 00h | Reserved |

7.3.1.3 Erase Count Attribute

This attribute gives information about the amount of flash block erases that have been performed.

Table 80: Erase Count Attribute for SMART structure version 0010h

| Offset | Value | Description |
|--------|-------|--|
| 0 | E5h | Attribute ID – Erase Count Usage (vendor specific) |
| 1..2 | 0003h | Flags – Pre-fail type, value is updated during normal operation |
| 3 | | Attribute value. The value returned here is an estimation of the remaining card life, in percent, based on the number of flash block erases compared to the target number of erase cycles per block. |
| 4 | | Attribute value (worst value) |
| 5..10 | | Estimated total number of block erases |
| 11 | 00h | Reserved |

This attribute is used for the SMART Return Status command. If the attribute value field is less than the erase count threshold, the SMART Return Status command will indicate a threshold exceeded condition.

7.3.1.4 Total ECC Errors Attribute

This attribute gives information about the total number of ECC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Table 81: Total ECC Errors Attribute for SMART structure version 0010h

| Offset | Value | Description |
|--------|-------|---|
| 0 | CBh | Attribute ID – Number of ECC errors |
| 1..2 | 0002h | Flags – Advisory type, value is updated during normal operation |
| 3 | 64h | Attribute value. This value is fixed at 100. |
| 4 | 64h | Attribute value (worst value) |
| 5..8 | | Total number of ECC errors (correctable and uncorrectable) |
| 9..10 | | - |
| 11 | 00h | Reserved |

7.3.1.5 Correctable ECC Errors Attribute

This attribute gives information about the total number of correctable ECC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Table 82: Correctable ECC Errors Attribute for SMART structure version 0010h

| Offset | Value | Description |
|--------|-------|---|
| 0 | CCh | Attribute ID – Number of corrected ECC errors |
| 1..2 | 0002h | Flags – Advisory type, value is updated during normal operation |
| 3 | 64h | Attribute value. This value is fixed at 100. |
| 4 | 64h | Attribute value (worst value) |
| 5..8 | | Total number of correctable ECC errors |
| 9..10 | | - |
| 11 | 00h | Reserved |

7.3.1.6 UDMA CRC Errors Attribute

This attribute gives information about the total number of UDMA CRC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Table 83: UDMA CRC Errors Attribute for SMART structure version 0010h

| Offset | Value | Description |
|--------|-------|---|
| 0 | C7h | Attribute ID – UDMA CRC error rate |
| 1..2 | 0002h | Flags – Advisory type, value is updated during normal operation |
| 3 | 64h | Attribute value. This value is fixed at 100. |
| 4 | 64h | Attribute value (worst value) |
| 5..8 | | Total number of UDMA CRC errors |
| 9..10 | | - |
| 11 | 00h | Reserved |

7.3.1.7 Total Number of Reads Attribute

This attribute gives information about the total number of flash read commands. This can be useful for the interpretation of the number of correctable or total ECC errors. This attribute is not used for the SMART Return Status command.

Table 84: Total Number of Reads Attribute for SMART structure version 0010h

| Offset | Value | Description |
|--------|-------|---|
| 0 | E8h | Attribute ID – Number of Reads (vendor specific) |
| 1..2 | 0002h | Flags – Advisory type, value is updated during normal operation |
| 3 | 64h | Attribute value. This value is fixed at 100. |
| 4 | 64h | Attribute value (worst value) |
| 5..10 | | Total number of flash read commands |
| 11 | 00h | Reserved |

7.3.1.8 Power On Count Attribute

Table 85: Power On Count Attribute for SMART structure version 0010h

| Offset | Value | Description |
|--------|-------|---|
| 0 | 0Ch | Attribute ID – Power On Count |
| 1..2 | 0002h | Flags – Advisory type, value is updated during normal operation |
| 3 | 64h | Attribute value. This value is fixed at 100. |
| 4 | 64h | Attribute value (worst value) |
| 5..8 | | Number of Power On cycles |
| 9..10 | | - |
| 11 | 00h | Reserved |

7.3.1.9 Total LBAs Written Attribute

This attribute gives the total amount of data written to the disk, in units of 32MB (65536 sectors). This number can be converted to Terabytes written (TBW) by dividing the raw attribute value by 2^{31} .

Table 86: Total LBAs Written for SMART structure version 0010h

| Offset | Value | Description |
|--------|-------|---|
| 0 | F1h | Attribute ID – Total LBAs Written (vendor specific) |
| 1..2 | 0002h | Flags – Advisory type, value is updated during normal operation |
| 3 | 64h | Attribute value. This value is fixed at 100. |
| 4 | 64h | Attribute value (worst value) |
| 5..10 | | Total number of LBAs written to the disk, divided by 65536 |
| 11 | 00h | Reserved |

7.3.1.10 Total LBAs Read Attribute

This attribute gives the total amount of data read from the disk, in units of 32MB (65536 sectors). This number can be converted to Terabytes written (TBW) by dividing the raw attribute value by 2^{31} .

Table 87: Total LBAs Written for SMART structure version 0010h

| Offset | Value | Description |
|--------|-------|---|
| 0 | F2h | Attribute ID – Total LBAs Read (vendor specific) |
| 1..2 | 0002h | Flags – Advisory type, value is updated during normal operation |
| 3 | 64h | Attribute value. This value is fixed at 100. |
| 4 | 64h | Attribute value (worst value) |
| 5..10 | | Total number of LBAs read from the disk, divided by 65536 |
| 11 | 00h | Reserved |

7.3.1.11 Anchor Block Status Attribute

This attribute is a placeholder for future use in the firmware; it has no useful data yet.

Table 88: Anchor Block Status for SMART structure version 0010h

| Offset | Value | Description |
|--------|-------|---|
| 0 | D6h | Attribute ID – Anchor Block Status (vendor specific) |
| 1..2 | 0002h | Flags – Advisory type, value is updated during normal operation |
| 3 | 64h | Attribute value. This value is fixed at 100. |
| 4 | 64h | Attribute value (worst value) |
| 5..10 | | - |
| 11 | 00h | Reserved |

7.3.1.12 Trim Status Attribute

This attribute is a placeholder for future use in the firmware; it has no useful data yet.

Table 89: Trim Status for SMART structure version 0010h

| Offset | Value | Description |
|--------|-------|---|
| 0 | D7h | Attribute ID – Trim Status (vendor specific) |
| 1..2 | 0002h | Flags – Advisory type, value is updated during normal operation |
| 3 | 64h | Attribute value. This value is fixed at 100. |
| 4 | 64h | Attribute value (worst value) |
| 5..10 | | - |
| 11 | 00h | Reserved |

7.4 S.M.A.R.T. Read Attribute Thresholds

This command returns one sector of SMART attribute thresholds.

Table 90: S.M.A.R.T. read data (Feature D1h)

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|---|---|---|----|---|---|---|
| COMMAND | Boh | | | | | | | |
| DRIVE/HEAD | 1 | 1 | 1 | D | nu | | | |
| CYLINDER HI | C2h | | | | | | | |
| CYLINDER LOW | 4Fh | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | D1h | | | | | | | |

The data structure returned is:

Table 91: S.M.A.R.T. Data Structure

| Offset | Value | Description |
|----------|-------|---|
| 0..1 | 0010h | SMART structure version for Firmware "1" |
| 2..361 | | Attribute threshold entries 1 to 30 (12 bytes each) |
| 362..379 | 00h | Reserved |
| 380..510 | 00h | - |
| 511 | | Data structure checksum |

Table 92: Spare Block Count Attribute Threshold

| Offset | Value | Description |
|--------|-------|---|
| 0 | C4h | Attribute ID – Reallocation Count |
| 1 | 19h* | Spare Block Count Threshold (* typical 25%, could vary) |
| 2..11 | 00h | Reserved |

Table 93: Spare Block Count Worst Chip Attribute Threshold

| Offset | Value | Description |
|--------|-------|-----------------------------------|
| 0 | D5h | Attribute ID – Reallocation Count |
| 1 | 00h | No threshold |
| 2..11 | 00h | Reserved |

Table 94: Erase Count Attribute Threshold

| Offset | Value | Description |
|--------|-------|--|
| 0 | E5h | Attribute ID – Erase Count Usage (vendor specific) |
| 1 | 01h* | Erase Count Threshold (* typical 1%, could vary) |
| 2..11 | 00h | Reserved |

Table 95: Total ECC Errors Attribute Threshold

| Offset | Value | Description |
|--------|-------|---|
| 0 | CBh | Attribute ID – Number of ECC errors |
| 1 | 00h | No threshold for the Total ECC Errors Attribute |
| 2..11 | 00h | Reserved |

Table 96: Correctable ECC Errors Attribute Threshold

| Offset | Value | Description |
|--------|-------|---|
| 0 | CCh | Attribute ID – Number of corrected ECC errors |
| 1 | 00h | No threshold for the Correctable ECC Errors Attribute |
| 2..11 | 00h | Reserved |

Table 97: UDMA CRC Errors Attribute

| Offset | Value | Description |
|--------|-------|--|
| 0 | C7h | Attribute ID – UDMA CRC error rate |
| 1 | 00h | No threshold for the UDMA CRC Errors Attribute |
| 2..11 | 00h | Reserved |

Table 98: Total Number of Reads Attribute

| Offset | Value | Description |
|--------|-------|--|
| 0 | E8h | Attribute ID – Number of Reads (vendor specific) |
| 1 | 00h | No threshold for the Total Number of Reads Attribute |
| 2..11 | 00h | Reserved |

Table 99: Power On Count Attribute

| Offset | Value | Description |
|--------|-------|---|
| 0 | 0Ch | Attribute ID – Power On Count |
| 1 | 00h | No threshold for the Power On Count Attribute |
| 2..11 | 00h | Reserved |

Table 100: Total LBAs Written Attribute

| Offset | Value | Description |
|--------|-------|---|
| 0 | F1h | Attribute ID – Total LBAs Written (vendor specific) |
| 1 | 00h | No threshold for the Total LBAs Written Attribute |
| 2..11 | 00h | Reserved |

Table 101: Total LBAs Read Attribute

| Offset | Value | Description |
|--------|-------|--|
| 0 | F2h | Attribute ID – Total LBAs Read (vendor specific) |
| 1 | 00h | No threshold for the Total LBAs Read Attribute |
| 2..11 | 00h | Reserved |

Table 102: Anchor Block Status Attribute

| Offset | Value | Description |
|--------|-------|--|
| 0 | D6h | Attribute ID – Anchor Block Status (vendor specific) |
| 1 | 00h | No threshold for the Anchor Block Status Attribute |
| 2..11 | 00h | Reserved |

Table 103: Trim Status Attribute

| Offset | Value | Description |
|--------|-------|--|
| 0 | D7h | Attribute ID – Trim Status (vendor specific) |
| 1 | 00h | No threshold for the Trim Status Attribute |
| 2..11 | 00h | Reserved |

7.5 S.M.A.R.T. Return Status

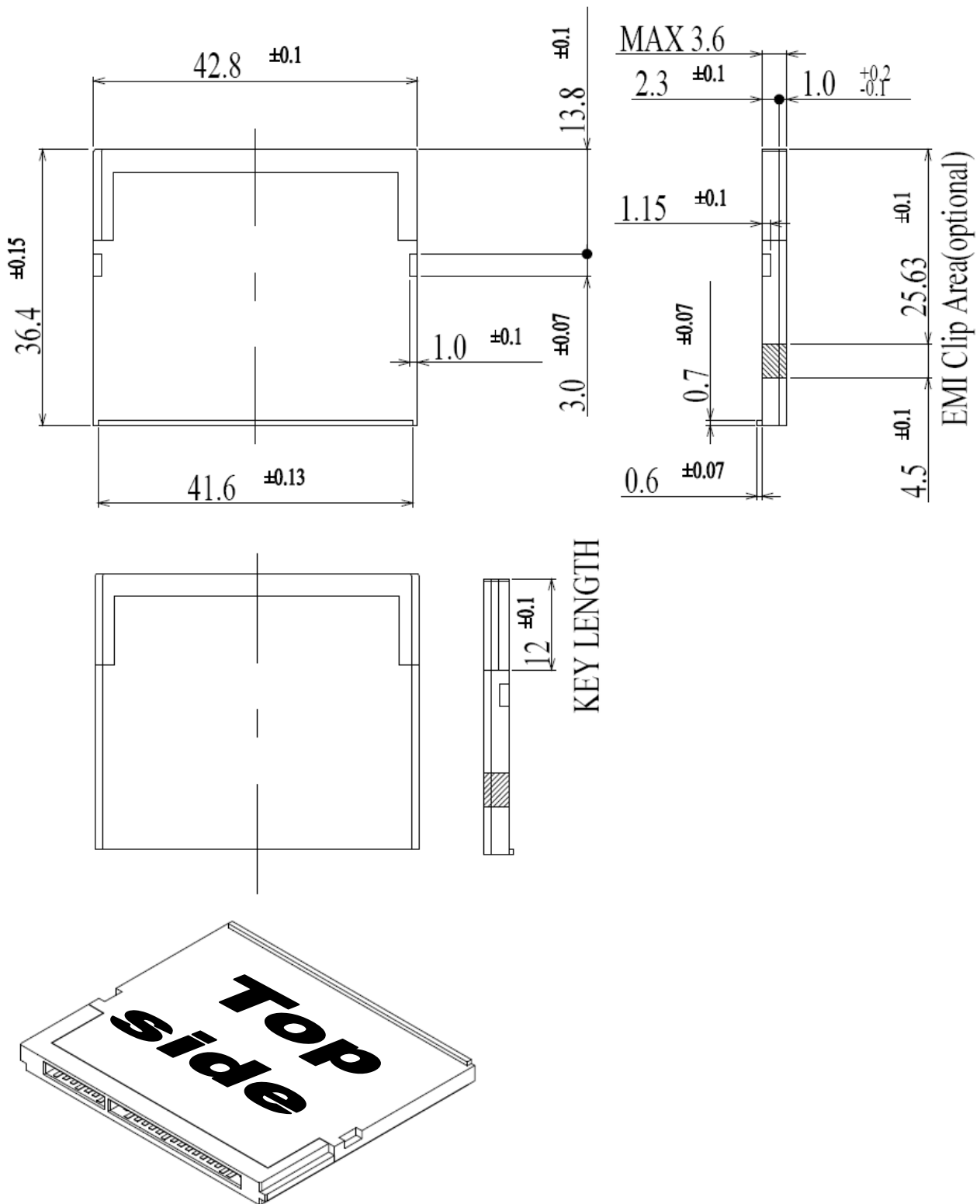
This command checks the device reliability status. If a threshold exceeded condition exists for either the Spare Block Count attribute or the Erase Count attribute, the device will set the Cylinder Low register to F4h and the Cylinder High register to 2Ch. If no threshold exceeded condition exists, the device will set the Cylinder Low register to 4Fh and the Cylinder High register to C2h.

Table 104: S.M.A.R.T. read data (Feature D1h)

| Task File Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|---|---|---|----|---|---|---|
| COMMAND | Boh | | | | | | | |
| DRIVE/HEAD | 1 | 1 | 1 | D | nu | | | |
| CYLINDER HI | C2h | | | | | | | |
| CYLINDER LOW | 4Fh | | | | | | | |
| SECTOR NUM | nu | | | | | | | |
| SECTOR COUNT | nu | | | | | | | |
| FEATURES | DAh | | | | | | | |

8 Package mechanical

Figure 6: CFAST card Dimensions



9 Declaration of Conformity

We

Manufacturer: Swissbit AG
Industriestrasse 4
CH-9552 Bronschhofen
Switzerland

declare under our sole responsibility that the product

Product Type: CFast Card / 1" SSD with sATA Interface
Brand Name: SWISSMEMORY™ CFAST™ card
Product Series: F-240
Part Number: SFCAxxxxHxBVxxx-x-xx-xxx-xxx

to which this declaration relates is in conformity with the following directives:

EN55022:2006 +A1:r B
FCC47 Part 15 Subpart B §15.111
EN 61000-4-2:2009
EN 61000-4-3:2006+A1:2008+A2:2010
EN 61000-6-2:2005
2002/96/EC Category 3 (WEEE)

following the provisions of Directive

Electromagnetic compatibility 2004/108/EC
Restriction of the use of certain hazardous substances 2011/65/EU

Swissbit AG, July 2013



Manuela Kögel
Head of Quality Management

10 RoHS and WEEE update from Swissbit

Dear Valued Customer,

We at Swissbit place great value on the environment and thus pay close attention to the diverse aspects of manufacturing environmentally and health friendly products. The European Parliament and the Council of the European Union have published two Directives defining a European standard for environmental protection. This states that Solid State Drives must comply with both Directives in order for them to be sold on the European market:

- **RoHS** – Restriction of Hazardous Substances
- **WEEE** – Waste Electrical and Electronic Equipment

Swissbit would like to take this opportunity to inform our customers about the measures we have implemented to adapt all our products to the European norms.

What is the WEEE Directive (2002/96/EC)?

The Directive covers the following points:

- Prevention of WEEE
- Recovery, recycling and other measures leading to a minimization of wastage of electronic and electrical equipment
- Improvement in the quality of environmental performance of all operators involved in the EEE life cycle, as well as measures to incorporate those involved at the EEE waste disposal points

What are the key elements?

The WEEE Directive covers the following responsibilities on the part of producers:

Producers must draft a disposal or recovery scheme to dispose of EEE correctly.
Producers must be registered as producers in the country in which they distribute the goods.
They must also supply and publish information about the EEE categories.
Producers are obliged to finance the collection, treatment and disposal of WEEE.

Inclusion of WEEE logos on devices

In reference to the Directive, the WEEE logo must be printed directly on all devices that have sufficient space.
«In exceptional cases where this is necessary because of the size of the product, the symbol of the WEEE Directive shall be printed on the packaging, on the instructions of use and on the warranty»
(WEEE Directive 2002/96/EC)

When does the WEEE Directive take effect?

The Directive came into effect internationally on 13 August, 2005.

What is RoHS (2002/95/EC)?

The goals of the Directive are to:

- Place less of a burden on human health and to protect the environment by restricting the use of hazardous substances in new electrical and electronic devices
- To support the WEEE Directive (see above)

RoHS enforces the restriction of the following 6 hazardous substances in electronic and electrical devices:

- Lead (Pb) – no more than 0.1% by weight in homogeneous materials
- Mercury (Hg) – no more than 0.1% by weight in homogeneous materials
- Cadmium (Cd) – no more than 0.01% by weight in homogeneous materials
- Chromium (Cr6+) – no more than 0.1% by weight in homogeneous materials
- PBB, PBDE – no more than 0.1% by weight in homogeneous materials

Swissbit is obliged to minimize the hazardous substances in the products.

According to part of the Directive, manufacturers are obliged to make a self-declaration for all devices with RoHS. Swissbit carried out intensive tests to comply with the self-declaration. We have also already taken steps to have the analyses of the individual components guaranteed by third-party companies.

Swissbit carried out the following steps during the year with the goal of offering our customers products that are fully compliant with the RoHS Directive.

- **Preparing all far-reaching directives, logistical enhancements and alternatives regarding the full understanding and introduction of the RoHS Directive's standards**
- **Checking the components and raw materials:**
 - Replacing non-RoHS-compliant components and raw materials in the supply chain
 - Cooperating closely with suppliers regarding the certification of all components and raw materials used by Swissbit
- **Modifying the manufacturing processes and procedures**
 - Successfully adapting and optimizing the new management-free integration process in the supply chain
 - Updating existing production procedures and introducing the new procedures to support the integration process and the sorting of materials
- **Carrying out the quality process**
 - Performing detailed function and safety tests to ensure the continuous high quality of the Swissbit product line

When does the RoHS Directive take effect?

As of 1 July, 2006, only new electrical and electronic devices with approved quantities of RoHS will be put on the market.

When will Swissbit be offering RoHS-approved products?

Swissbit's RoHS-approved products are available now. Please contact your Swissbit contact person to find out more about exchanging your existing products for RoHS-compliant devices.

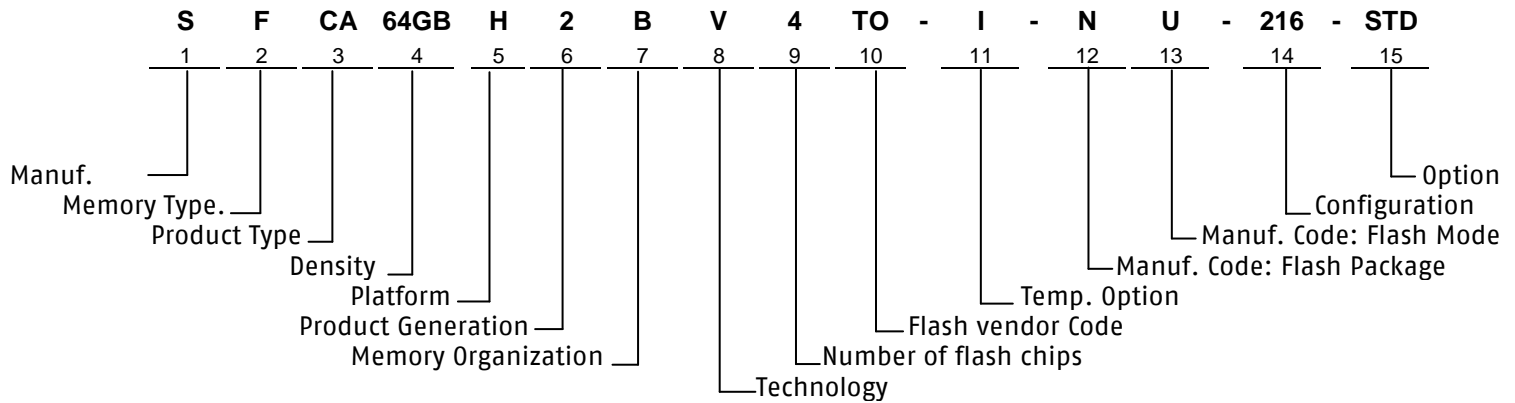
For your attention

We understand that packaging and accessories are not EEE material and are therefore not subject to the WEEE or RoHS Directives.

Contact details:

Swissbit AG
Industriestrasse 4
CH-9552 Bronschhofen
Tel: +41 71 913 03 03 – Fax: +41 71 913 03 15
E-mail: info@swissbit.com – Website: www.swissbit.com

11 Part Number Decoder



11.1 Manufacturer

| | |
|---------------|---|
| Swissbit code | S |
|---------------|---|

11.2 Memory Type

| | |
|-------|---|
| Flash | F |
|-------|---|

11.3 Product Type

| | |
|------------|----|
| CFast card | CA |
|------------|----|

11.4 Density

| | |
|----------|------|
| 2 GByte | 2048 |
| 4 GByte | 4096 |
| 8 GByte | 8192 |
| 16 GByte | 16GB |
| 32 GByte | 32GB |
| 64 GByte | 64GB |

11.5 Platform

| | |
|-----------------|---|
| CFast / CF-card | H |
|-----------------|---|

11.6 Product Generation

11.7 Memory Organization

| | |
|----|---|
| x8 | B |
|----|---|

11.8 Technology

| | |
|--------------|---|
| F-2X0 Series | V |
|--------------|---|

11.9 Number of Flash Chip

| | |
|---------|---|
| 4 Flash | 4 |
|---------|---|

11.10 Flash Code

| | |
|---------|----|
| Toshiba | TO |
| Micron | MT |
| Samsung | SA |

11.11 Temp. Option

| | | |
|------------------------|--------------|---|
| Industrial Temp. Range | -40°C – 85°C | I |
| Standard Temp. Range | 0°C – 70°C | C |

11.12 DIE Classification

| | |
|-------------------------------|---|
| SLC MONO (single die package) | M |
| SLC DDP (dual die package) | D |
| SLC QDP (quad die package) | Q |
| SLC ODP (octal die package) | N |

11.13 PIN Mode

| | |
|----------------------|-----|
| Normal nCE & R/nB | S/A |
| Dual nCE & Dual R/nB | T/B |
| Quad nCE & Quad R/nB | U/C |

11.14 Drive configuration XYZ

X → Type

| Drive Mode | PIO | DMA support | X |
|------------|-----|-------------|---|
| Fix | yes | yes | 2 |

Y → Firmware Revision

| FW Revision | Y |
|-------------|---|
| Firmware 1 | 1 |
| Firmware 2 | 2 |

Z → max. transfer mode

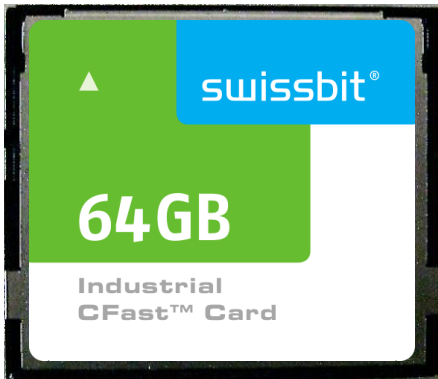
| Max PIO Mode | Z |
|---|---|
| UDMA6 (MDMA ₂ , PIO ₄) | 6 |

11.15 Option

| | |
|---------------------|-----|
| Swissbit / Standard | STD |
|---------------------|-----|

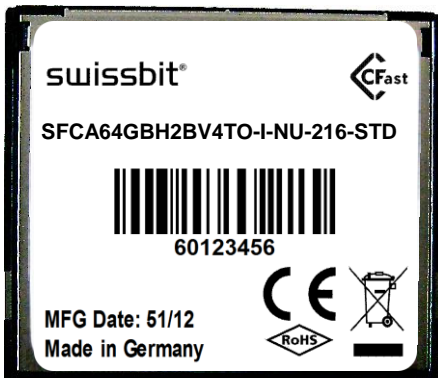
12 Swissbit CFast marking specification

12.1 Top view



Industrial CFast card

12.2 Bottom view



12.2.1 Label content:

- Swissbit logo
- CFast logo
- Part number
- Lot Code information with bar code
- CE logo
- RoHS logo
- WEEE logo
- Manufacturing Date
- Made in Germany

Revision History

Table 105: Document Revision History

| Date | Revision | Revision Details |
|-------------------|----------|--|
| October 25, 2012 | 1.00 | first released specification |
| November 21, 2012 | 1.10 | 2GB, 16GB, 32GB capacity corrected |
| December 18, 2012 | 1.20 | Added new CE Declaration, new picture of the back side label |
| July 04, 2013 | 1.21 | Corrected 32GB and 64GB part number |

Disclaimer:

No part of this document may be copied or reproduced in any form or by any means, or transferred to any third party, without the prior written consent of an authorized representative of Swissbit AG ("SWISSBIT"). The information in this document is subject to change without notice. SWISSBIT assumes no responsibility for any errors or omissions that may appear in this document, and disclaims responsibility for any consequences resulting from the use of the information set forth herein. SWISSBIT makes no commitments to update or to keep current information contained in this document. The products listed in this document are not suitable for use in applications such as, but not limited to, aircraft control systems, aerospace equipment, submarine cables, nuclear reactor control systems and life support systems. Moreover, SWISSBIT does not recommend or approve the use of any of its products in life support devices or systems or in any application where failure could result in injury or death. If a customer wishes to use SWISSBIT products in applications not intended by SWISSBIT, said customer must contact an authorized SWISSBIT representative to determine SWISSBIT willingness to support a given application. The information set forth in this document does not convey any license under the copyrights, patent rights, trademarks or other intellectual property rights claimed and owned by SWISSBIT. The information set forth in this document is considered to be "Proprietary" and "Confidential" property owned by SWISSBIT.

ALL PRODUCTS SOLD BY SWISSBIT ARE COVERED BY THE PROVISIONS APPEARING IN SWISSBIT'S TERMS AND CONDITIONS OF SALE ONLY, INCLUDING THE LIMITATIONS OF LIABILITY, WARRANTY AND INFRINGEMENT PROVISIONS. SWISSBIT MAKES NO WARRANTIES OF ANY KIND, EXPRESS, STATUTORY, IMPLIED OR OTHERWISE, REGARDING INFORMATION SET FORTH HEREIN OR REGARDING THE FREEDOM OF THE DESCRIBED PRODUCTS FROM INTELLECTUAL PROPERTY INFRINGEMENT, AND EXPRESSLY DISCLAIMS ANY SUCH WARRANTIES INCLUDING WITHOUT LIMITATION ANY EXPRESS, STATUTORY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

©2013 SWISSBIT AG All rights reserved.