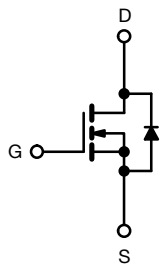
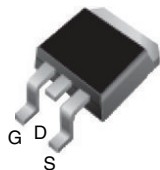


E Series Power MOSFET

D²PAK (TO-263)


N-Channel MOSFET

FEATURES

- Low figure-of-merit (FOM): $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	650	
$R_{DS(on)}$ max. (Ω) at 25 °C	$V_{GS} = 10$ V	0.099
Q_g max. (nC)	150	
Q_{gs} (nC)	24	
Q_{gd} (nC)	42	
Configuration	Single	

ORDERING INFORMATION

Package	D ² PAK (TO-263)
Lead (Pb)-free	SiHB33N60E-E3
Lead (Pb)-free and Halogen-free	SiHB33N60E-GE3
	SiHB33N60ET5-GE3
	SiHB33N60ET1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current ^a	I_{DM}	88	
Linear Derating Factor		2.2	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	793	mJ
Maximum Power Dissipation	P_D	278	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	dV/dt	$V_{DS} = 0$ V to 80 % V_{DS}	V/ns
Reverse Diode dV/dt ^d			
Soldering Recommendations (Peak temperature) ^c	for 10 s	300	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{PD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 7.5$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C

**THERMAL RESISTANCE RATINGS**

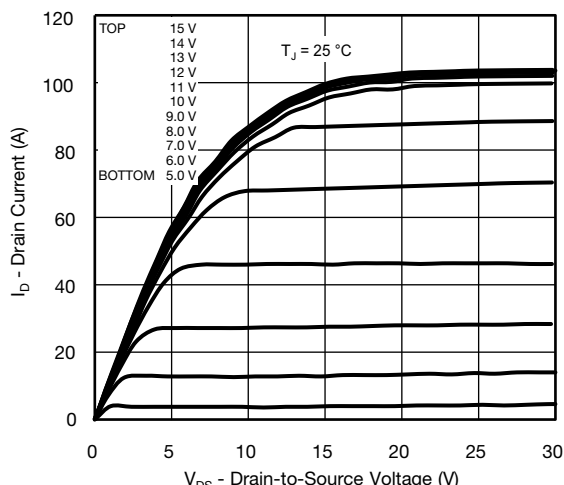
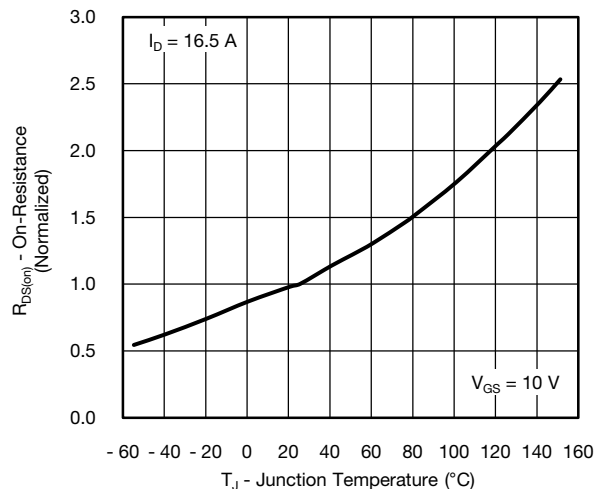
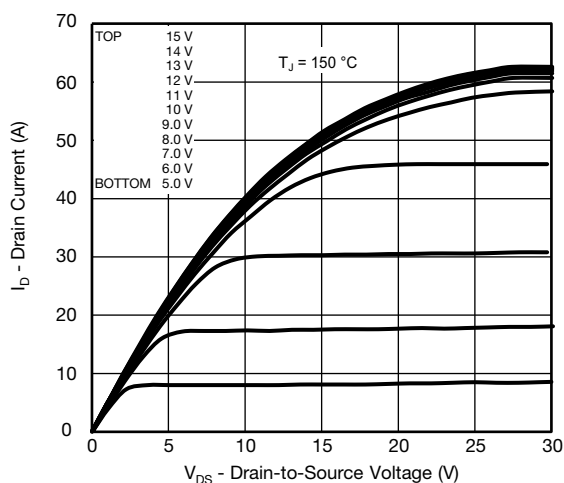
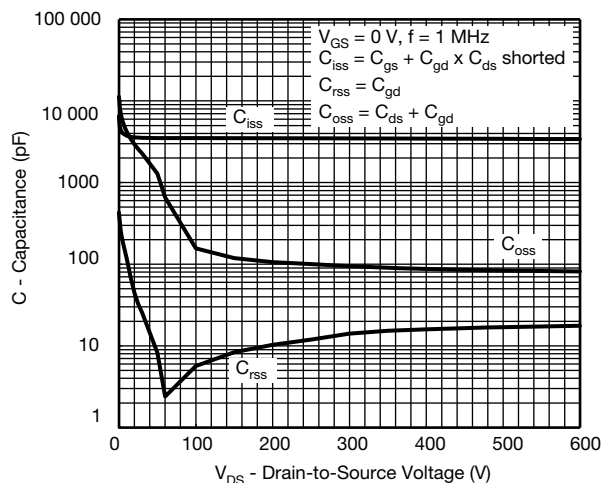
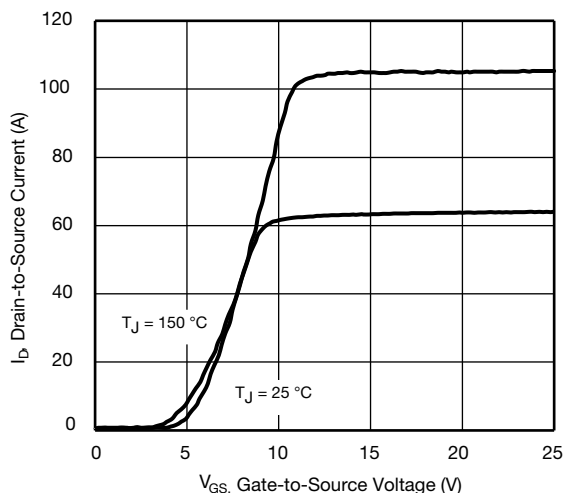
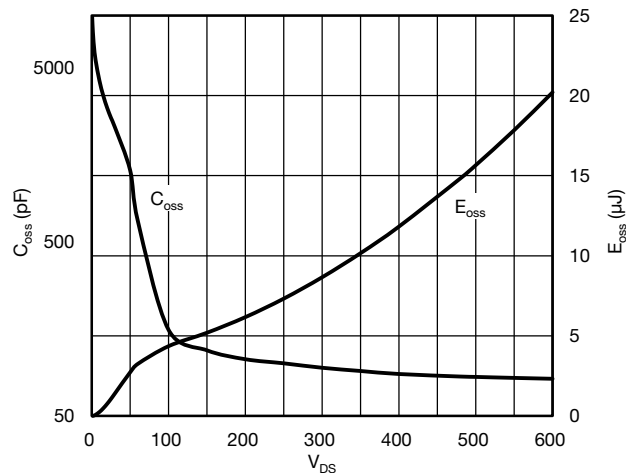
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.45	

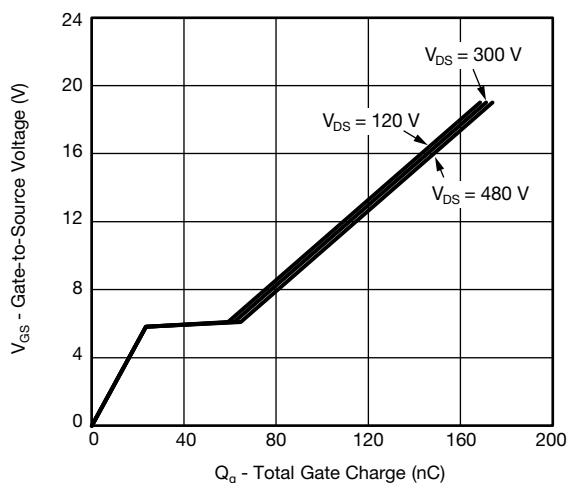
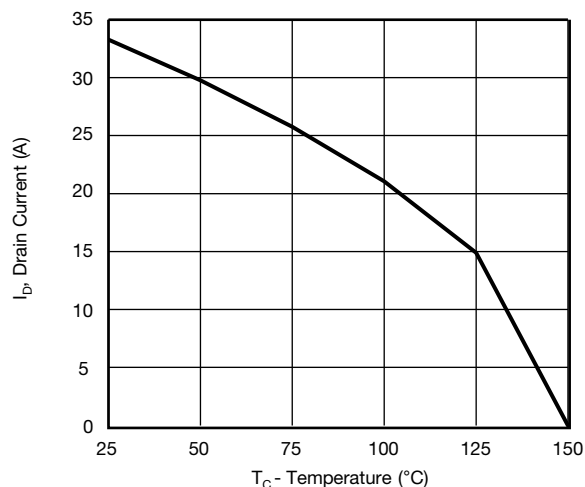
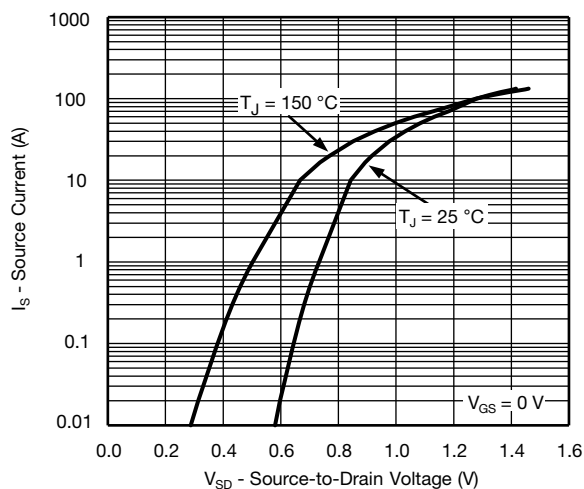
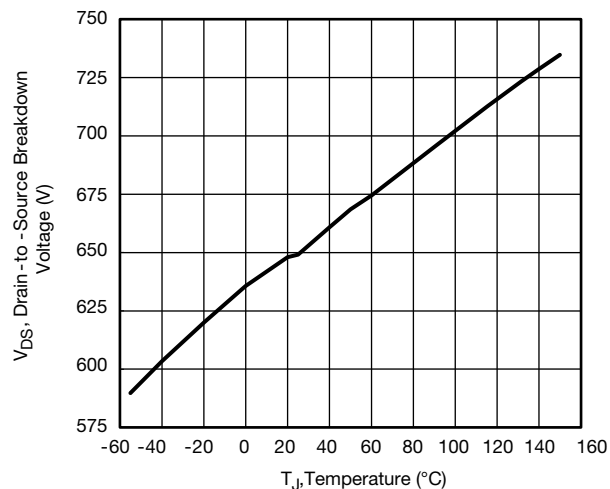
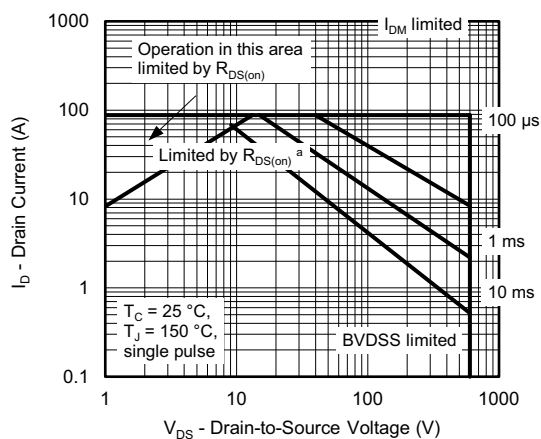
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

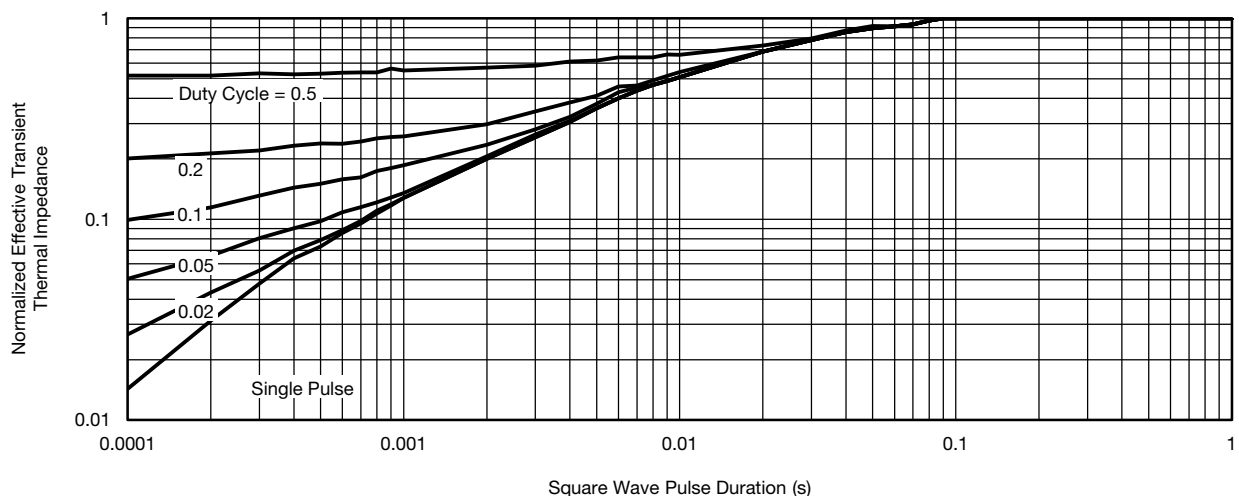
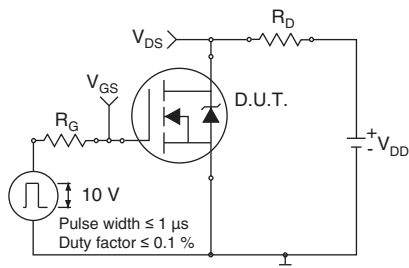
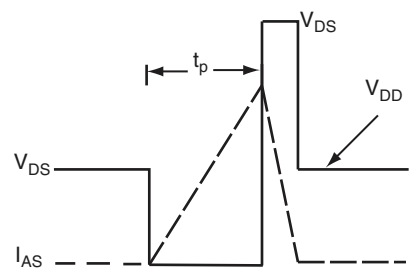
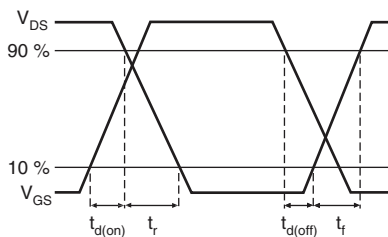
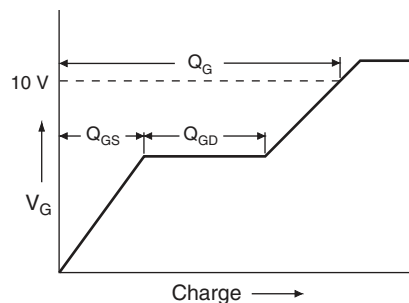
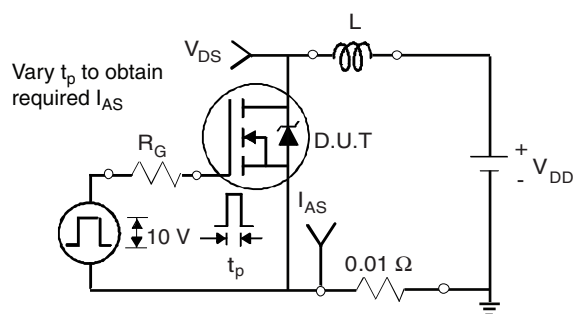
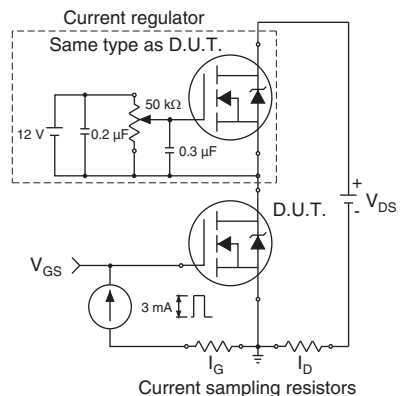
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 1\text{ mA}$	-	0.71	-	V/ $^{\circ}\text{C}$
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$	-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 480\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$	-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 16.5\text{ A}$	-	0.083	0.099	Ω
Forward Transconductance ^a	g_{fs}	$V_{DS} = 30\text{ V}$, $I_D = 16.5\text{ A}$	-	11	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$	-	3508	-	pF
Output Capacitance	C_{oss}		-	156	-	
Reverse Transfer Capacitance	C_{rss}		-	6	-	
Effective Output Capacitance, Energy Related ^b	$C_{o(er)}$	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ V to } 480\text{ V}$	-	136	-	
Effective Output Capacitance, Time Related ^c	$C_{o(tr)}$		-	468	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$, $I_D = 16.5\text{ A}$, $V_{DS} = 480\text{ V}$	-	100	150	nC
Gate-Source Charge	Q_{gs}		-	24	-	
Gate-Drain Charge	Q_{gd}		-	42	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 480\text{ V}$, $I_D = 16.5\text{ A}$ $R_g = 9.1\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	28	56	ns
Rise Time	t_r		-	60	90	
Turn-Off Delay Time	$t_{d(off)}$		-	99	150	
Fall Time	t_f		-	54	80	
Gate Input Resistance	R_g	$f = 1\text{ MHz}$, open drain	0.2	0.7	1.0	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	33	A
Pulsed Diode Forward Current	I_{SM}		-	-	88	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 16.5\text{ A}$, $V_{GS} = 0\text{ V}$	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = I_S$, $dI/dt = 100\text{ A}/\mu\text{s}$, $V_R = 20\text{ V}$	-	503	1006	ns
Reverse Recovery Charge	Q_{rr}		-	8.5	17	μC
Reverse Recovery Current	I_{RRM}		-	26	-	A

Notes

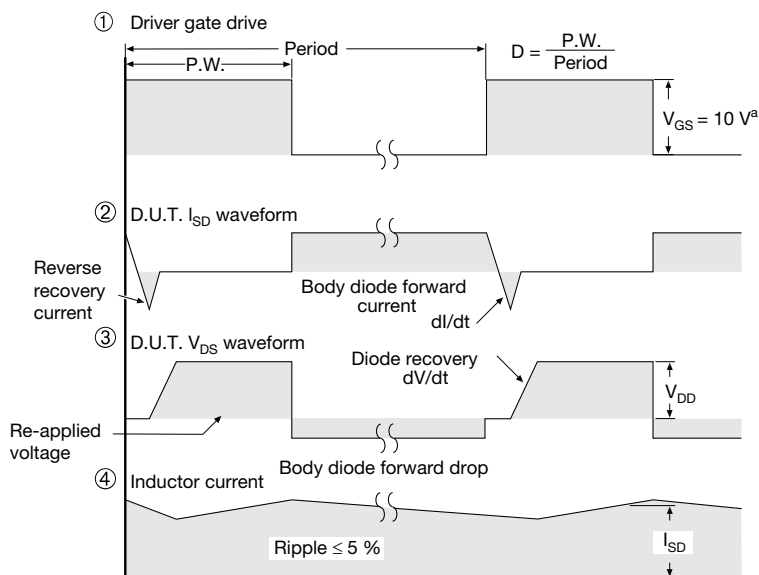
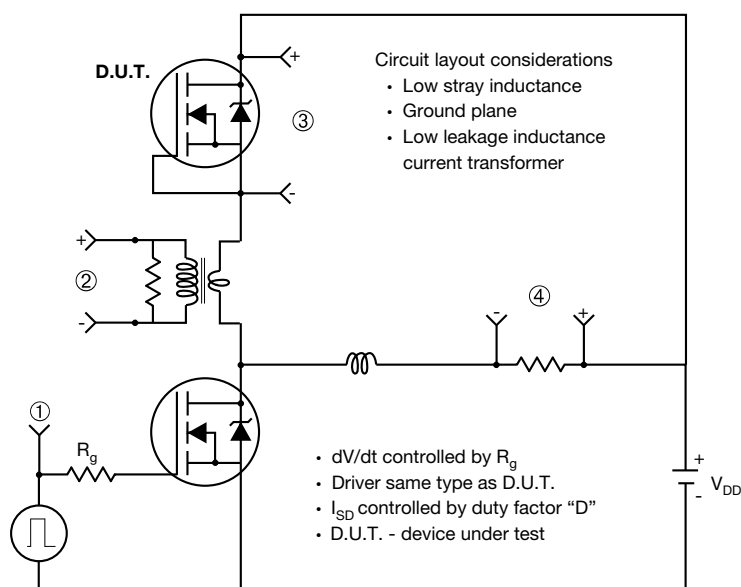
- a. Repetitive rating; pulse width limited by maximum junction temperature
- b. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
- c. $C_{oss(tr)}$ is a fixed capacitance that gives the charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 10 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Typical Source-Drain Diode Forward Voltage

Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature

Fig. 9 - Maximum Safe Operating Area


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

Fig. 13 - Switching Time Test Circuit

Fig. 16 - Unclamped Inductive Waveforms

Fig. 14 - Switching Time Waveforms

Fig. 17 - Basic Gate Charge Waveform

Fig. 15 - Unclamped Inductive Test Circuit

Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 \text{ V}$ for logic level devices

Fig. 19 - For N-Channel

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TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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