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Specification	
Part Number:	MCT028J6W240320PML
Version:	
Date:	

Revision

No.	Date	Description	Item	Page

Midas Active Matrix Display Part Number System

MC	T	057	A	6	*	W	320240	L	M	L	*	*	*	*	*
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

1 = **MC:** Midas Components

2 = **T:** TFT **A:** Active Matrix OLED

3 = **Size**

4 = **Series**

5 = **Viewing Angle: 6:** 6 O'clock **12:** 12 O'clock **O:** All round

6 = **Blank:** No Touch **T:** Resistive Touchscreen **C:** Capacitive Touchscreen

7 = **Operating Temp Range:** **S:** 0 to 50Deg C **B:** -20+60Deg C
W: -20+70Deg C **E:** -30+85Deg C

8 = **No of Pixels**

9 = **Orientation:** **P:** Portrait **L:** Landscape

10 = **Mode:** **R:** Reflective **M:** Transmissive **T:** Transflective
S: Sunlight Readable (transmissive)
W: White on Black (Monochrome)

11 = **Backlight:** **Blank:** None **L:** LED **C:** CCFL

12 = **Blank:** No Module/board **C:** Controller board module

13 = **Blank:** None **V**: Video

14 = **Blank:** None **B**: Bracket

15 = **Blank:** None **H**: Host Cable

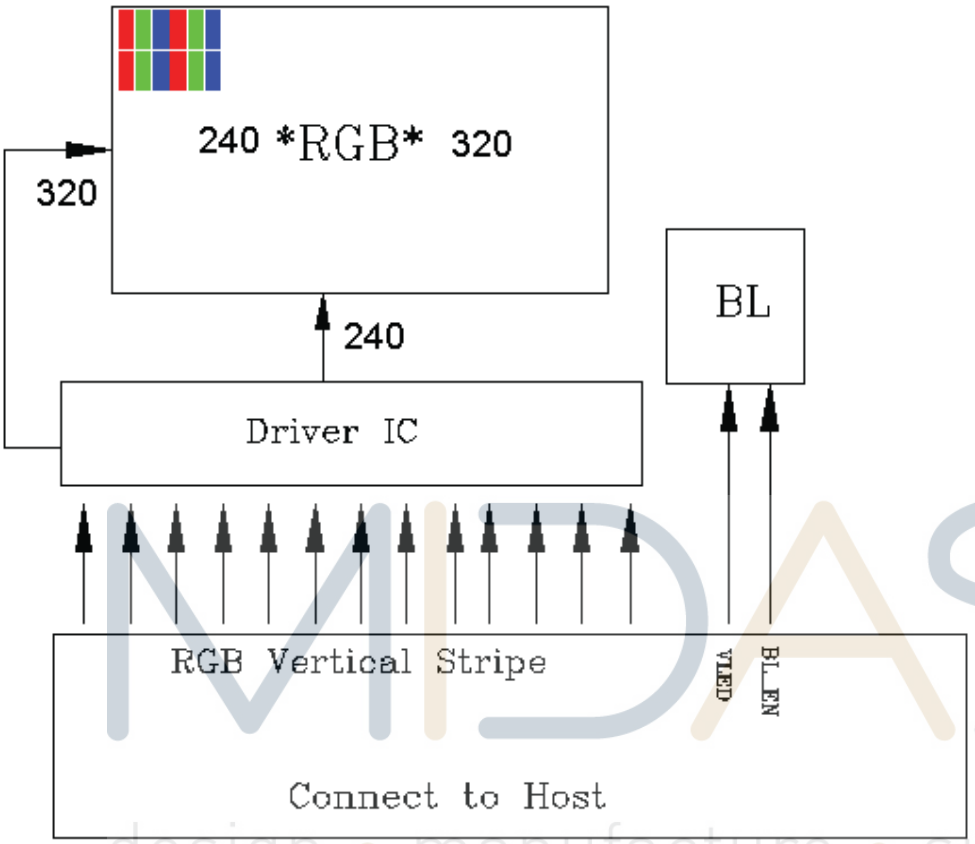
16 = **Blank:** None **K**: Keyboard

GENERAL SPECIFICATIONS

ITEM	SPECIFICATION	UNIT
OUTLINE DIMEMSIONS	50(W) X69.2 (H) X2.45 (D)	mm
DISPLAY SIZE	2.8	inch
DOT PITCH	0.18mmX0.18mm	mm
NUMBER OF DOTS	240*（RGB）*320	-
DRIVER IC	ILI9341	-
LCD TYPE	TFT(262K) TRANSMISSIVE	-
INTERFACE	MCU 16 BITS	
BACKLIGHT TYPE	LED White	-
VIEWING DIRECTION	6 O'clock	-

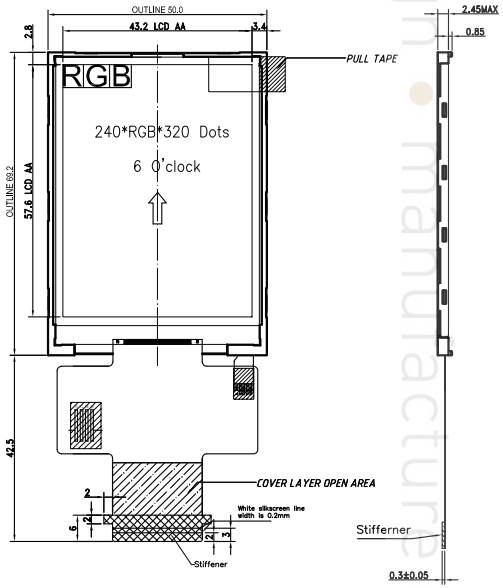
***See attached drawing for details.**

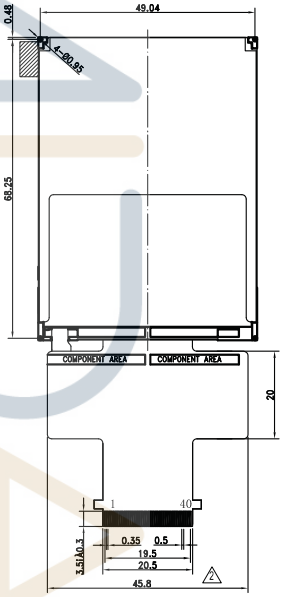
BLOCK DIAGRAM



DIMENSIONAL OUTLINE

REV	DESCRIPTION	DATE
A0	First issue	JAN-26-2013

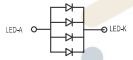




40	YU (NC)
39	XL (NC)
38	YD (NC)
37	XR (NC)
36	CS
35	RS
34	WR
33	RD
32	DB0
31	DB1
30	DB2
29	DB3
28	DB4
27	DB5
26	DB6
25	DB7
24	DB8
23	DB9
22	DB10
21	DB11
20	DB12
19	DB13
18	DB14
17	DB15
16	DB16
15	DB17
14	GND
13	RESET
12	VCC
11	HSYNC
10	VSYNC
9	DE
8	DOTCLK
7	SDA
6	NC
5	NC
4	NC
3	GND
2	LEDA
1	LEDK

NOTES:

1. Display type: 2.8" TFT, 240(RGB)X320
2. Viewing angle: 6 O'clock
3. Display mode: 262K TFT/Transmissive/Normal White
4. Operating temp.: -20°C~+70°C
5. Storage temp.: -30°C~+80°C
6. IC: ILI9341
7. Logic power supply voltage: 2.8V
8. Backlight: 4 chip White LED , In Parallel, If=60mA
9. Luminance: 260cd/m2
10. All the raw material are Rohs complicant



B/L CIRCUIT DIAGRAM
4 PCS WHITE LED;IF =60mA,VF=3.2V

SHEET: 1 OF 1		Midas Displays	
SCALE: DO NOT SCALE			
GEN TOLERANCE: ±0.3	UNIT mm	PROJECTION	PART NO:
APP: BC	01/26/2013		MCT028J6W240320PML
CHK: JQ	01/26/2013		
DWN: PW	01/28/2013		

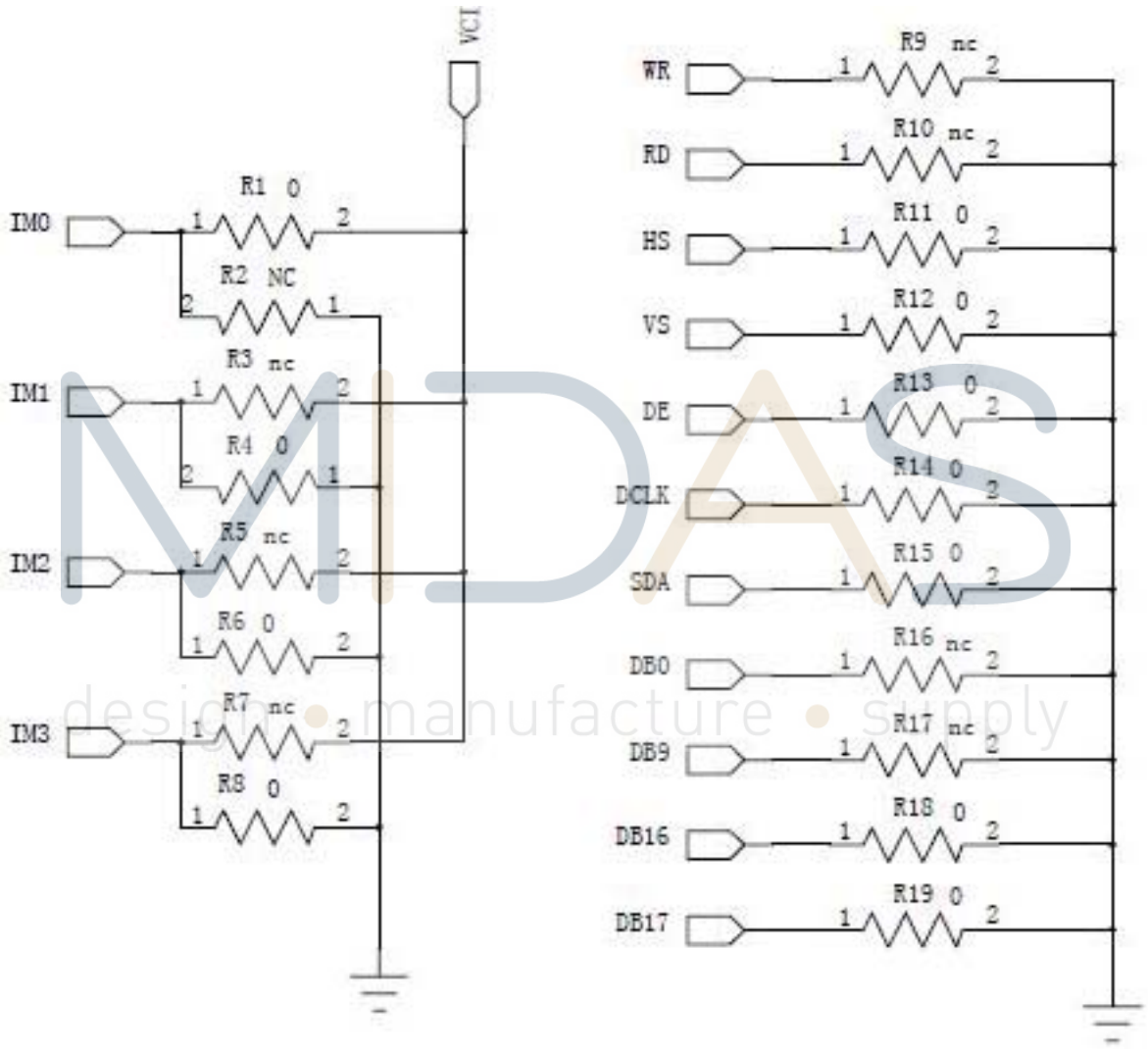
PIN DESCRIPTION:

<table>
<tr><th>NO.</th><th>PIN NAME</th><th>Type</th><th>Description</th></tr>
<tr><td>1</td><td>LEDK</td><td>P</td><td>Power supply for LED (Cathode)</td></tr>
<tr><td>2</td><td>LEDA</td><td>P</td><td>Power supply for LED (Anode)</td></tr>
<tr><td>3</td><td>GND</td><td>P</td><td>Ground(0V)</td></tr>
<tr><td>4~6</td><td>NC</td><td>-</td><td>No connection</td></tr>
<tr><td>7</td><td>SDA</td><td>I/O</td><td>SPI Serial Data Input/output</td></tr>
<tr><td>8</td><td>DOTCLK</td><td>I</td><td>Pixel clock signal</td></tr>
<tr><td>9</td><td>DE</td><td>I</td><td>Data enable</td></tr>
<tr><td>10</td><td>VSYNC</td><td>I</td><td>Vertical synchronizing signal</td></tr>
<tr><td>11</td><td>HSYNC</td><td>I</td><td>Horizontal synchronizing signal</td></tr>
<tr><td>12</td><td>VCC</td><td>P</td><td>Power voltage</td></tr>
<tr><td>13</td><td>RESET</td><td>I</td><td>Reset signal</td></tr>
<tr><td>14</td><td>GND</td><td>P</td><td>Ground(0V)</td></tr>
<tr><td>15~32</td><td>DB17~DB0</td><td>I/O</td><td>Data bus
- Select the MCU interface mode
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">MCU-Interface Mode</th><th colspan="2">DB Pin in use</th></tr>
<tr><th>Register/Content</th><th>GRAM</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80 MCU 8-bit bus interface I</td><td>D[7:0]</td><td>D[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>80 MCU 16-bit bus interface I</td><td>D[7:0]</td><td>D[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80 MCU 9-bit bus interface I</td><td>D[7:0]</td><td>D[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80 MCU 18-bit bus interface I</td><td>D[7:0]</td><td>D[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface I</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface I</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>80 MCU 16-bit bus interface II</td><td>D[8:1]</td><td>D[17:10], D[8:1]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>80 MCU 8-bit bus interface II</td><td>D[17:10]</td><td>D[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80 MCU 18-bit bus interface II</td><td>D[8:1]</td><td>D[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80 MCU 9-bit bus interface II</td><td>D[17:10]</td><td>D[17:9]</td></tr>
</table>
In MPU Parallel interface bus and serial interface select
If use RGB Interface must select serial interface (3SPI 0101)
* : Fix this pin at VDDI or VSS</td></tr>
<tr><td>33</td><td>RD</td><td>I</td><td>Read signal, active at low in MCU mode;
In SPI mode, connect to GND</td></tr>
<tr><td>34</td><td>WR</td><td>I</td><td>Write Signal, active at low in MCU mode;
In SPI mode, SPI Serial Clock</td></tr>
<tr><td>35</td><td>RS</td><td>I</td><td>In MCU mode, Register select signal, low is selected data register; High is selected command register. In SPI mode, connect to GND</td></tr>
<tr><td>36</td><td>CS</td><td>I</td><td>Chip selection pin/ Serial port data enable signal</td></tr>
<tr><td>37</td><td>XR(NC)</td><td>-</td><td>No connection</td></tr>
<tr><td>38</td><td>YD(NC)</td><td>-</td><td>No connection</td></tr>
<tr><td>39</td><td>XL(NC)</td><td>-</td><td>No connection</td></tr>
<tr><td>40</td><td>YU(NC)</td><td>-</td><td>No connection</td></tr>
</table>

Note: 1: input, 0: output, P: Power

Link to example connector

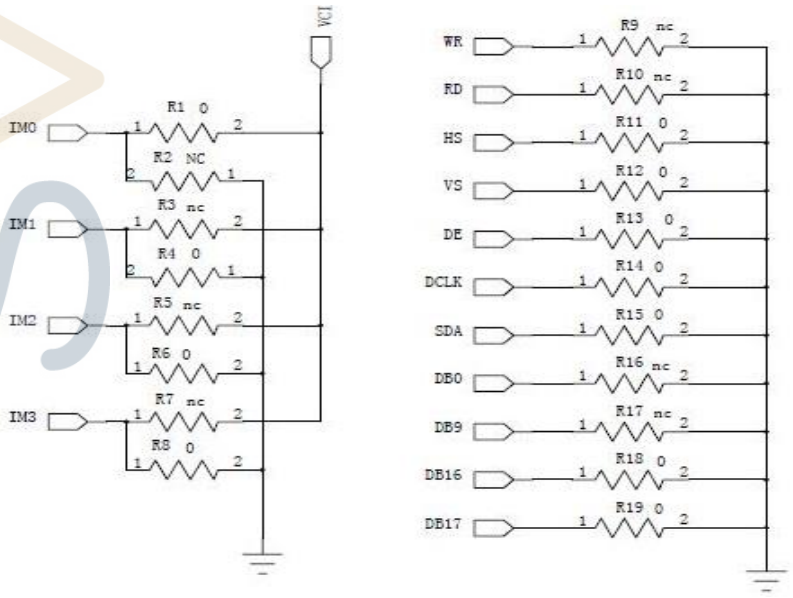
Note: 2: Default interface of this part is “80 MCU 16-bit bus interface I” ([IM3:IM0] =0001), and “HS”, “VS”, “DE”, “DCLK”, “SDA”, “DB16”, “DB17”, already are connected to GND via 0 ohm resistor on FPC. Refer to below circuit.



IM3	IM2	IM1	IM0	MCU-Interface Mode	DB pin in use		PIN of LCM to Gnd
					Register/content	GRAM	
0	0	0	0	80 MCU 8bit -bus	DB(7-0)	DB(7-0)	**HS,VS,DE,DCLK,SDA,DB8-DB17**
0	0	0	1	80 MCU 16bit -bus	DB(7-0)	DB(15-0)	HS,VS,DE,DCLK,SDA,DB16,DB17
0	0	1	0	80 MCU 9bit -bus	DB(7-0)	DB(8-0)	**HS,VS,DE,DCLK,SDA,DB9-DB17**
0	0	1	1	80 MCU 18bit -bus	DB(7-0)	DB(17-0)	**HS,VS,DE,DCLK,SDA**
0	1	0	1	3-wire 9-bit date serial	SDA in/out		**HS,VS,DE,DCLK,RS,RD,DB0-DB17**
0	1	1	0	4-wire 8-bit date serial	SDA in/out		**HS,VS,DE,DCLK,RD,DB0-DB17**
1	0	0	0	80 MCU 16bit -bus	DB(8-1)	DB(17-10) (8-1)	**HS,VS,DE,DCLK,SDA,DB0,DB9**
1	0	0	1	80 MCU 8bit -bus	DB(17-10)	DB(17-10)	**HS,VS,DE,DCLK,SDA,DB0-DB9**
1	0	1	0	80 MCU 18bit -bus	DB(17-10)	DB(17-0)	**HS,VS,DE,DCLK,SDA**
1	0	0	1	80 MCU 9bit -bus	DB(8-0)	DB(17-9)	**HS,VS,DE,DCLK,SDA,DB0-DB8**
R6=0	**R5=0**	**R3=0**	**R1=0**				
R8=1	**R6=1**	**R4=1**	**R2=1**				

NOTE:

Default interface of this part is "80 MCU 16-bit bus interface I" ([IM3:IM0] =0001), and "HS", "VS", "DE", "DCLK", "SDA", "DB16", "DB17", already are connected to GND via 0 ohm resistor on FPC. Refer to below circuit.



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Item	Symbol	Values		Unit	Remark
		Min	Max		
Power Supply for Pump	VCC	-0.3	4.5	V	
Operating temperature range	To	-20	70	Degree C	
Storage temperature range	Ts	-30	80	Degree C	
Logic input voltage range	VI	-0.3	VCC+0.3	V	
Logic input voltage range	VO	-0.3	VCC+0.3	V	

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics

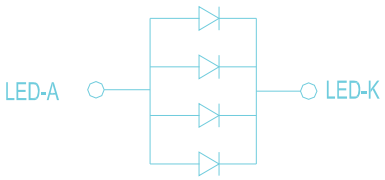
DC Characteristics

Item	Symbol	Values			Unit	Conditions
		Min	Typ	Max		
Low Level Input Voltage	Vil	GND	-	0.3xVCC	v	
High Level Input Voltage	Vih	0.7xVCC	-	VCC	uA	
High Level Output Voltage	Voh	VCC-0.4	-	VCC	ohm	
Low Level Output Voltage	Vol	GND	-	GND+0.4	uA	
Power Supply	VCC	2.5	2.8	3.3	V	
Input Leakage Current	Iil			±1.0	uA	
Pull High/Low Resistor	Rp	-	100K	-	ohm	

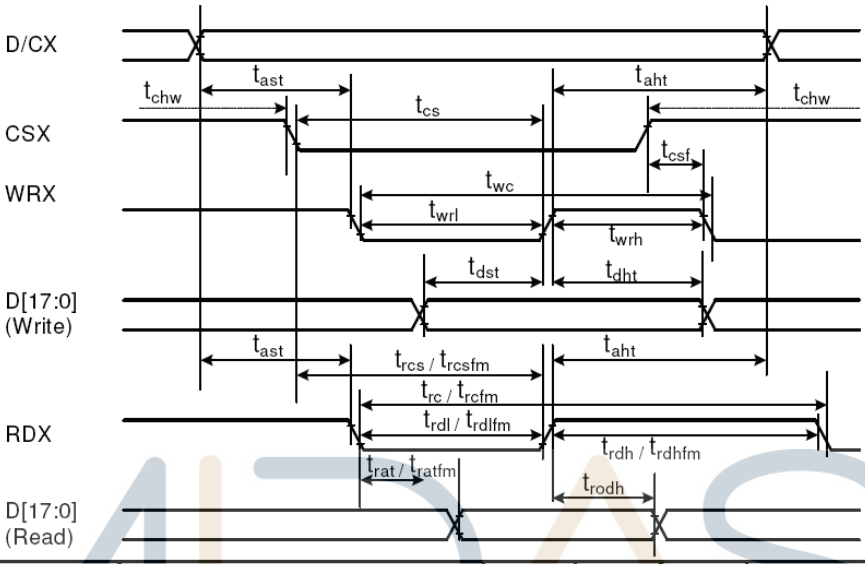
Item	Symbol	Min	Typ	Max	Unit	Remark
Average luminous Intensity	Iv		260		cd/m2	IF=60mA
Chromaticity Coordinates	X	0.234	0.284	0.334		IF=60mA
	Y	0.273	0.323	0.373		IF=60mA
Forward Voltage	VF		3.2	3.4	V	IF=60mA
Reverse Current	IR			50	μA	VR=5V,1LED
Luminous Tolerance	IV-M	80			%	(MIN/MAX)×100
Power Dissipation	Pd	192			mW	
Peak Forward Current	Ifp	100			uA	
Reverse Voltage	VR	5			V	

B/L CIRCUIT DIAGRAM

4 PCS WHITE LED;IF =60mA,VF=3.2V

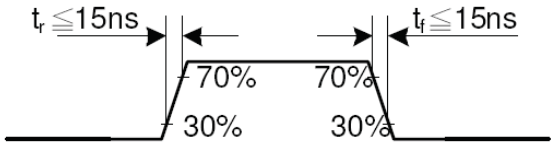


Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- Ⅰ system)

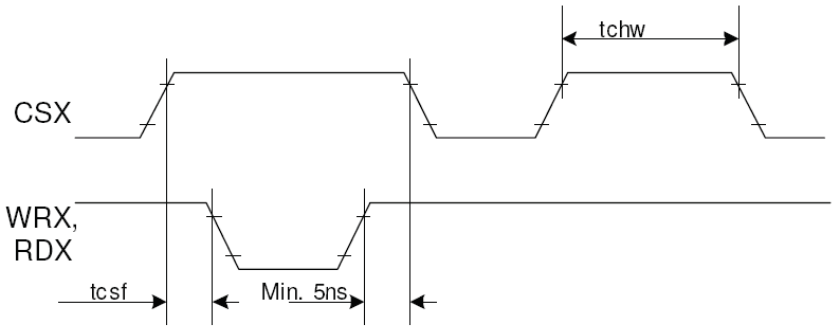


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

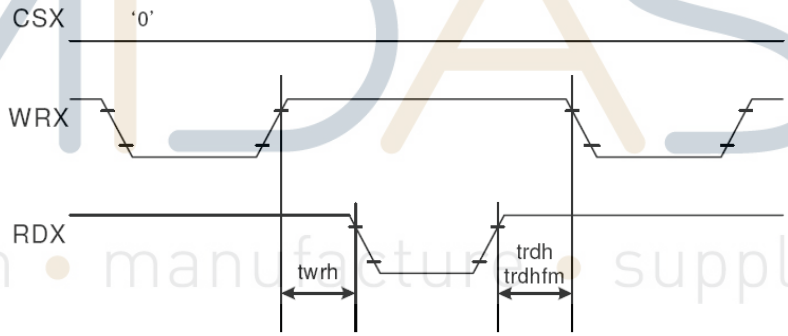


CSX timings :



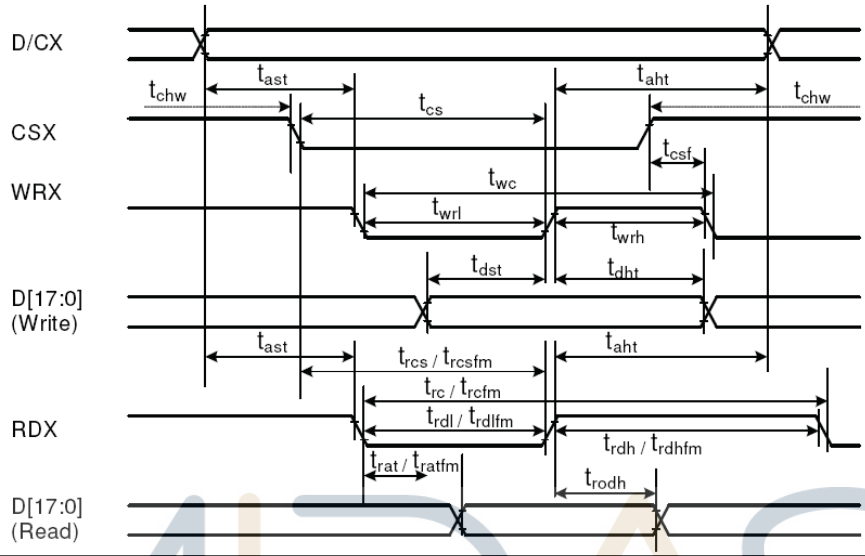
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



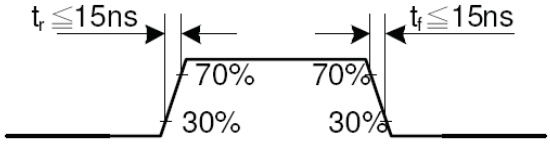
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-Ⅱ system)

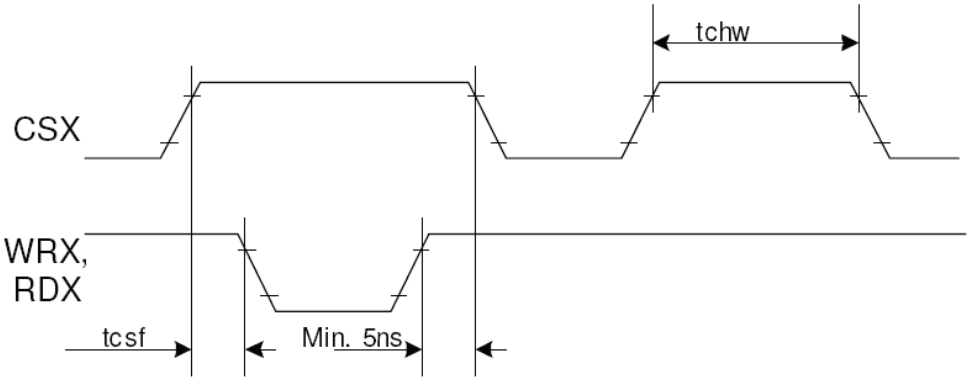


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.

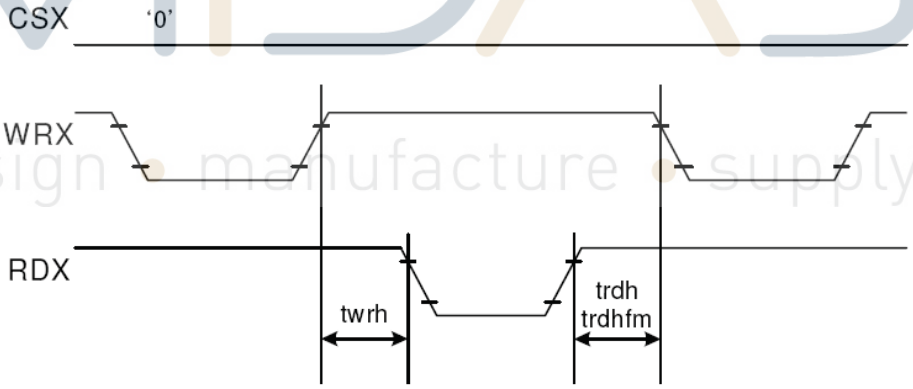


CSX timings :



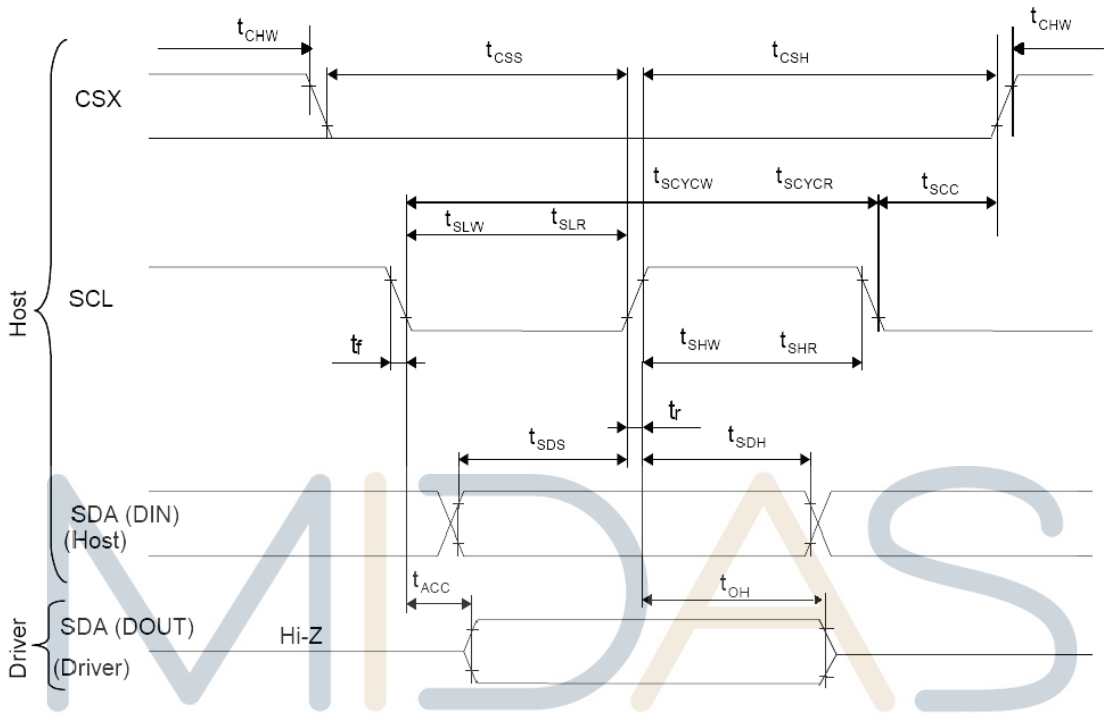
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



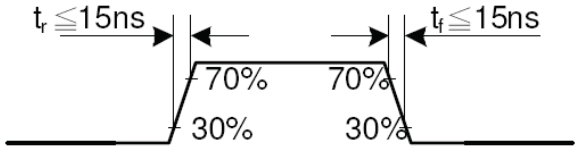
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Display Serial Interface Timing Characteristics (3-line SPI system)

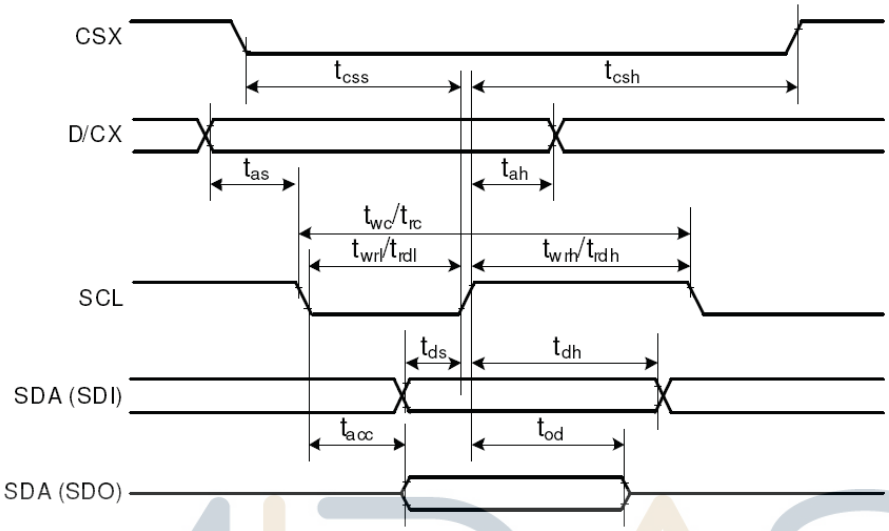


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: Ta = 25 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

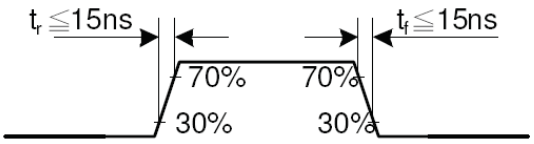


Display Serial Interface Timing Characteristics (4-line SPI system)

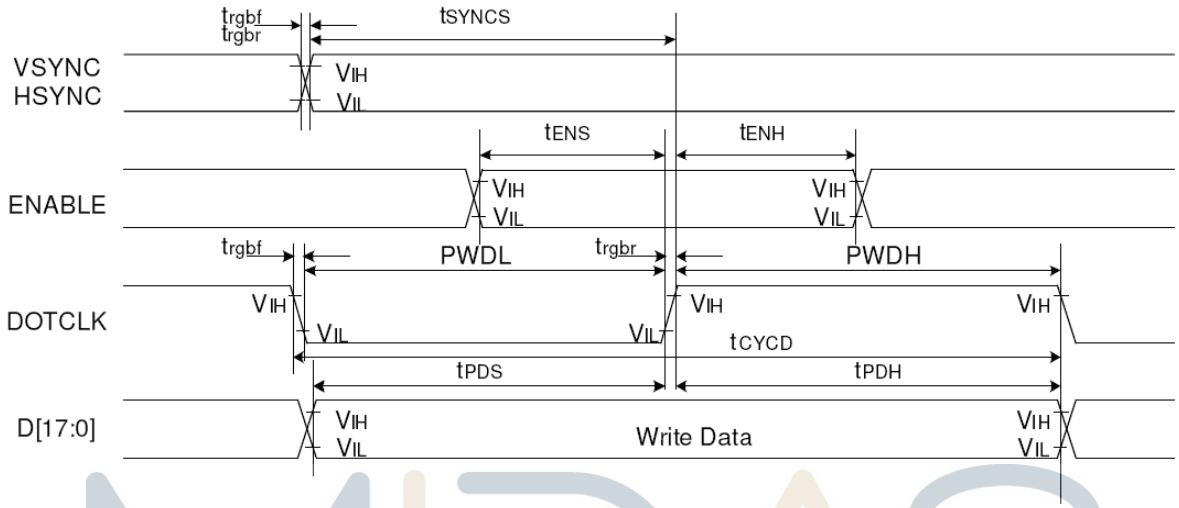


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL "H" pulse width (Write)	40	-	ns	
	twrl	SCL "L" pulse width (Write)	40	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	tod	Output disable time (Read)	10	50	ns	For minimum CL=8pF

Note: Ta = 25 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

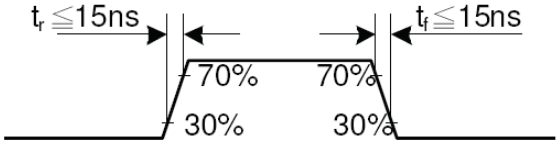


Parallel 18/16/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V



Controller Information

IC: ILI9341

OPTICAL CHARACTERISTICS

Item		Symbol	Conditions	Specifications	Unit	Note
Transmittance		T%	Viewing normal angle $\theta_X = \theta_Y = 0°$	6.0	%	All left side data are based on CMO's following condition – 1.CG : NTSC 59% 2.LC : TN 3.Light Source : CMO LED BLU 4.Film : Nitto Linear Polarizer 5.Machine : DMS
Contrast Ratio		CR		300	--	
Response Time (by Quick)		Ton+ Toff		30	ms	
Viewing Angle	Hor.	θ_{X+}	Center CR>10	45	deg.	
		θ_{X-}		45		
	Ver.	θ_{Y+}		45		
		θ_{Y-}		20		
CF only Chromaticity	Red	X_R	Viewing normal angle $\theta_X = \theta_Y = 0°$	0.631	--	Under C light Simulation
		Y_R		0.316	--	
	Green	X_G		0.298	--	
		Y_G		0.566	--	
	Blue	X_B		0.138	--	
		Y_B		0.122	--	
	White	X_W		0.297	--	
		Y_W		0.327		

*Note (1) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

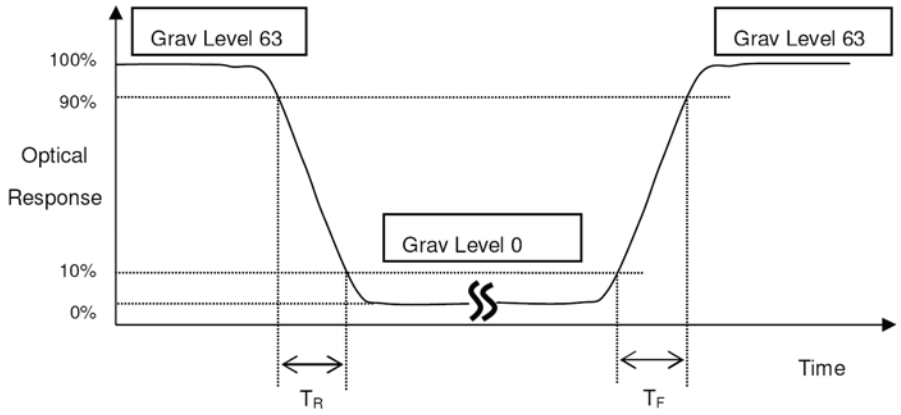
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

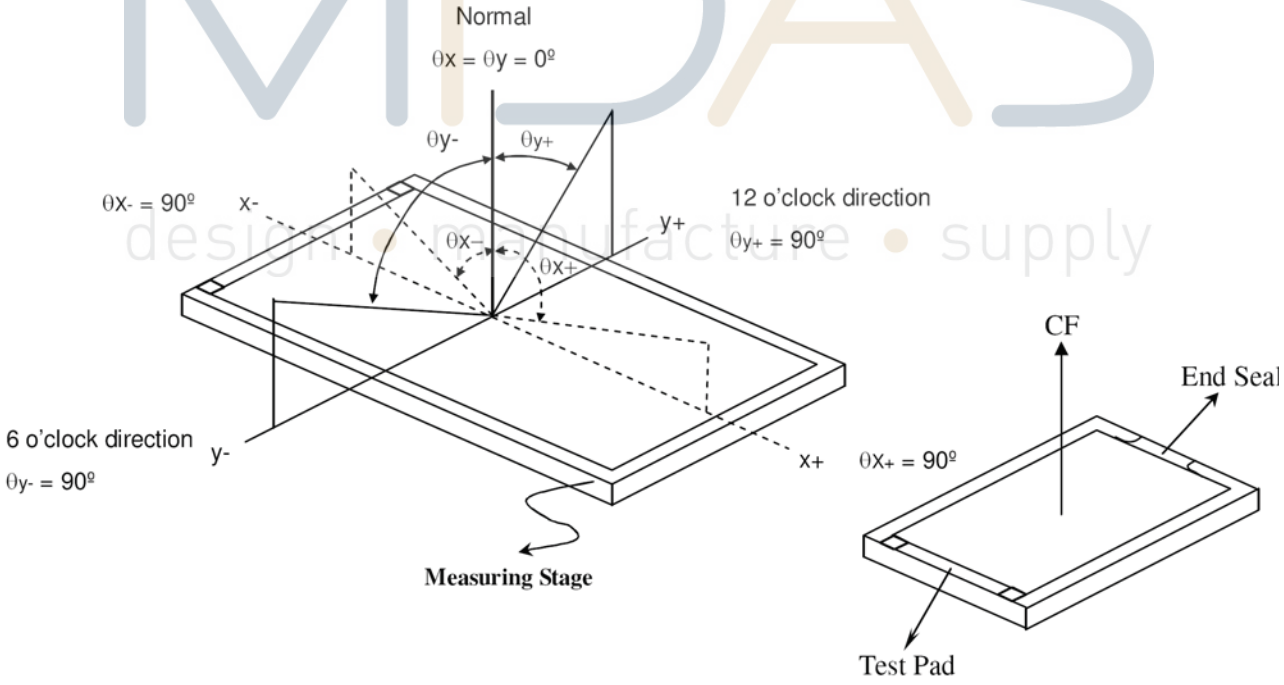
CR = CR (10)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (5).

*Note (2) Definition of Response Time (Ton, Toff):

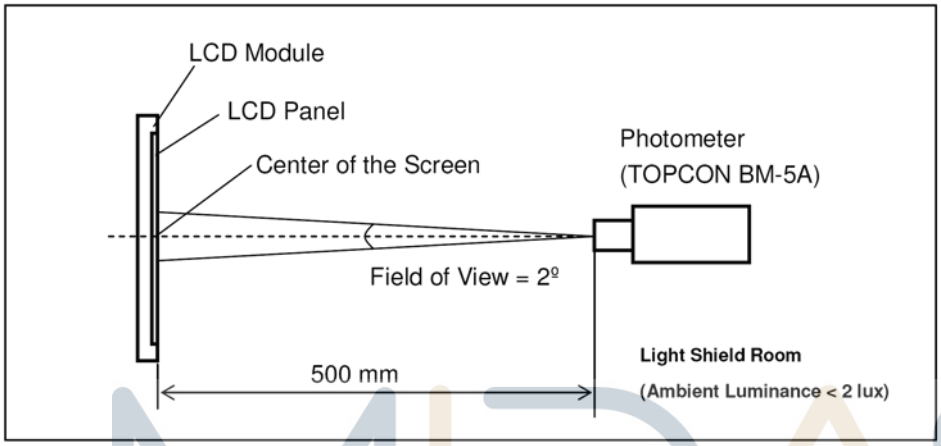


*Note(3) Definition of Viewing Angle

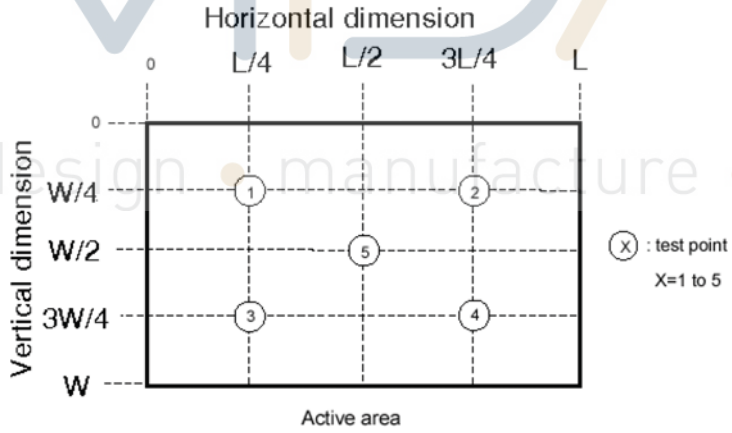


*Note (4) Measurement Set-Up:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (5)



PACKAGE