

PSMN013-100YSE

N-channel 100 V 13 mΩ standard level MOSFET in LFPAK56

18 December 2012

Product data sheet

1. General description

Standard level N-channel MOSFET in a LFPAK56 package qualified to 175 °C. Part of NXP's "NextPower Live" portfolio, the PSMN013-100YSE complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn on, whilst offering a low $R_{DS(on)}$ characteristic to keep temperatures down and efficiency up in continued use. Ideal for telecommunication systems based on a 48 V backplane / supply rail.

2. Features and benefits

- Enhanced forward biased safe operating area for superior linear mode operation
- Very low $R_{DS(on)}$ for low conduction losses

3. Applications

- Electronic fuse
- Hot swap
- Load switch
- Soft start

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 1	-	-	58	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2	-	-	238	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 20\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12	-	11	13	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 20\text{ A}$; $V_{DS} = 50\text{ V}$; Fig. 14 ; Fig. 15	-	26	-	nC
$Q_{G(tot)}$	total gate charge		-	75	-	nC



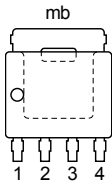
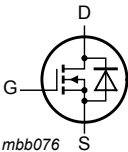
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche Ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 82\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped; Fig. 3	-	-	125	mJ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK; Power-SO8 (SOT669)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN013-100YSE	LPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN013-100YSE	13100

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 1	-	82	A

Symbol	Parameter	Conditions		Min	Max	Unit
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 1		-	58	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 4		-	330	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2		-	238	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$		-	100	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	330	A
Avalanche Ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 82\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped; Fig. 3		-	125	mJ

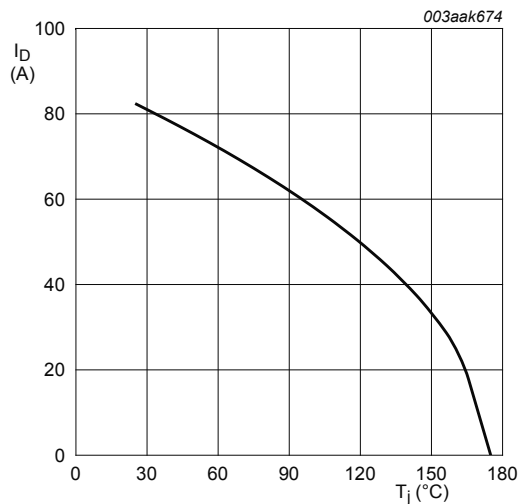


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10V$$

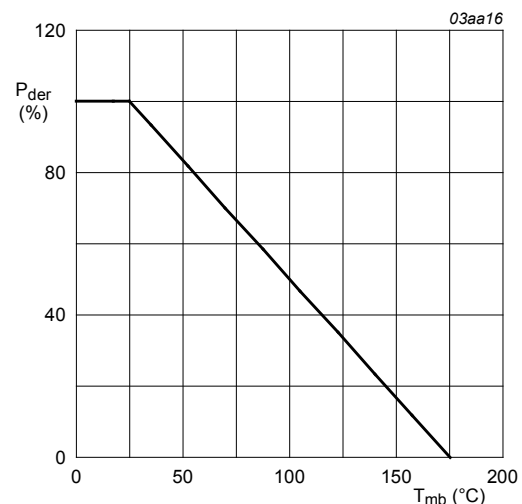


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

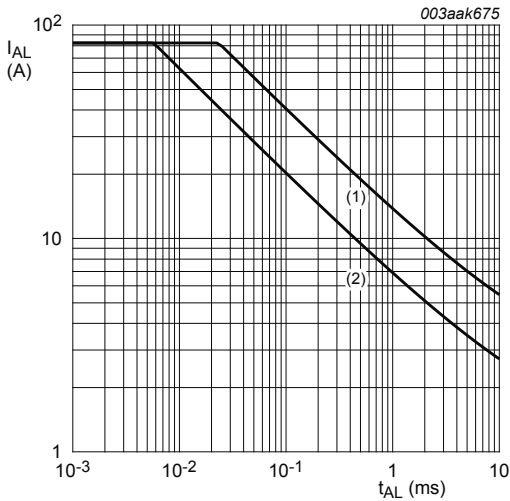


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j(jnt)} = 25^{\circ}C$; (2) $T_{j(jnt)} = 100^{\circ}C$

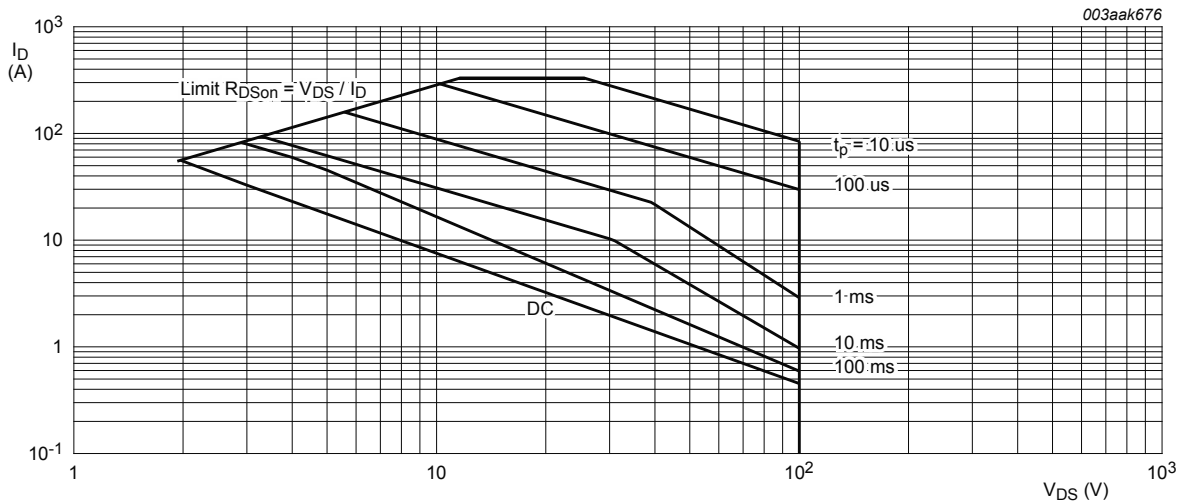


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.56	0.63	K/W

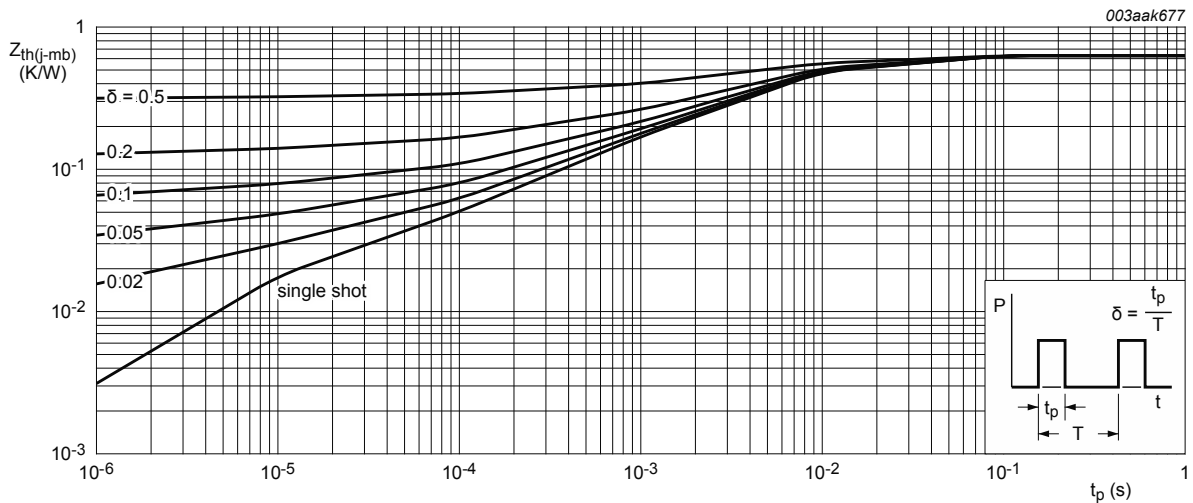


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_J = 25 ^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_J = -55 ^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_J = 25 ^\circ C$; Fig. 10 ; Fig. 11	2	3	4	V
V_{GSth}	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_J = 175 ^\circ C$; Fig. 11	1	-	-	V
		$I_D = 1 mA; V_{DS} = V_{GS}; T_J = -55 ^\circ C$; Fig. 11	-	-	4.6	V
I_{DSS}	drain leakage current	$V_{DS} = 100 V; V_{GS} = 0 V; T_J = 25 ^\circ C$	-	0.03	2	μA
		$V_{DS} = 100 V; V_{GS} = 0 V; T_J = 175 ^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 V; V_{DS} = 0 V; T_J = 25 ^\circ C$	-	10	100	nA
		$V_{GS} = 20 V; V_{DS} = 0 V; T_J = 25 ^\circ C$	-	10	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 20 A; T_J = 25 ^\circ C$; Fig. 12	-	11	13	mΩ
		$V_{GS} = 10 V; I_D = 20 A; T_J = 100 ^\circ C$; Fig. 12 ; Fig. 13	-	-	23	mΩ
		$V_{GS} = 10 V; I_D = 20 A; T_J = 175 ^\circ C$; Fig. 12 ; Fig. 13	-	-	36	mΩ
R_G	gate resistance	$f = 1 MHz$	0.33	0.66	1.32	Ω

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 20 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 14 ; Fig. 15		-	75	-	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V		-	60	-	nC
Q _{GS}	gate-source charge	I _D = 20 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 14 ; Fig. 15		-	16	-	nC
Q _{GD}	gate-drain charge			-	26	-	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 20 A; V _{DS} = 50 V; Fig. 14 ; Fig. 15		-	4.7	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 16		-	3775	-	pF
C _{oss}	output capacitance			-	265	-	pF
C _{rss}	reverse transfer capacitance			-	192	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 2.9 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω		-	16	-	ns
t _r	rise time			-	23	-	ns
t _{d(off)}	turn-off delay time			-	42	-	ns
t _f	fall time			-	21	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 20 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 17		-	0.82	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V		-	61	-	ns
Q _r	recovered charge			-	146	-	nC

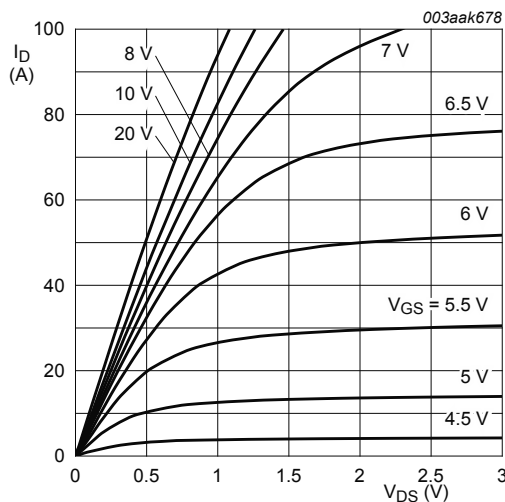


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25^\circ\text{C}$

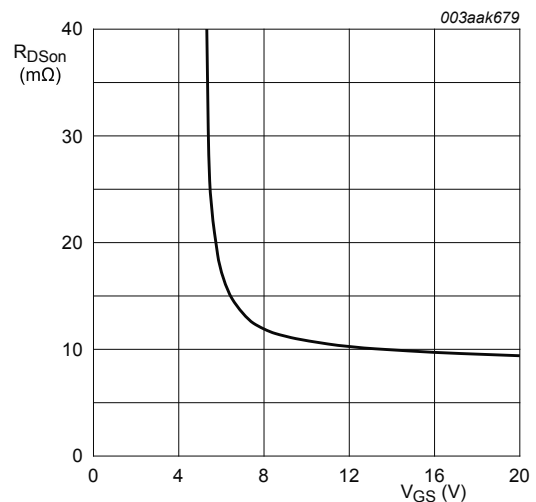


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ\text{C}$; $I_D = 20\text{ A}$

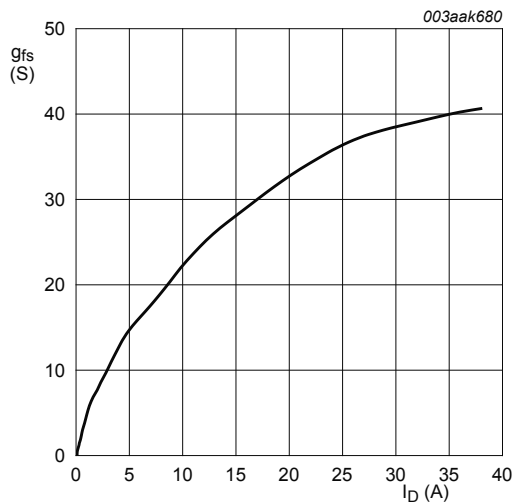


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25^\circ\text{C}; V_{DS} = 10\text{V}$

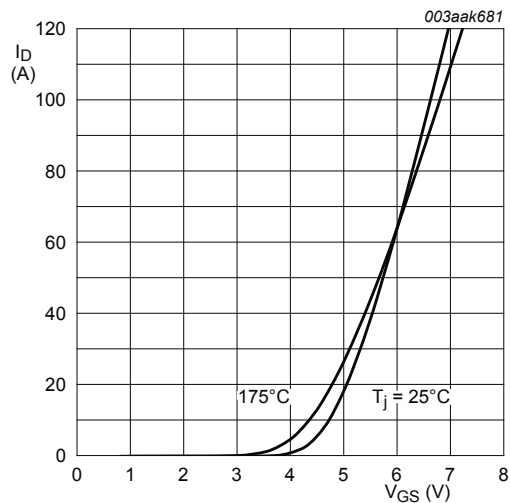


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{V}$

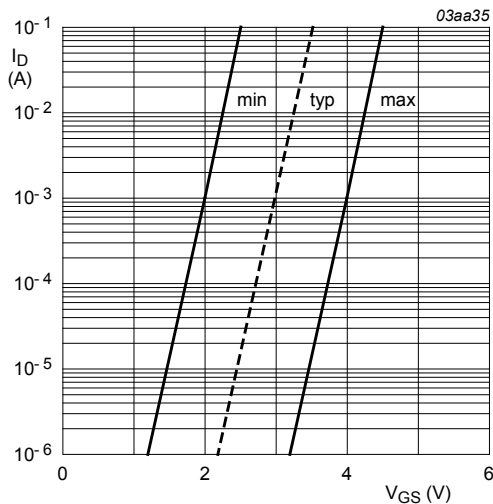


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

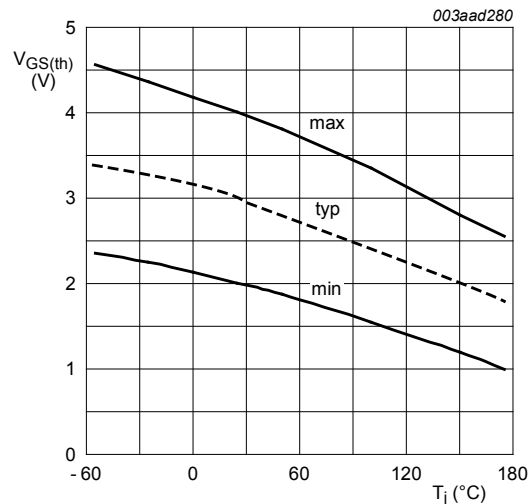


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

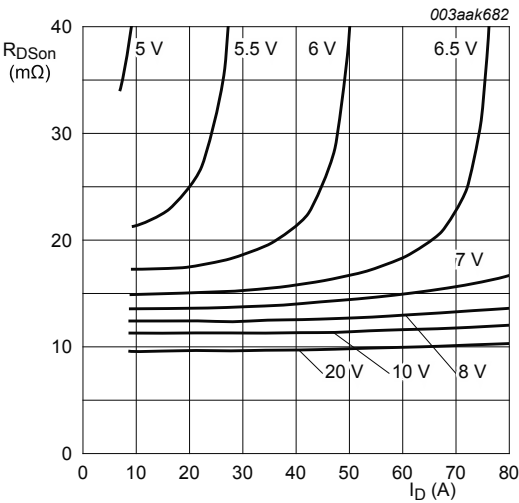


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^{\circ}\text{C}$$

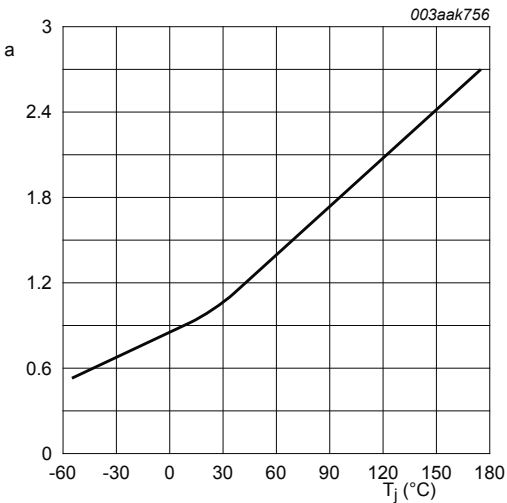


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^{\circ}\text{C})}$$

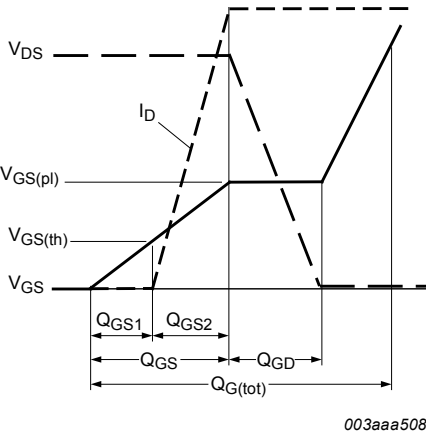


Fig. 14. Gate charge waveform definitions

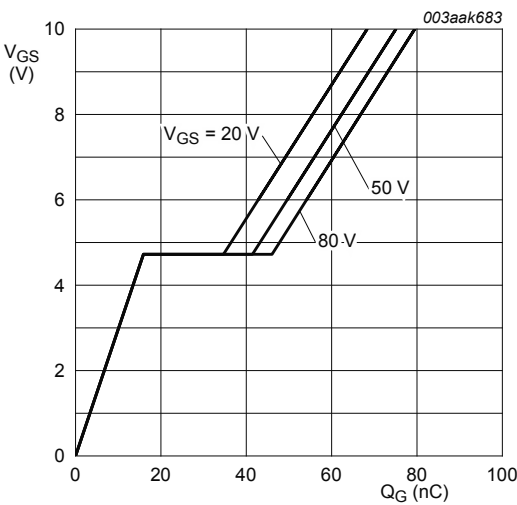


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^{\circ}\text{C}; I_D = 20\text{A}$$

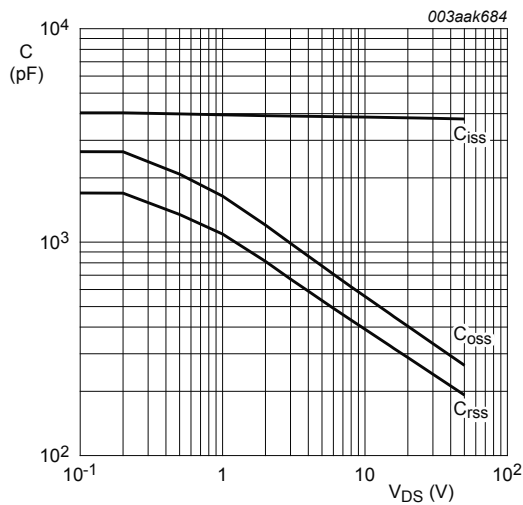


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS}=0V; f=1MHz$

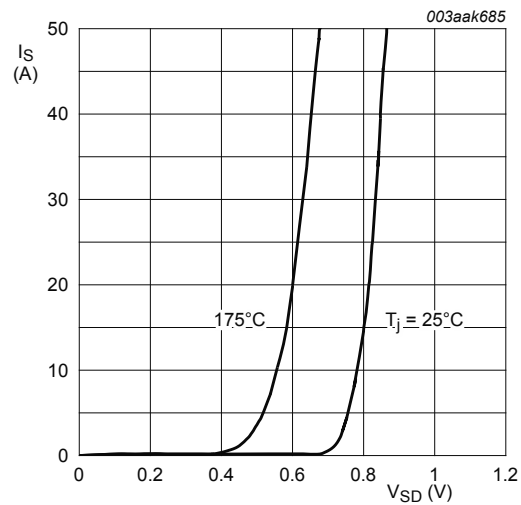


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS}=0V$

11. Package outline

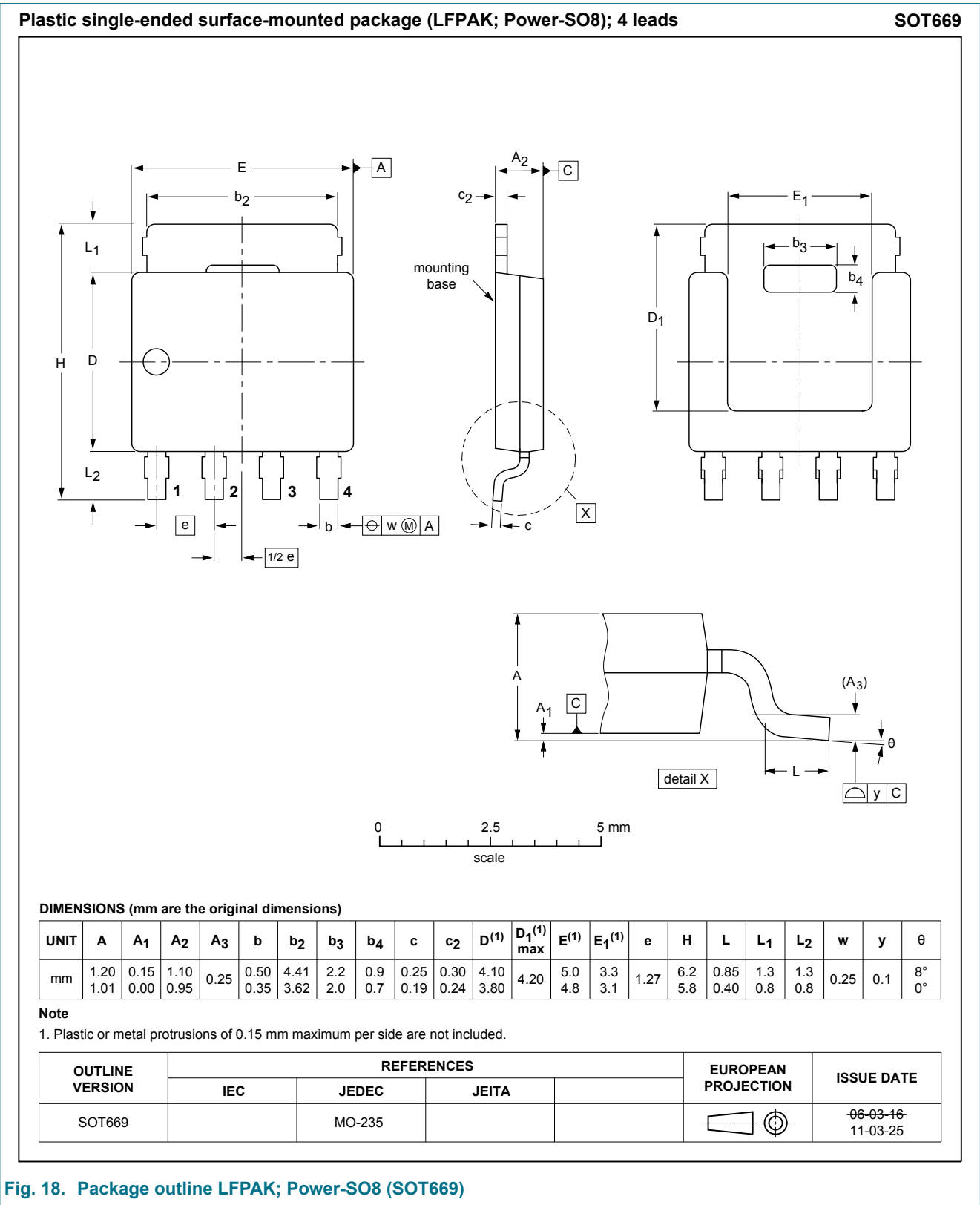


Fig. 18. Package outline LPAK; Power-SO8 (SOT669)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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