



PSMN3R3-80BS

N-channel 80 V, 3.5 mΩ standard level MOSFET in D2PAK

Rev. 2 — 29 February 2012

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in D2PAK package qualified to 175°C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive

1.3 Applications

- DC-to-DC converters
- Motor control
- Load switch
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

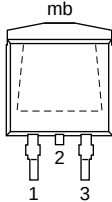
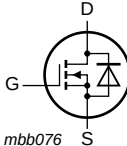
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	80	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1	[1]	-	120	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	-	306	W
T _j	junction temperature		-55	-	175	°C
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 13	-	3	3.5	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C; see Figure 12 ; see Figure 13	-	4.95	5.8	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = 10 V; I _D = 75 A; V _{DS} = 40 V; see Figure 14 ; see Figure 15	-	28	-	nC
Q _{G(tot)}	total gate charge		-	111	-	nC
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 120 A; V _{sup} ≤ 80 V; R _{GS} = 50 Ω; unclamped	-	-	676	mJ

[1] Continuous current is limited by package.



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	drain		

SOT404 (D2PAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN3R3-80BS	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

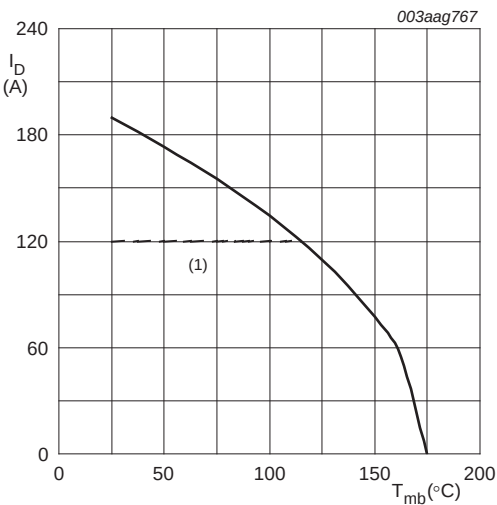
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

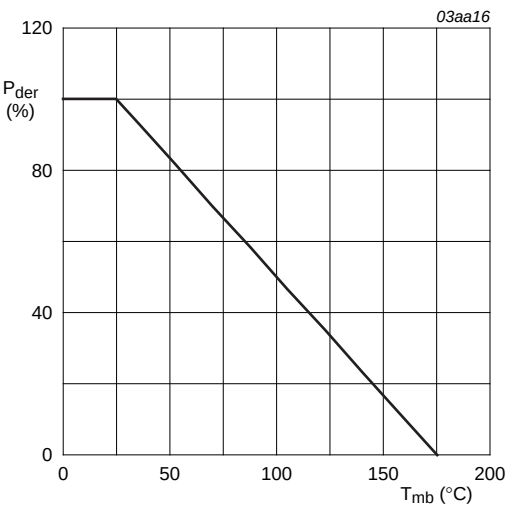
Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	80	V
V _{DGR}	drain-gate voltage	T _j ≥ 25 °C; T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	80	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; see Figure 1	[1] -	120	A
		V _{GS} = 10 V; T _{mb} = 25 °C; see Figure 1	[1] -	120	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; see Figure 3	-	760	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	306	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
T _{sld(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	[1] -	120	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	760	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 120 A; V _{sup} ≤ 80 V; R _{GS} = 50 Ω; unclamped	-	676	mJ

[1] Continuous current is limited by package.



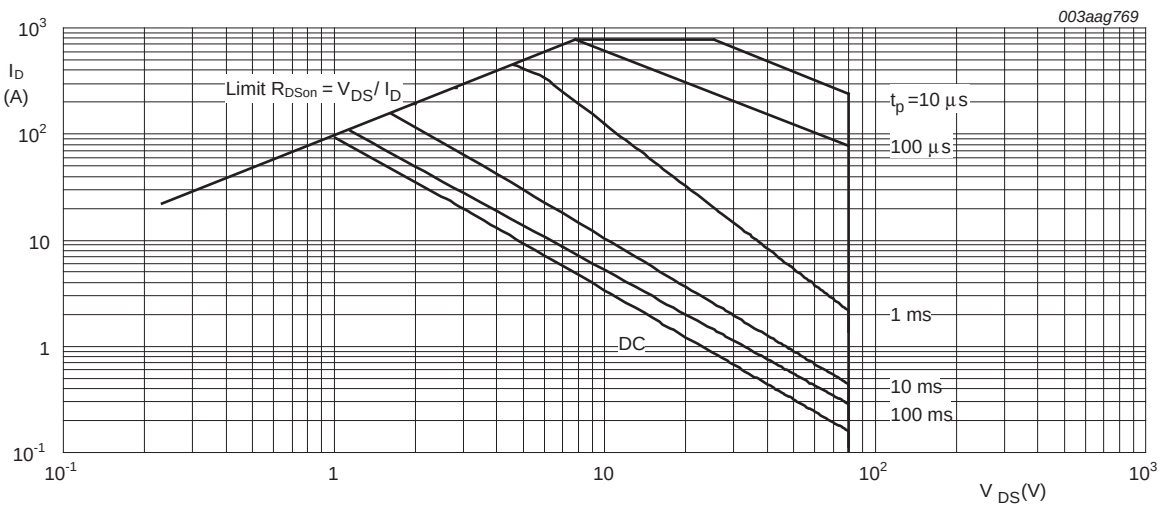
$V_{GS} \geq 10$ V; (1) Capped at 120 A due to package

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



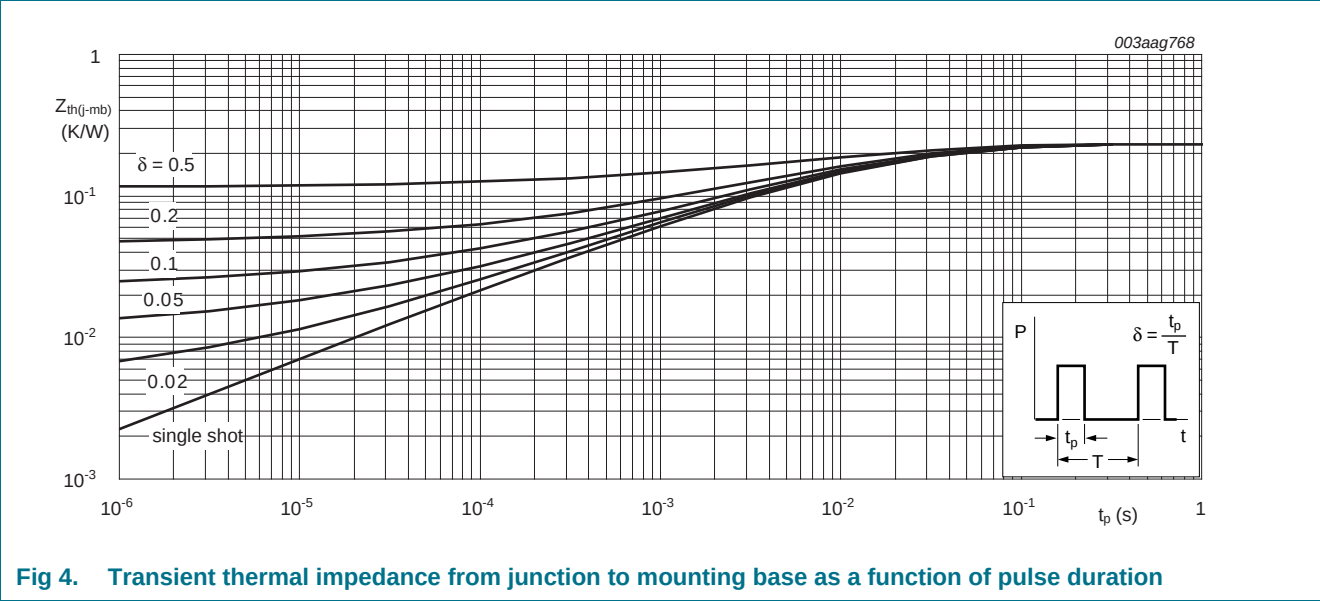
$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.22	0.49	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed circuit board	-	50	-	K/W



6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = -55\ ^\circ C$	73	-	-	V
		$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$	80	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_j = 175\ ^\circ C$; see Figure 10	1	-	-	V
		$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_j = -55\ ^\circ C$; see Figure 10	-	-	4.6	V
		$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_j = 25\ ^\circ C$; see Figure 10 ; see Figure 11	2	3	4	V
I_{DSS}	drain leakage current	$V_{DS} = 80\ V$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$	-	0.02	10	μA
		$V_{DS} = 80\ V$; $V_{GS} = 0\ V$; $T_j = 175\ ^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = -20\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	10	100	nA
		$V_{GS} = 20\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ V$; $I_D = 25\ A$; $T_j = 175\ ^\circ C$; see Figure 12 ; see Figure 13	-	7.1	8.4	mΩ
		$V_{GS} = 10\ V$; $I_D = 25\ A$; $T_j = 25\ ^\circ C$; see Figure 13	-	3	3.5	mΩ
		$V_{GS} = 10\ V$; $I_D = 25\ A$; $T_j = 100\ ^\circ C$; see Figure 12 ; see Figure 13	-	4.95	5.8	mΩ
R_G	internal gate resistance (AC)	$f = 1\ MHz$	-	0.9	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 0\ A$; $V_{DS} = 0\ V$; $V_{GS} = 10\ V$	-	104	-	nC
		$I_D = 75\ A$; $V_{DS} = 40\ V$; $V_{GS} = 10\ V$; see Figure 14 ; see Figure 15	-	111	-	nC
Q_{GS}	gate-source charge		-	38	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	24	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	14	-	nC
Q_{GD}	gate-drain charge		-	28	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 75\ A$; $V_{DS} = 40\ V$; see Figure 14 ; see Figure 15	-	6.1	-	V
C_{iss}	input capacitance	$V_{DS} = 40\ V$; $V_{GS} = 0\ V$; $f = 1\ MHz$;	-	8161	-	pF
C_{oss}	output capacitance	$T_j = 25\ ^\circ C$; see Figure 16	-	701	-	pF
C_{rss}	reverse transfer capacitance		-	337	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40\ V$; $R_L = 0.53\ \Omega$; $V_{GS} = 10\ V$;	-	38	-	ns
t_r	rise time	$R_{G(ext)} = 4.7\ \Omega$; $I_D = 75\ A$	-	29	-	ns
$t_{d(off)}$	turn-off delay time		-	94	-	ns
t_f	fall time		-	33	-	ns

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ °C}$; see Figure 17	-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = 100\text{ A/}\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	59	-	ns
Q_r	recovered charge	$V_{DS} = 20\text{ V}$	-	109	-	nC

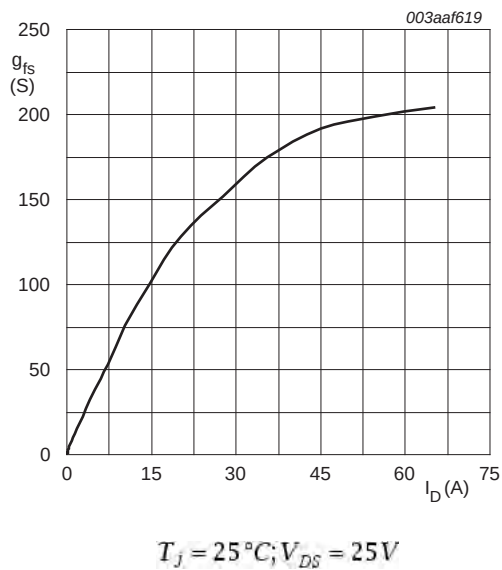


Fig 5. Forward transconductance as a function of drain current; typical values

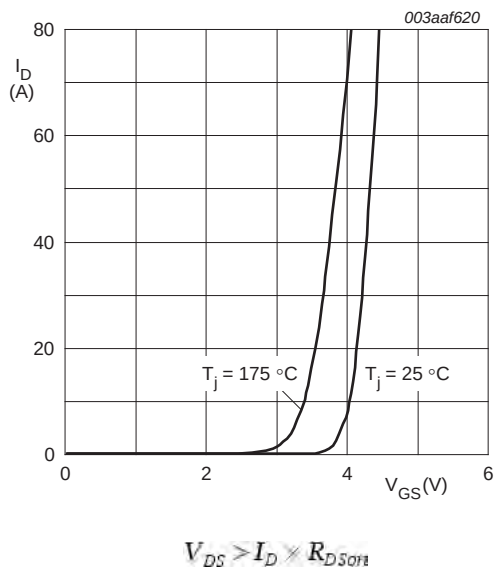


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

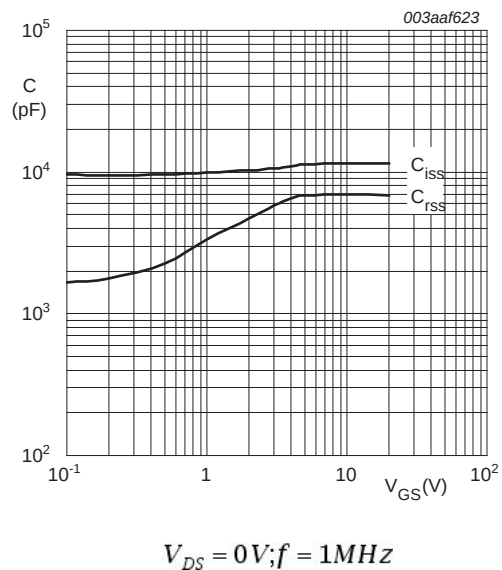


Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

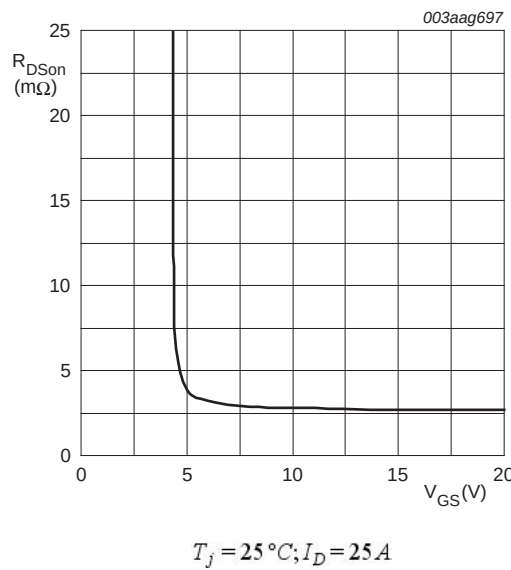


Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

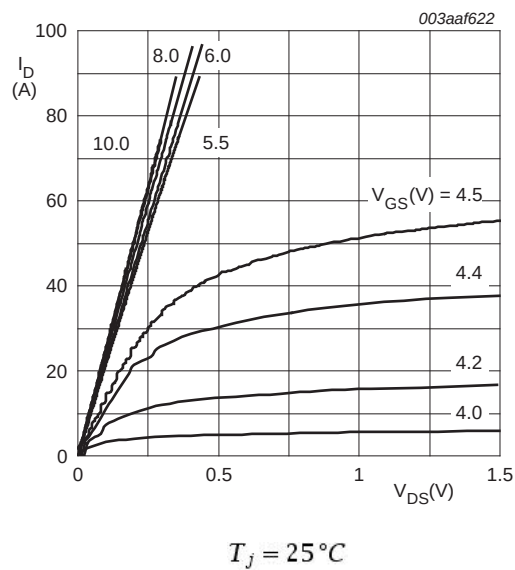


Fig 9. Output characteristics: drain current as a function of drain-source voltage; typical values

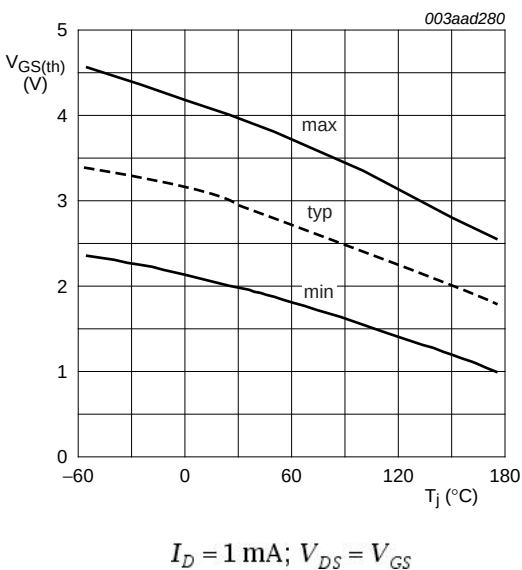


Fig 10. Gate-source threshold voltage as a function of junction temperature

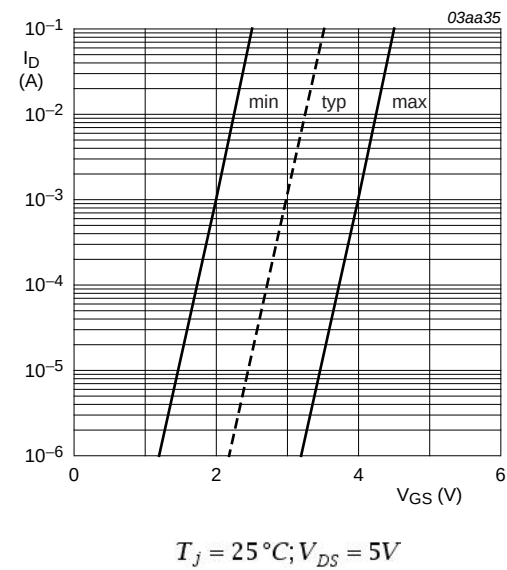


Fig 11. Sub-threshold drain current as a function of gate-source voltage

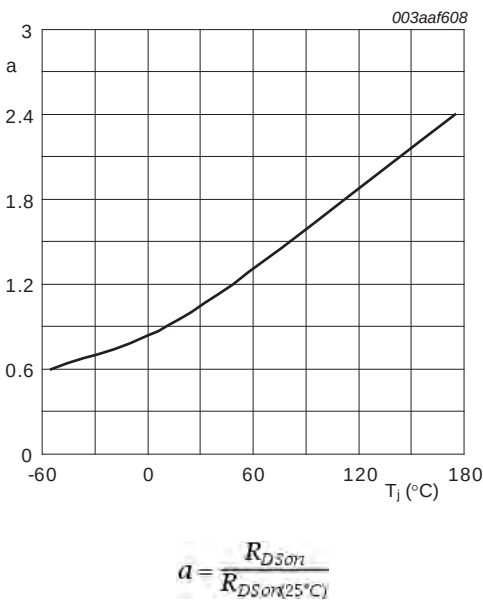
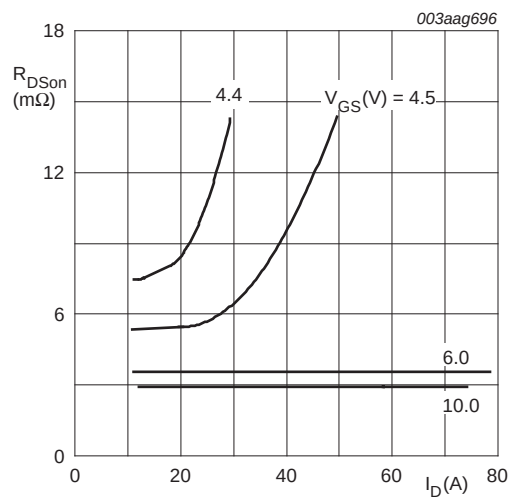


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^\circ\text{C}; I_D = 25\text{ A}$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values

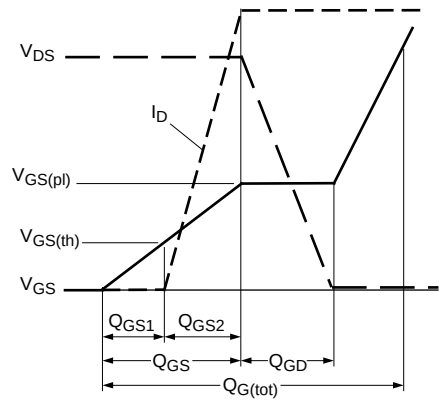
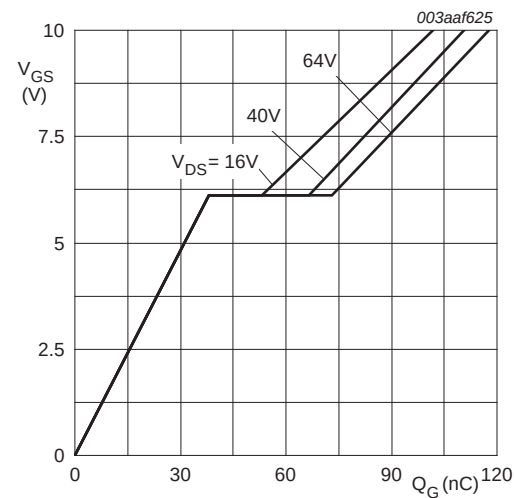
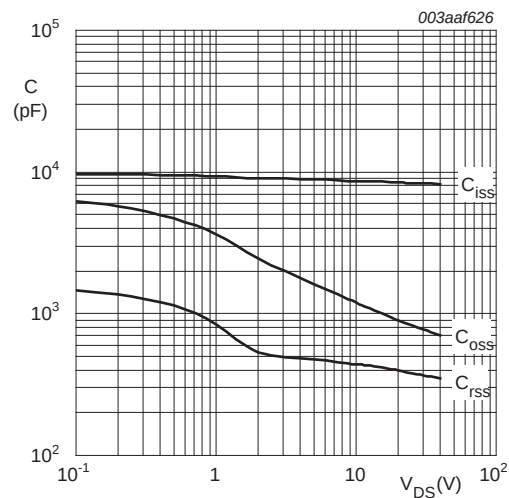


Fig 14. Gate charge waveform definitions



$I_D = 75\text{ A}$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

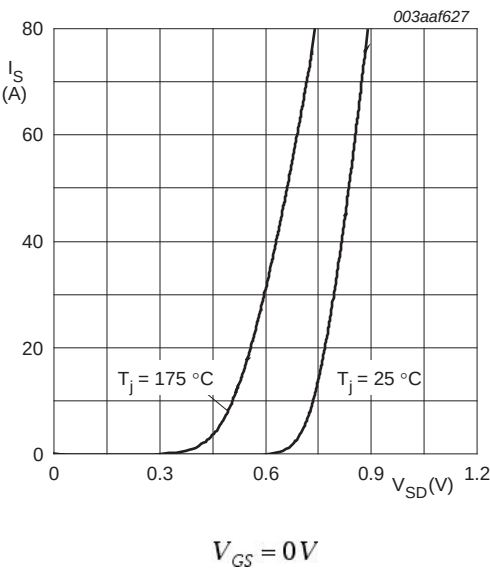


Fig 17. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

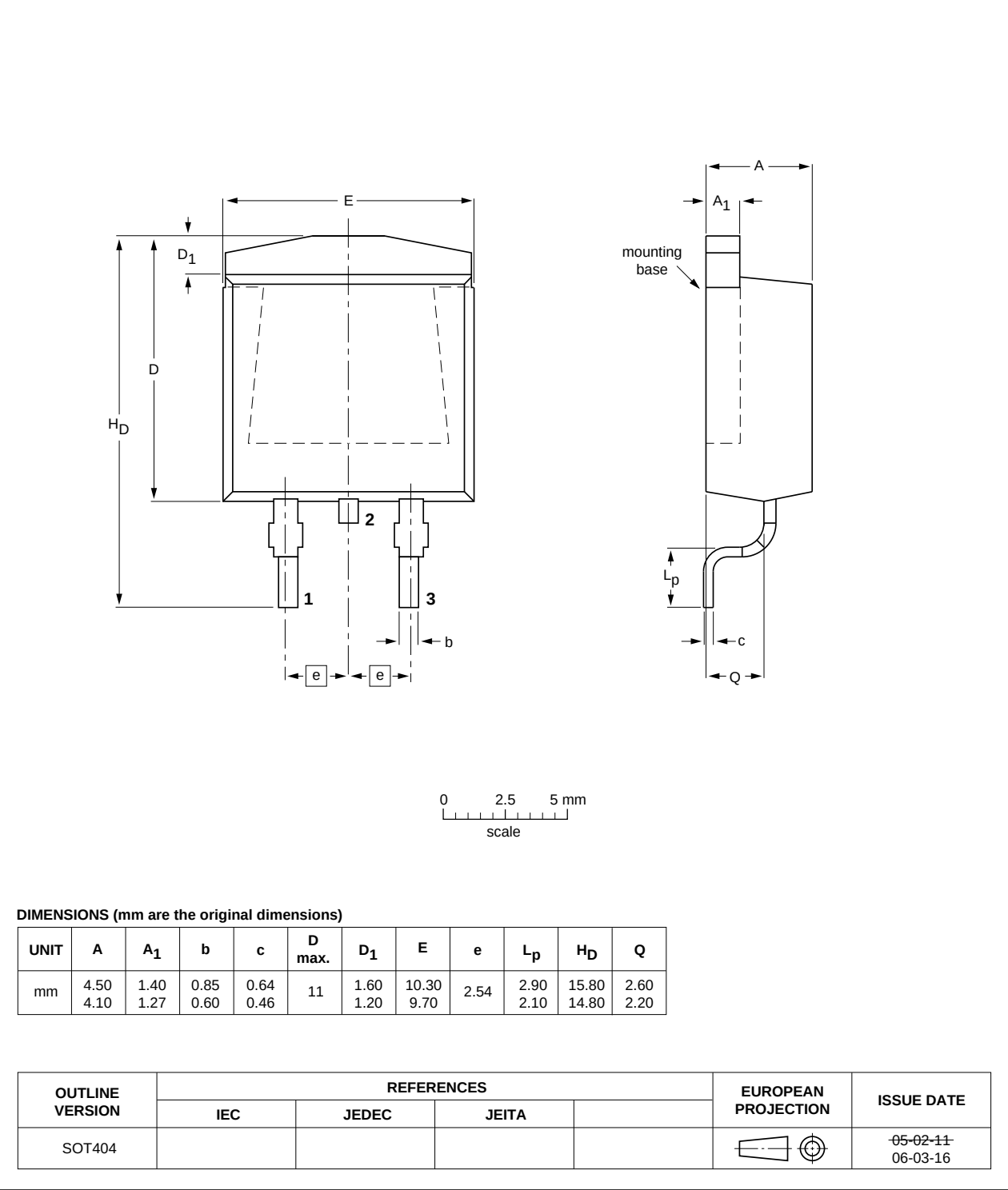


Fig 18. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN3R3-80BS v.2	20120229	Product data sheet	-	PSMN3R3-80BS v.1
Modifications:	• Status changed from objective to product. • Various changes to content.			
PSMN3R3-80BS v.1	20110928	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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