

2N3866 (SILICON)
2N3866A



SOLID STATE INC.

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CASE 79
 (TO-39)

Collector connected to case

NPN silicon transistor, designed for amplifier, frequency-multiplier, or oscillator applications in military and industrial equipment. Suitable for uses as output, driver, or pre-driver stages in VHF and UHF equipment.

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	55	Vdc
Emitter-Base Voltage	V_{EB}	3.5	Vdc
Collector Current	I_C	0.4	Amp
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	5.0 28.6	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Breakdown Voltage ($I_C = 5.0 \text{ mAdc}$, $R_{BE} = 10 \text{ ohms}$)	BV_{CER}	55	—	—	Vdc
Collector-Emitter Sustaining Voltage ($I_C = 5.0 \text{ mAdc}$, $I_B = 0$)	$BV_{CEO(sus)}$	30	—	—	Vdc
Collector-Base Breakdown Voltage ($I_E = 0$, $I_C = 0.1 \text{ mAdc}$)	BV_{CBO}	55	—	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 0.1 \text{ mAdc}$, $I_C = 0$)	BV_{EBO}	3.5	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 28 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	—	20	μA
Collector Cutoff Current ($V_{CE} = 55 \text{ Vdc}$, $V_{BE} = 1.5 \text{ Vdc}$)	I_{CEX}	—	—	100	μAdc

ON CHARACTERISTICS

DC Current Gain ($I_C = 0.36 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 0.05 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$) 2N3866 ($I_C = 50 \text{ mAdc}$, $V_{CE} = 5.0 \text{ Vdc}$) 2N3866A	h_{FE}	5.0 10 25	— — —	— 200 200	—
Collector-Emitter Saturation Voltage ($I_C = 100 \text{ mAdc}$, $I_B = 20 \text{ mAdc}$)	$V_{CE(sat)}$	—	—	1.0	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain — Bandwidth Product ($I_C = 50 \text{ mAdc}$, $V_{CE} = 15 \text{ Vdc}$, $f = 200 \text{ MHz}$) 2N3866 2N3866A	f_T	500 800	800 —	— —	MHz
Output Capacitance ($V_{CB} = 30 \text{ Vdc}$, $I_E = 0$, $f = 1.0 \text{ MHz}$)	C_{ob}	—	2.0	3.0	pF

FUNCTIONAL TEST

Power Gain	Test Circuit-Figure 1 $P_{in} = 0.1 \text{ W}$, $V_{CE} = 28 \text{ Vdc}$ $f = 400 \text{ MHz}$, $T_C = 25^\circ\text{C}$	G_{pe}	10	—	—	dB
Power Output		P_{out}	1.0	—	—	Watts
Collector Efficiency		η	45	—	—	%

2N3866, 2N3866A (continued)

FIGURE 1 — 400 MHz RF AMPLIFIER CIRCUIT FOR POWER-OUTPUT TEST

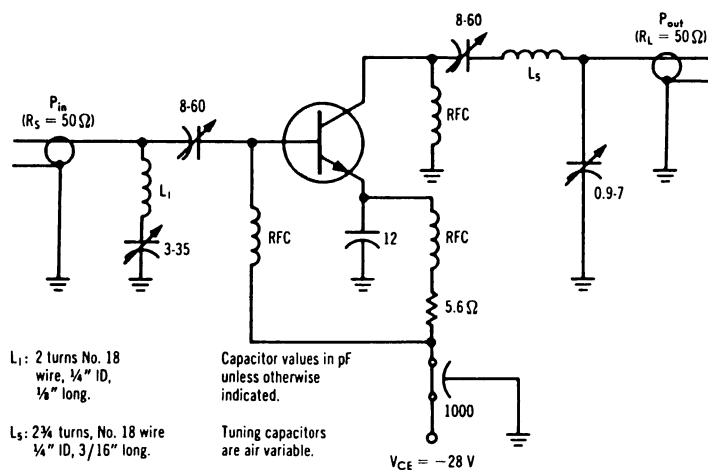


FIGURE 2 — POWER OUTPUT versus FREQUENCY (Class C)

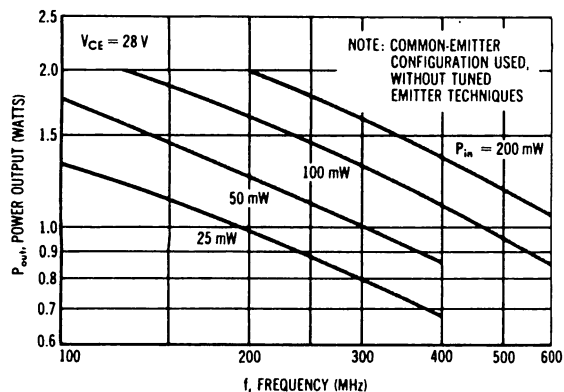


FIGURE 4 — PARALLEL INPUT RESISTANCE AND CAPACITANCE versus FREQUENCY (Class C)

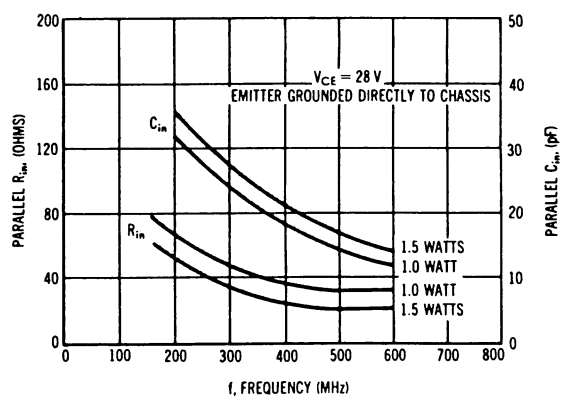


FIGURE 3 — POWER OUTPUT versus POWER INPUT (Class C)

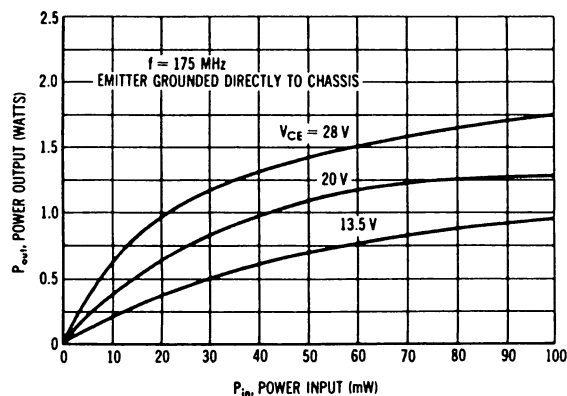


FIGURE 5 — PARALLEL OUTPUT CAPACITANCE versus FREQUENCY (Class C)

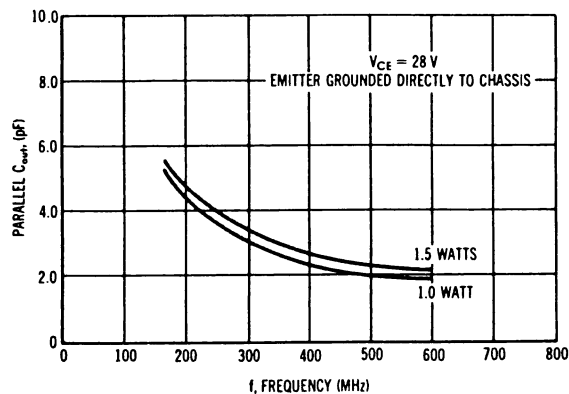


FIGURE 6 — SMALL-SIGNAL CURRENT GAIN
versus FREQUENCY

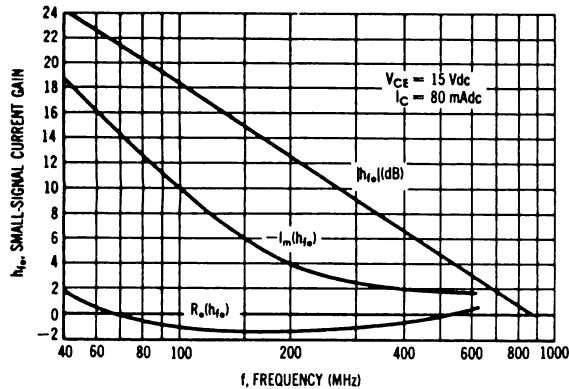


FIGURE 7 — OUTPUT CAPACITANCE
versus COLLECTOR VOLTAGE

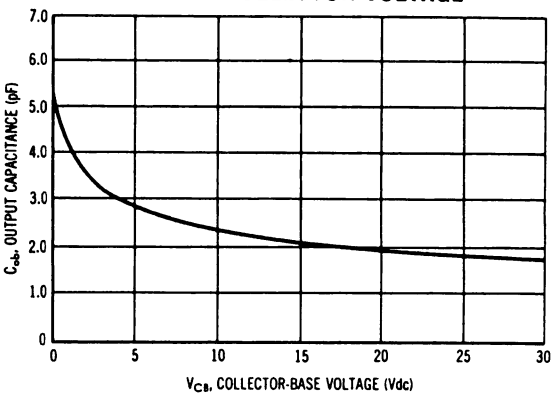


FIGURE 8 — f_T versus COLLECTOR CURRENT

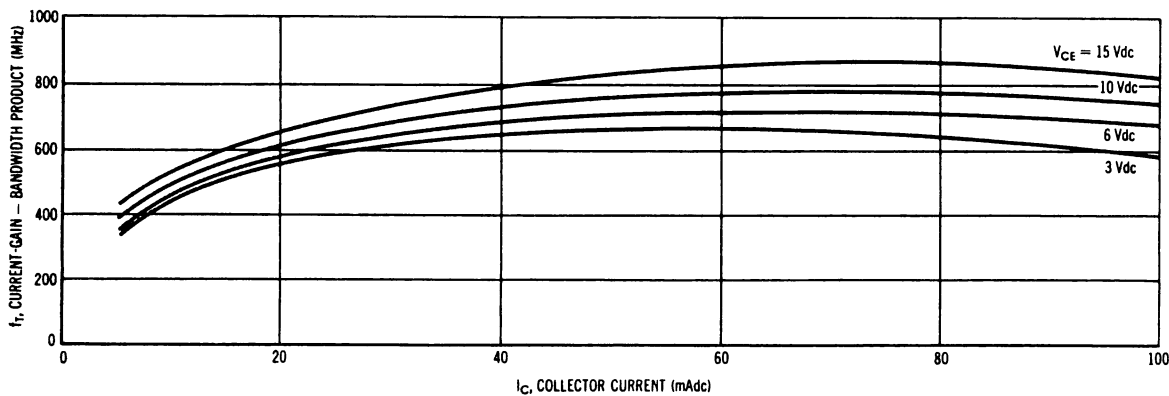


FIGURE 9 — $r_b' C_c$ versus COLLECTOR CURRENT

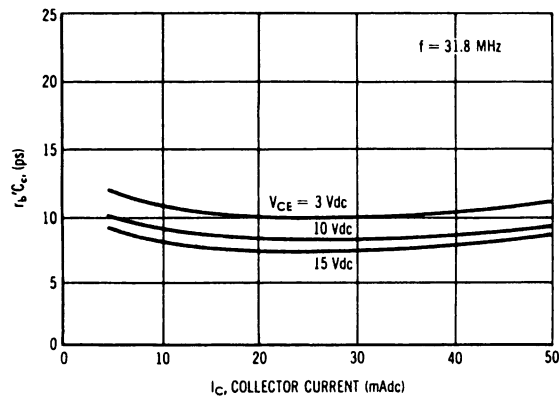
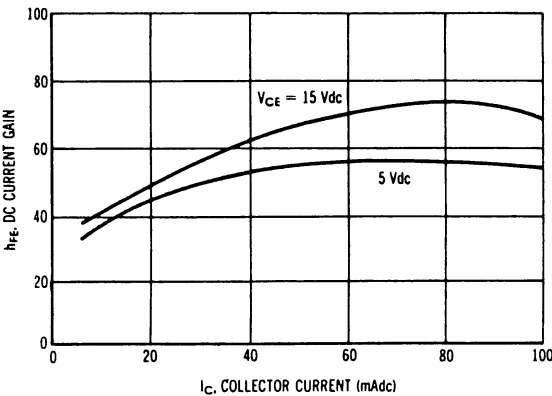


FIGURE 10 — DC CURRENT GAIN
versus COLLECTOR CURRENT



y PARAMETER VARIATIONS

FIGURE 11 — SMALL-SIGNAL INPUT ADMITTANCE versus COLLECTOR CURRENT

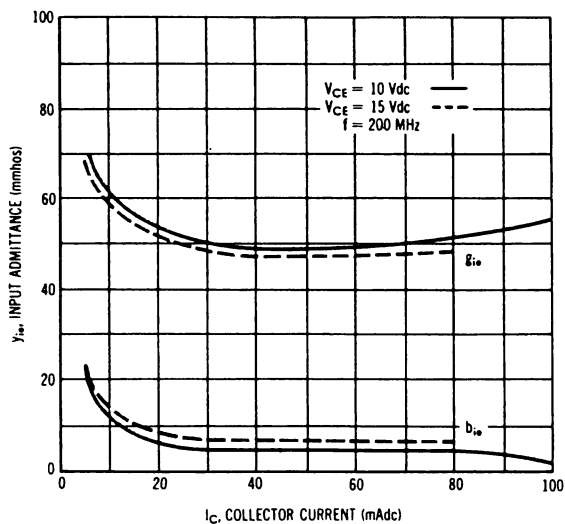


FIGURE 13 — SMALL-SIGNAL FORWARD TRANSFER ADMITTANCE versus COLLECTOR CURRENT

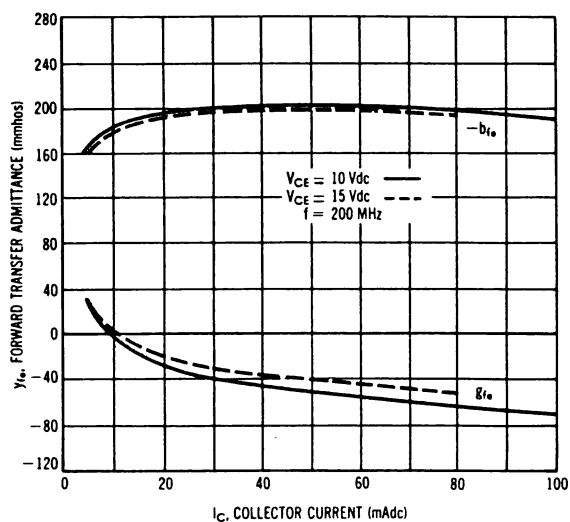


FIGURE 12 — SMALL-SIGNAL REVERSE TRANSFER ADMITTANCE versus COLLECTOR CURRENT

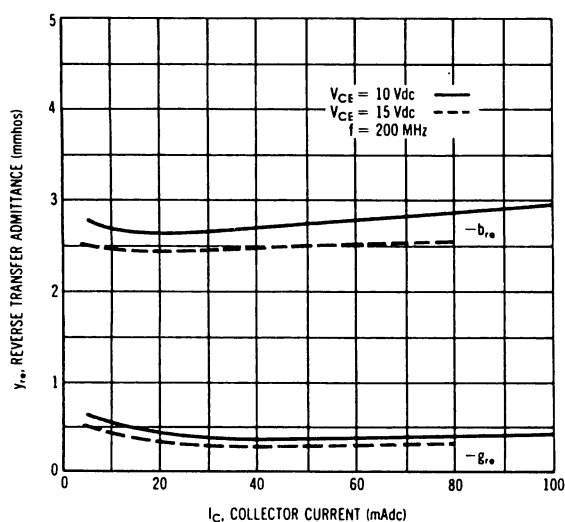
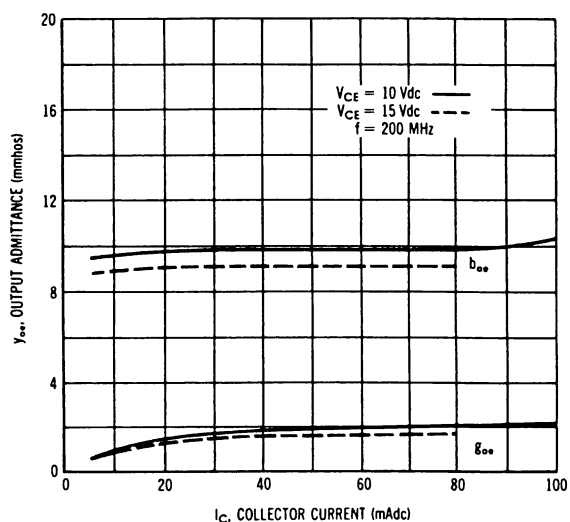


FIGURE 14 — SMALL-SIGNAL OUTPUT ADMITTANCE versus COLLECTOR CURRENT



DESIGN NOTE

Figures 11 through 18 show small-signal admittance-parameter data. This data can be used for Class A amplifier designs.

For Class C power-amplifier designs, the small-signal parameters are not applicable. Figures 4 and 5 give parallel output capacitance and the parallel input resistance and capacitance for Class C power-amplifier operation.

The parallel resistive portion of the collector load impedance for a power amplifier, R_L' , may be computed by assuming a peak voltage swing equal to V_{CC} , and using the expression

$$R_L' = \frac{V_{CC}^2}{2P}$$

where P = RF power output. The computed R_L' may then be combined with the data in Figures 2 and 3 to comprise complete device impedance data for Class C power amplifier design.

y PARAMETER VARIATIONS
($V_{CE} = 15$ Vdc, $I_C = 80$ mAdc, $T_A = 25^\circ\text{C}$)

FIGURE 15 — SMALL-SIGNAL INPUT ADMITTANCE versus FREQUENCY

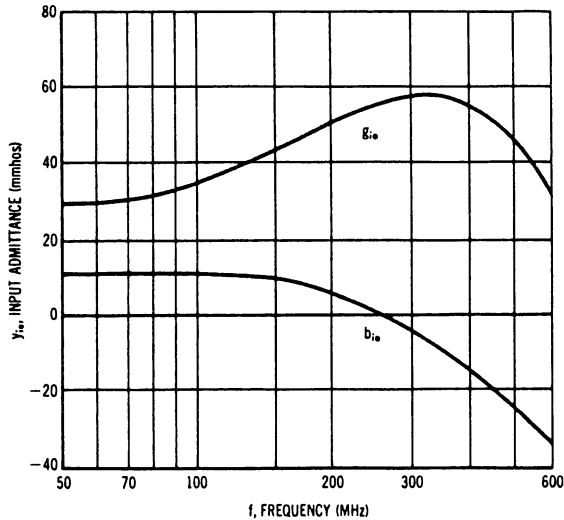


FIGURE 17 — SMALL-SIGNAL FORWARD TRANSFER ADMITTANCE versus FREQUENCY

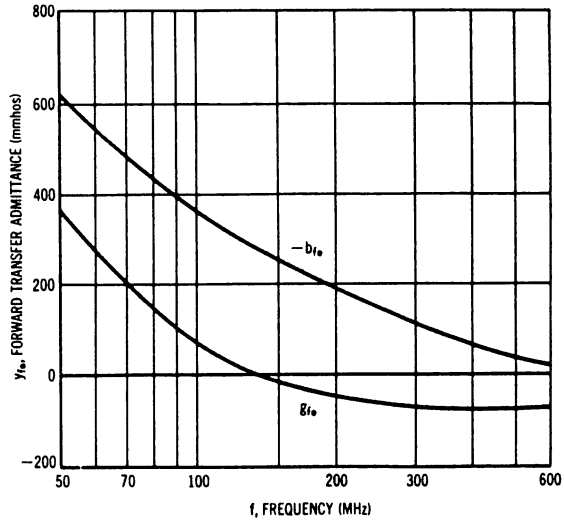


FIGURE 16 — SMALL-SIGNAL REVERSE TRANSFER ADMITTANCE versus FREQUENCY

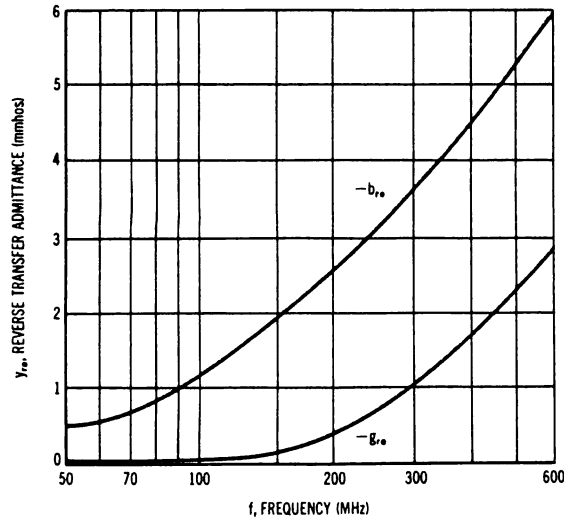
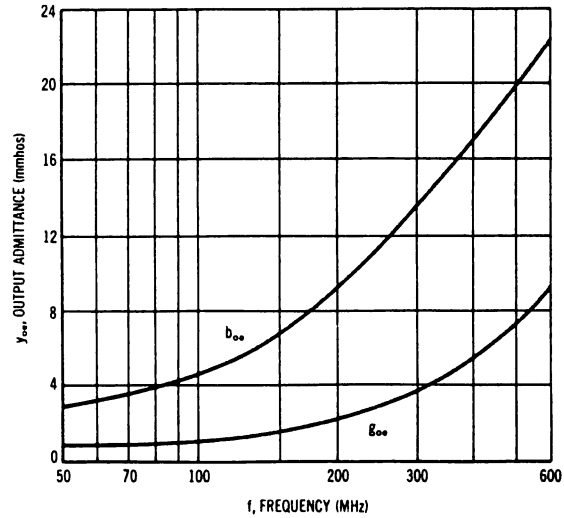
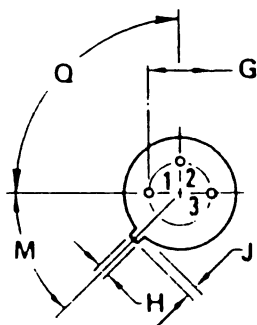
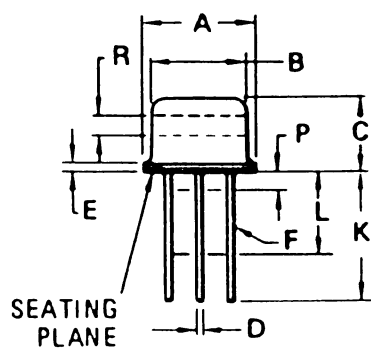


FIGURE 18 — SMALL-SIGNAL OUTPUT ADMITTANCE versus FREQUENCY





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	—	0.500	—
L	6.35	—	0.250	—
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
Q	90° NOM		90° NOM	
R	2.54	—	0.100	—

All JEDEC dimensions and notes apply.

STYLE 1

PIN 1. EMITTER

2. BASE

3. COLLECTOR

TO-39