

N-channel 600 V, 0.092 Ω typ., 31.5 A MDmesh™ II Power MOSFETs in a TO-247 package

Datasheet - production data

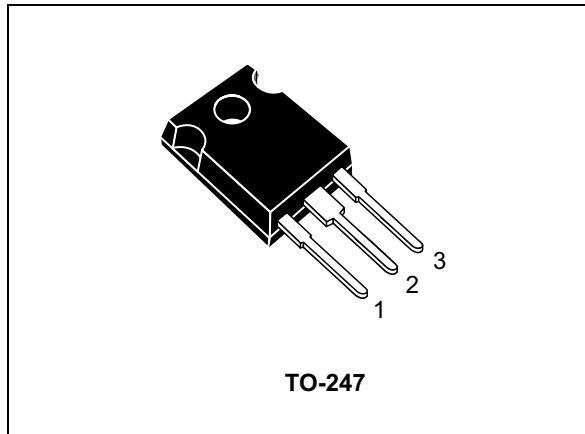
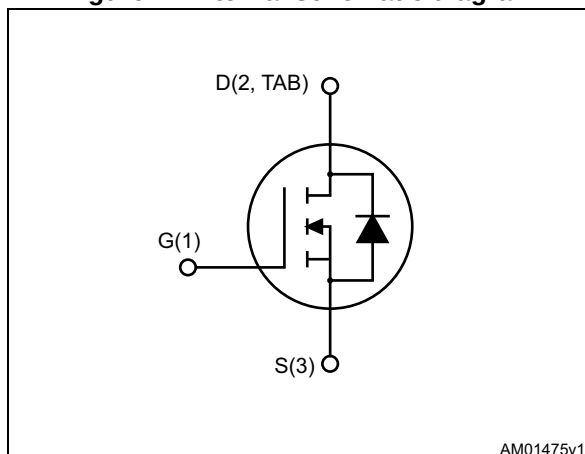


Figure 1. Internal schematic diagram



Features

Order code	V _{DSS}	R _{DS(on)}	I _D	P _{TOT}
STW34NM60N	600 V	0.105 Ω	31.5 A	250 W

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Packages	Packaging
STW34NM60N	34NM60N	TO-247	Tube

Contents

1 **Electrical ratings** 3

2 **Electrical characteristics** 4

 2.1 Electrical characteristics (curves) 6

3 **Test circuits** 8

4 **Package information** 9

 4.1 TO-247 package information 9

5 **Revision history** 11



1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	31.5	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	20	A
$I_{DM}^{(1)}$	Drain current (pulsed)	126	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	250	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{jmax})	7	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$)	345	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	-55 to 150	$^{\circ}\text{C}$
T_J	Max. operating junction temperature	150	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 31.5\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$
3. $V_{DS} \leq 480\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.5	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb max	50	

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 600\text{ V}$ $V_{DS} = 600\text{ V}$, $T_c = 125\text{ }^{\circ}\text{C}$			1 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 14.5\text{ A}$		0.092	0.105	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	2722	-	pF
C_{oss}	Output capacitance		-	173	-	pF
C_{rss}	Reverse transfer capacitance		-	1.75	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0$, $V_{DS} = 0\text{ to }480\text{ V}$	-	458	-	pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 15.75\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 19 and 14)	-	18	-	ns
t_r	Rise time		-	36	-	ns
$t_{d(off)}$	Turn-off delay time		-	104	-	ns
t_f	Fall time		-	73	-	ns
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 31.5\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 15)	-	84	-	nC
Q_{gs}	Gate-source charge		-	14	-	nC
Q_{gd}	Gate-drain charge		-	45	-	nC
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, gate DC Bias=0 test signal level=20 mV open drain	-	2.9	-	Ω

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		31.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		126	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 31.5 \text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 31.5 \text{ A}$, $V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$, (see Figure 16)	-	412		ns
Q_{rr}	Reverse recovery charge		-	8		μC
I_{RRM}	Reverse recovery current		-	39		A
t_{rr}	Reverse recovery time	$I_{SD} = 31.5 \text{ A}$, $V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 150 \text{ }^\circ\text{C}$ (see Figure 16)	-	490		ns
Q_{rr}	Reverse recovery charge		-	10		μC
I_{RRM}	Reverse recovery current		-	43		A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

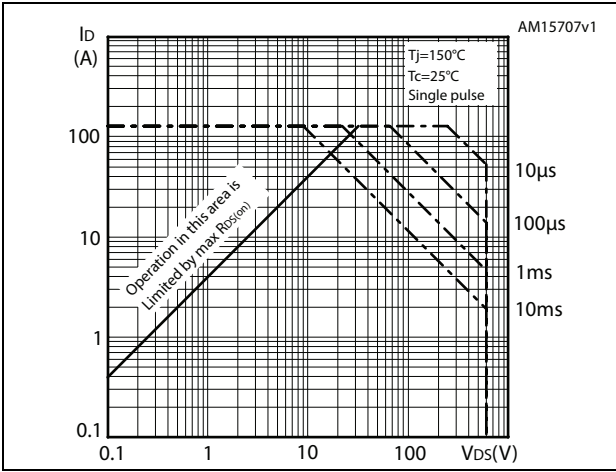


Figure 3. Thermal impedance

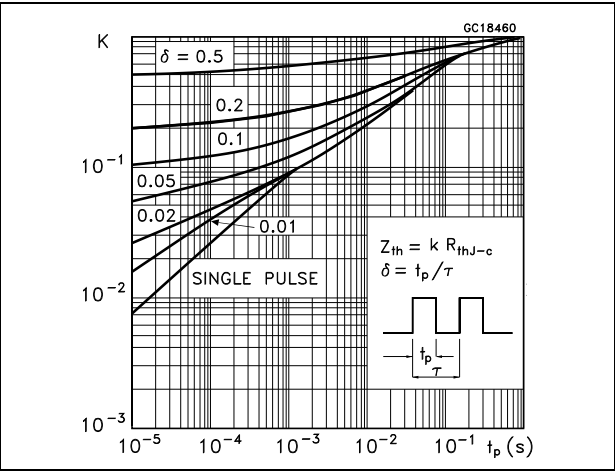


Figure 4. Output characteristics

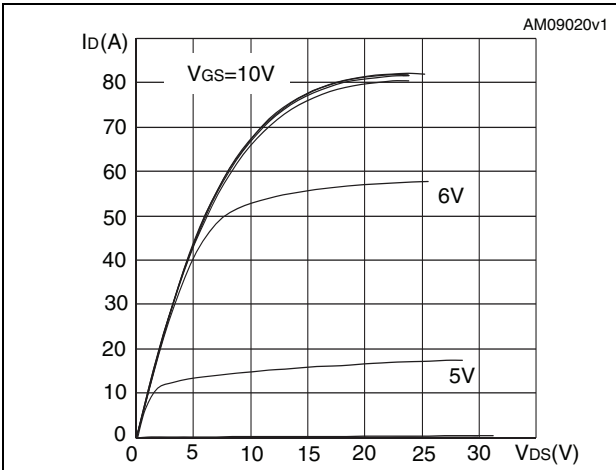


Figure 5. Transfer characteristics

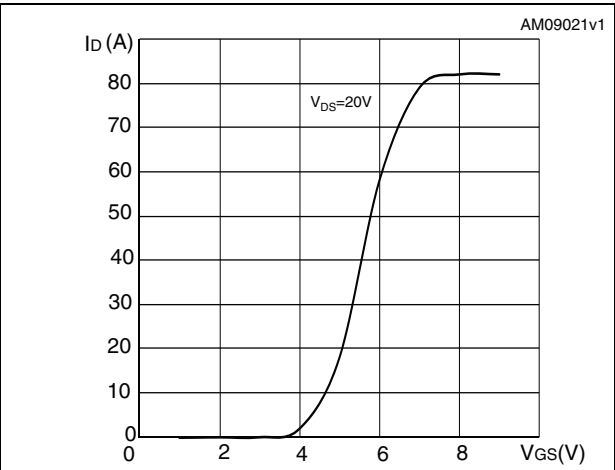


Figure 6. Gate charge vs gate-source voltage

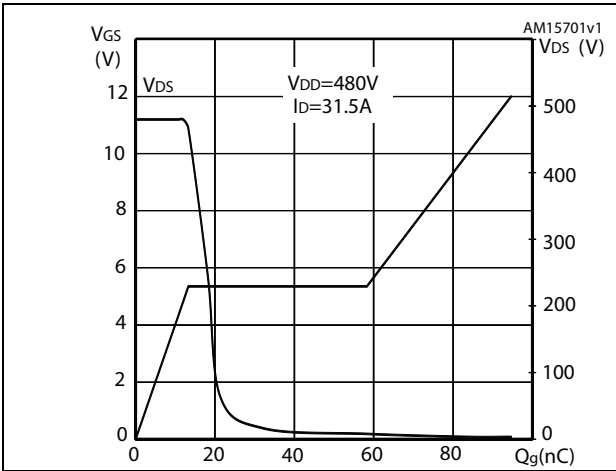


Figure 7. Static drain-source on-resistance

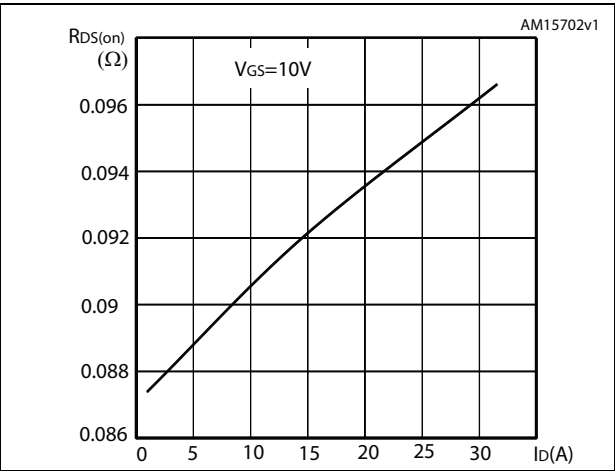


Figure 8. Capacitance variations

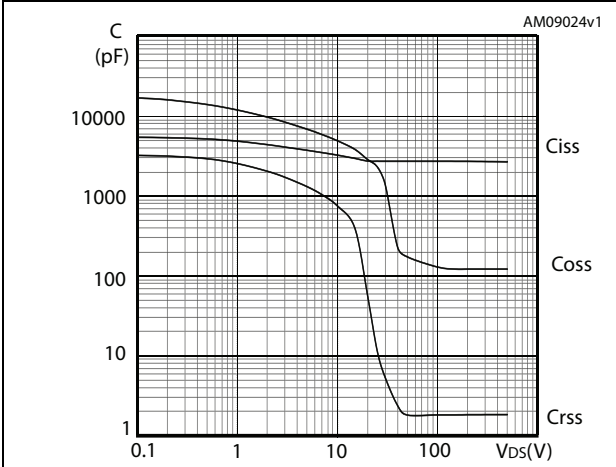


Figure 9. Output capacitance stored energy

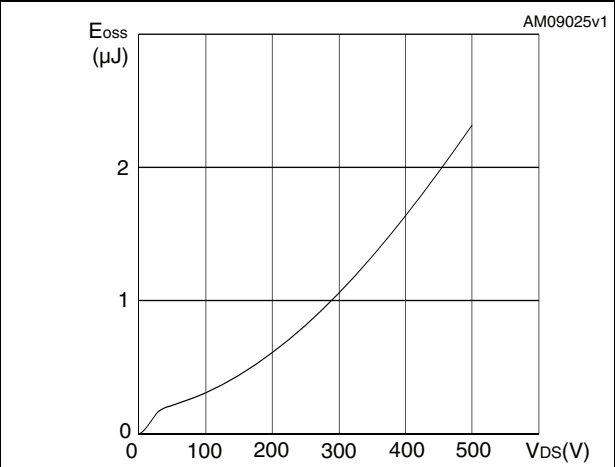


Figure 10. Normalized gate threshold voltage vs temperature

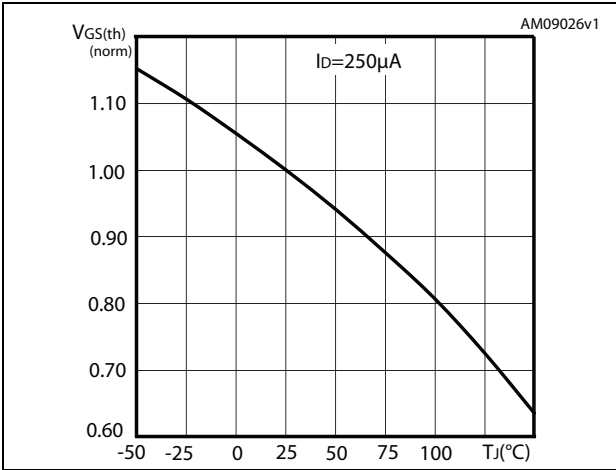


Figure 11. Normalized on-resistance vs temperature

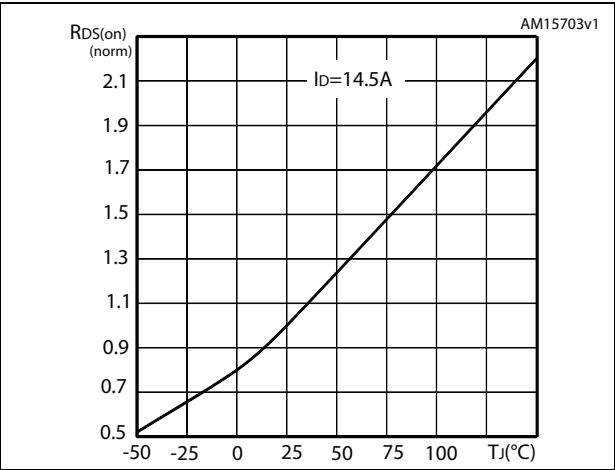


Figure 12. Normalized BVDSS vs temperature

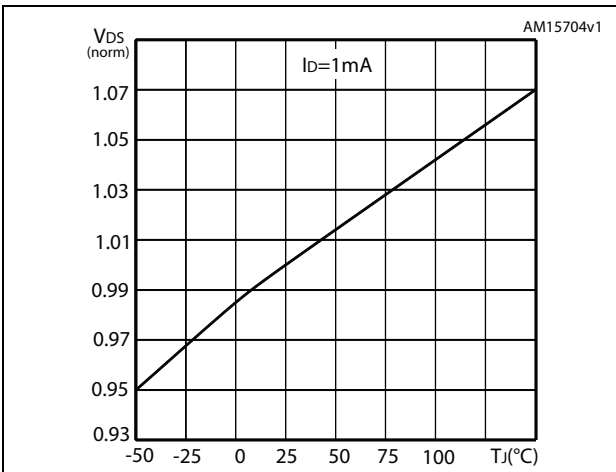
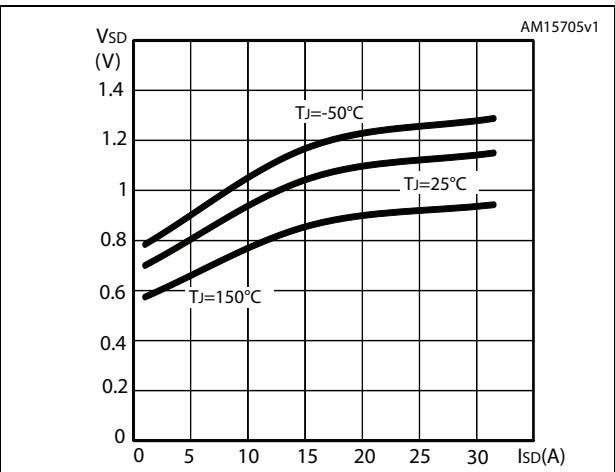


Figure 13. Source-drain diode forward characteristics



3 Test circuits

Figure 14. Switching times test circuit for resistive load

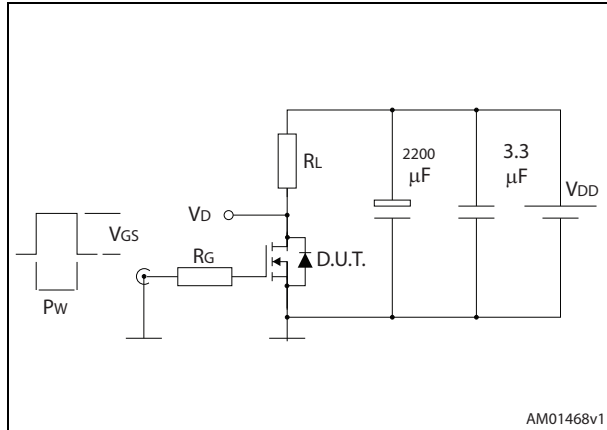


Figure 15. Gate charge test circuit

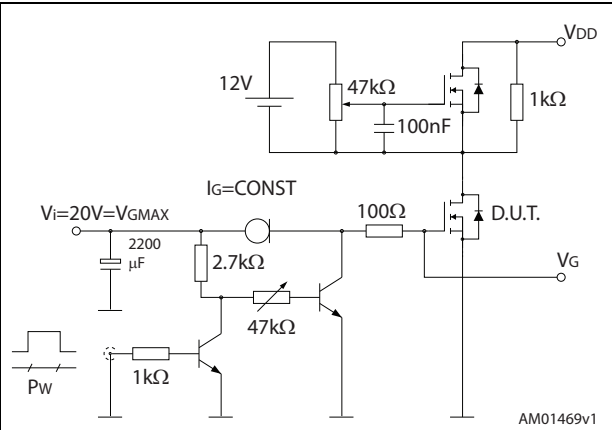


Figure 16. Test circuit for inductive load switching and diode recovery times

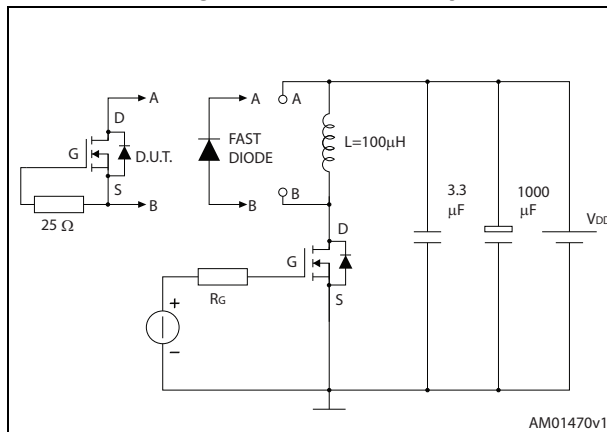


Figure 17. Unclamped inductive load test circuit

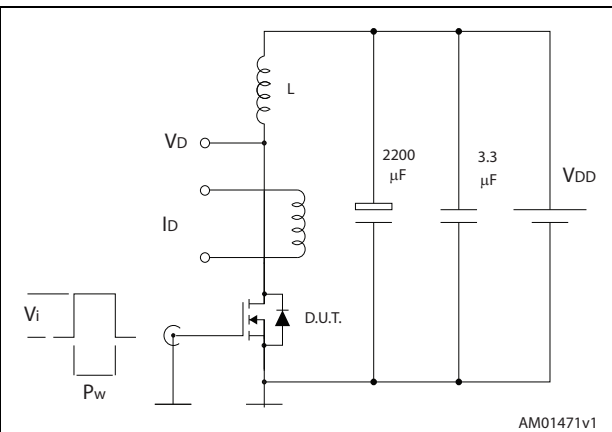


Figure 18. Unclamped inductive waveform

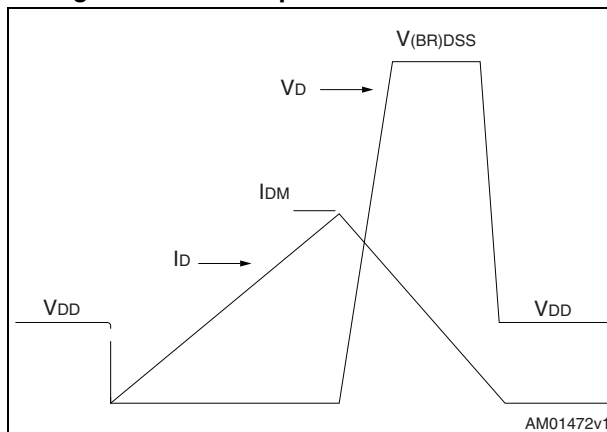
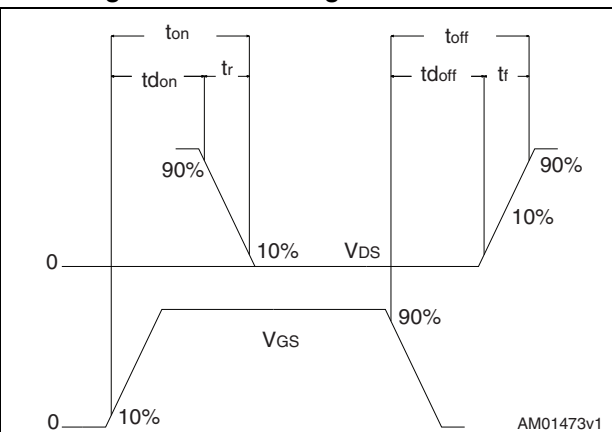


Figure 19. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-247 package information

Figure 20. TO-247 drawing

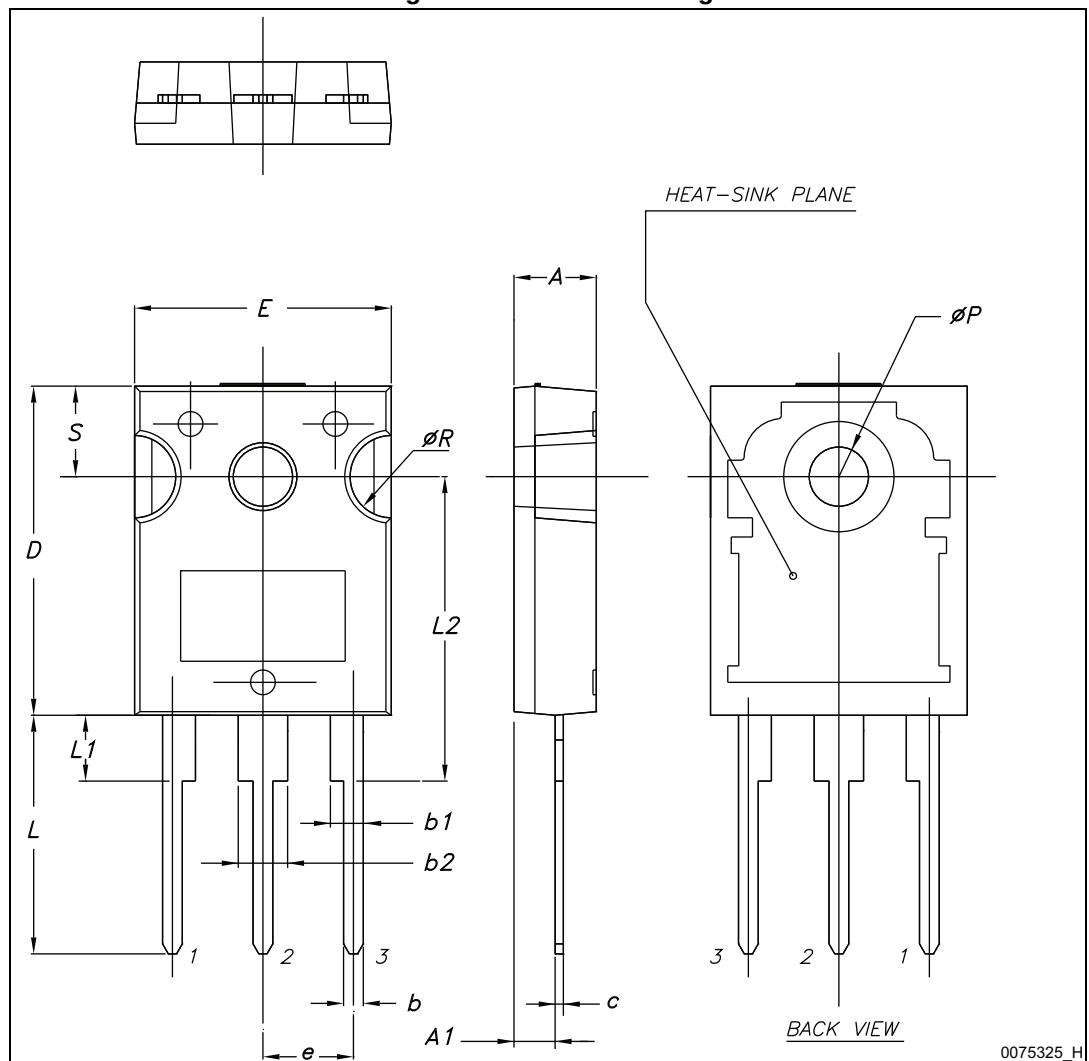


Table 7. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 8. Document revision history

Date	Revision	Changes
25-Mar-2015	1	Initial release.
30-Mar-2015	2	Updated <i>Figure 2: Safe operating area</i> and <i>Figure 3: Thermal impedance</i> .

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved