

IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

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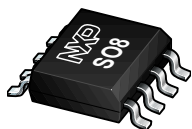
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Thank you for your cooperation and understanding,

WeEn Semiconductors



ACT102H-600D

AC Thyristor power switch

20 August 2014

Product data sheet

1. General description

An AC Thyristor power switch with very high noise immunity and over-voltage protection configured for negative gate triggering in a SOT96-1 (SO8) small surface-mountable plastic package

2. Features and benefits

- Exclusive negative gate triggering
- Full cycle AC conduction
- High noise immunity
- Remote gate separates the gate driver from the effects of the load current
- Surface-mountable package
- Very sensitive gate for lowest gate trigger current
- Safe clamping of low energy over-voltage transients
- Self-protective turn-on during high energy voltage transients

3. Applications

- Fan motor circuits
- Pump motor circuits
- Lower-power highly inductive, resistive and safety loads

4. Quick reference data

Table 1. Quick reference data

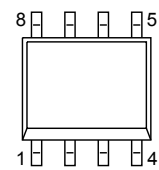
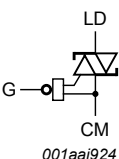
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	600	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{\text{J}(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 20\text{ ms}$; Fig. 3 ; Fig. 4	-	-	8	A
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{amb}} \leq 100\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2	-	-	0.2	A
V_{PP}	peak pulse voltage	$T_{\text{J}} \leq 25\text{ }^{\circ}\text{C}$; non-repetitive, off-state; Fig. 5	-	-	2	kV
Static characteristics						
I_{GT}	gate trigger current	$V_{\text{D}} = 12\text{ V}$; $I_{\text{T}} = 100\text{ mA}$; LD+ G-; $T_{\text{J}} = 25\text{ }^{\circ}\text{C}$; Fig. 7	0.5	-	5	mA



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	0.5	-	5	mA
V_{CL}	clamping voltage	$I_{CL} = 0.1\text{ mA}$; $t_p = 1\text{ ms}$; $T_j \leq 125\text{ }^\circ\text{C}$	650	-	-	V

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	n.c.	not connected	 SO8 (SOT96-1)	 001aa 924
2	LD	Load		
3	n.c.	not connected		
4	n.c.	not connected		
5	G	Gate		
6	CM	Common		
7	CM	Common		
8	n.c.	not connected		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
ACT102H-600D	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	600	V
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{amb}} \leq 100\text{ °C}$; Fig. 1 ; Fig. 2	-	0.2	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{\text{j(init)}} = 25\text{ °C}$; $t_{\text{p}} = 16.7\text{ ms}$	-	8.8	A
		full sine wave; $T_{\text{j(init)}} = 25\text{ °C}$; $t_{\text{p}} = 20\text{ ms}$; Fig. 3 ; Fig. 4	-	8	A
I^2t	I^2t for fusing	$t_{\text{p}} = 10\text{ ms}$; SIN	-	0.31	A^2s
di_{T}/dt	rate of rise of on-state current	$I_{\text{T}} = 1\text{ A}$; $I_{\text{G}} = 20\text{ mA}$; $di_{\text{G}}/dt = 0.2\text{ A}/\mu\text{s}$	-	50	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current	$t = 20\text{ }\mu\text{s}$	-	1	A
P_{GM}	peak gate power		-	2	W
$P_{\text{G(AV)}}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	150	$^{\circ}\text{C}$
T_{j}	junction temperature		-	125	$^{\circ}\text{C}$
V_{PP}	peak pulse voltage	$T_{\text{j}} \leq 25\text{ °C}$; non-repetitive, off-state; Fig. 5	-	2	kV

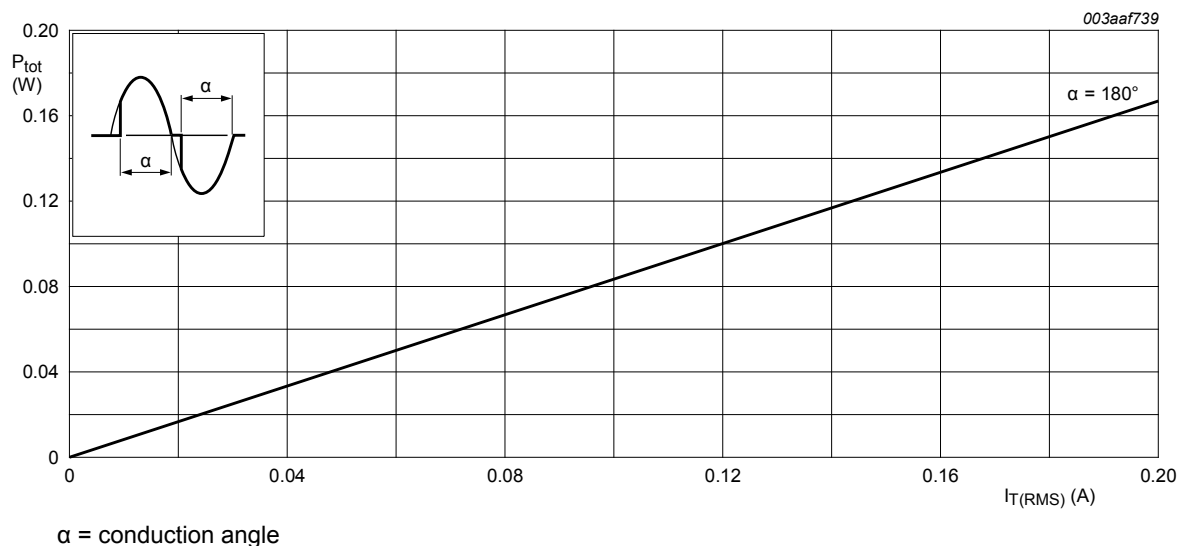


Fig. 1. Total power dissipation as a function of RMS on-state current; maximum values

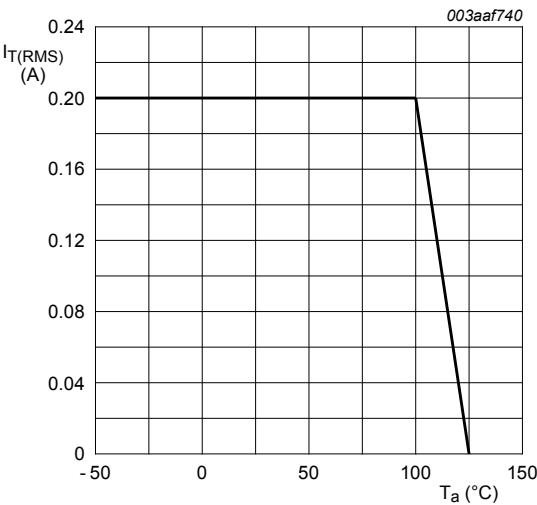


Fig. 2. RMS on-state current as a function of solder point temperature; maximum values

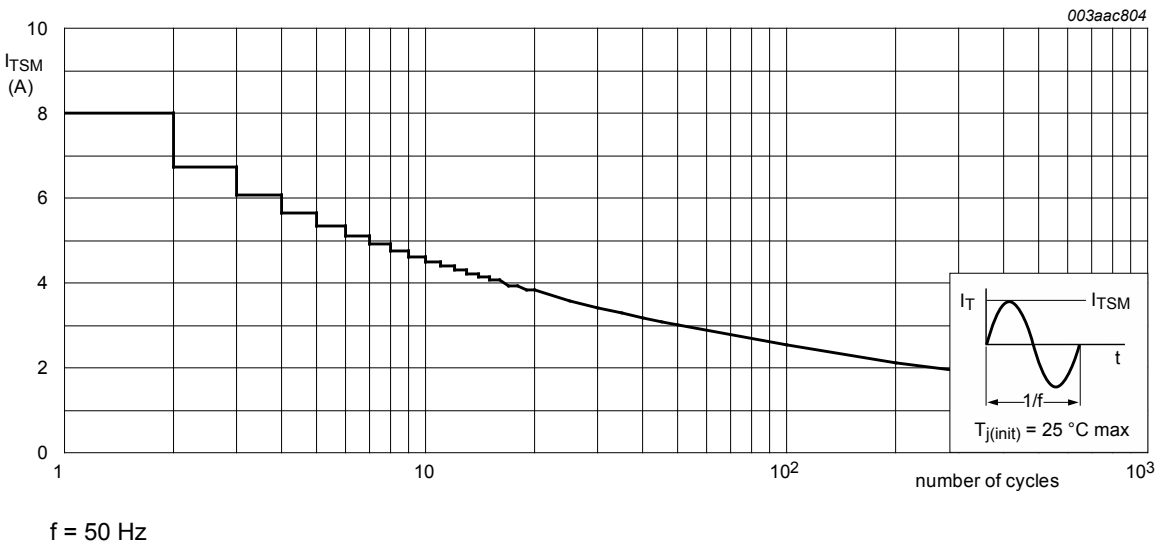


Fig. 3. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

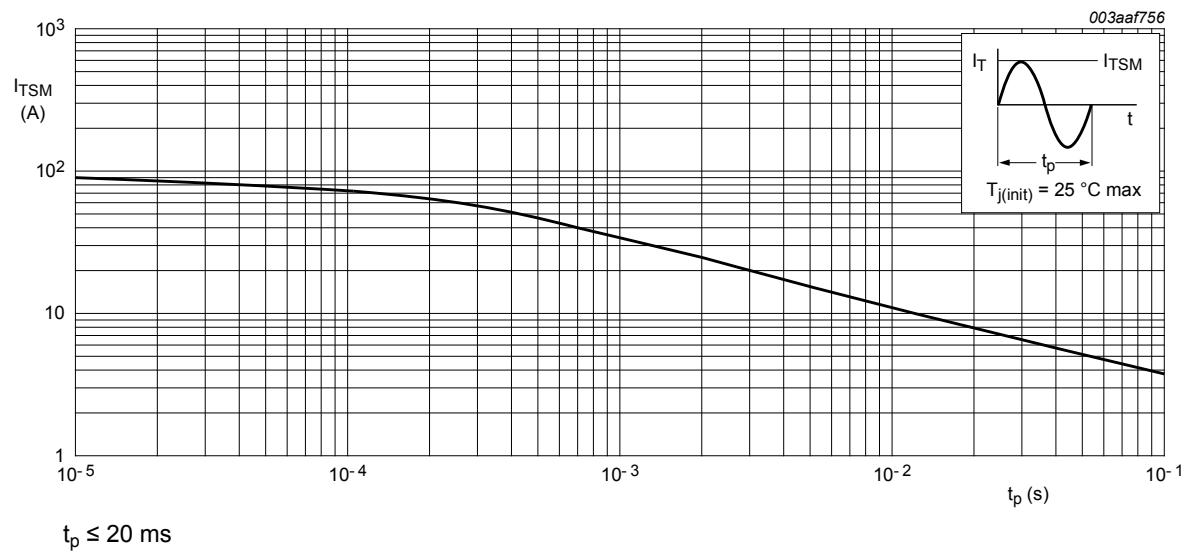


Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values

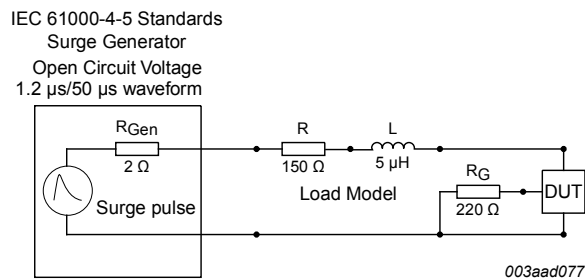
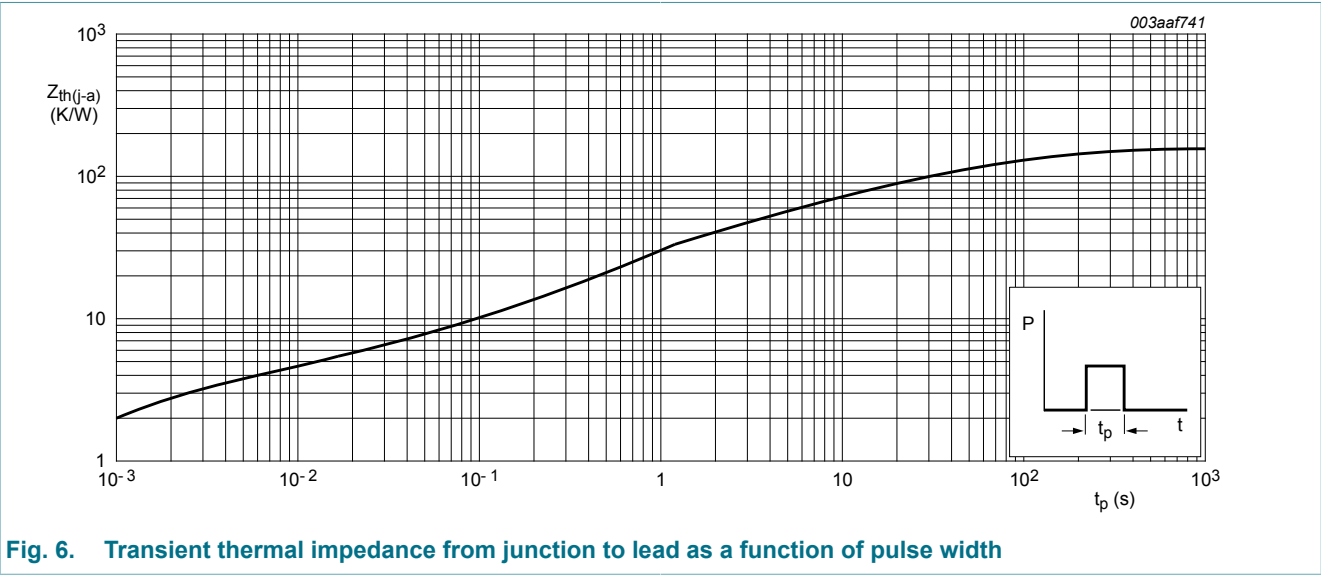


Fig. 5. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

8. Thermal characteristics

Table 5. Thermal characteristics

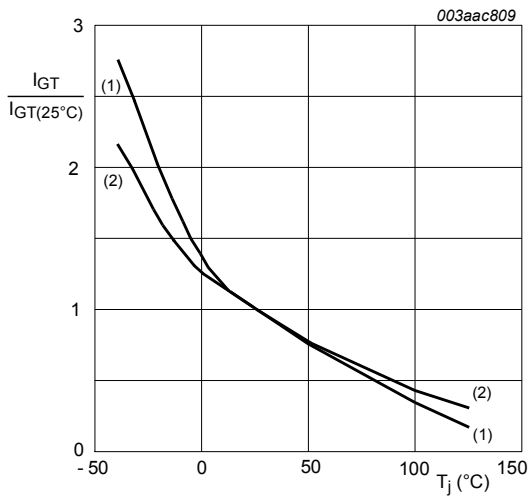
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	full cycle; Fig. 6		-	150	-	K/W



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ °C}$; Fig. 7	0.5	-	5	mA
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD- G-; $T_j = 25\text{ °C}$; Fig. 7	0.5	-	5	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ °C}$; Fig. 8	-	-	25	mA
		$V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD- G-; $T_j = 25\text{ °C}$; Fig. 8	-	-	25	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 9	-	-	20	mA
V_T	on-state voltage	$I_T = 0.3\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10	-	-	1.2	V
V_{GT}	gate trigger voltage	$V_D = 400\text{ V}$; $I_T = 100\text{ mA}$; $T_j = 125\text{ °C}$	0.15	-	-	V
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; $T_j = 25\text{ °C}$	-	-	0.9	V
I_D	off-state current	$V_D = 600\text{ V}$; $T_j = 25\text{ °C}$	-	-	2	μA
		$V_D = 600\text{ V}$; $T_j = 125\text{ °C}$	-	-	0.2	mA
V_{CL}	clamping voltage	$I_{CL} = 0.1\text{ mA}$; $t_p = 1\text{ ms}$; $T_j \leq 125\text{ °C}$	650	-	-	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit; Fig. 11	300	-	-	V/ μs
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}$; $T_j = 125\text{ °C}$; $I_{T(RMS)} = 1\text{ A}$; $dV_{com}/dt = 15\text{ V}/\mu\text{s}$; gate open circuit; Fig. 12 ; Fig. 13	0.15	-	-	A/ms



(1) LD+ G-
(2) LD- G-

Fig. 7. Normalized gate trigger current as a function of junction temperature

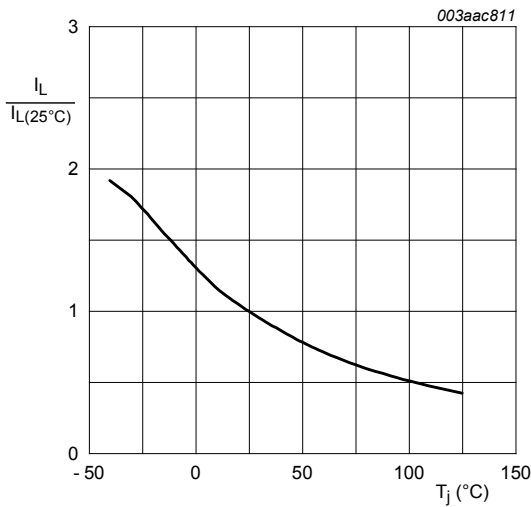


Fig. 8. Normalized latching current as a function of junction temperature

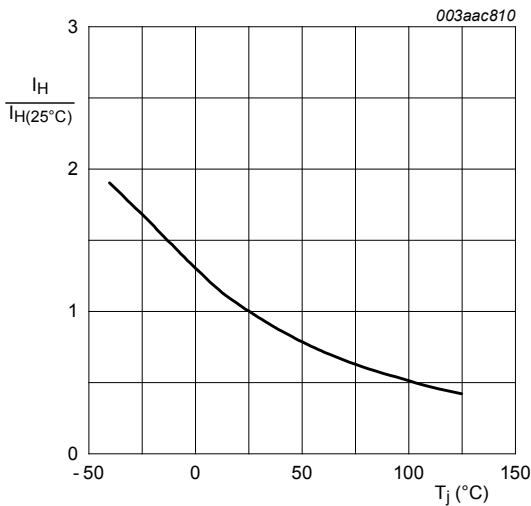
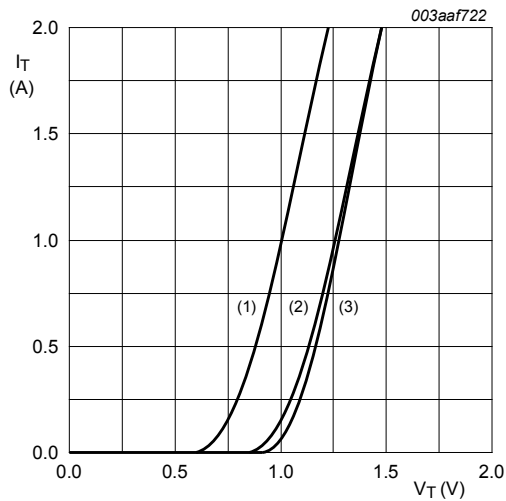
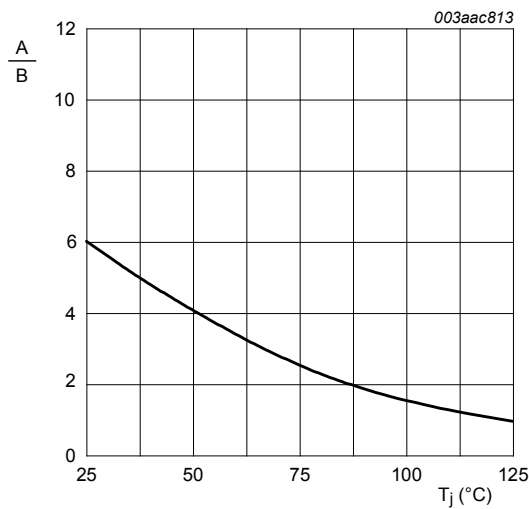


Fig. 9. Normalized holding current as a function of junction temperature



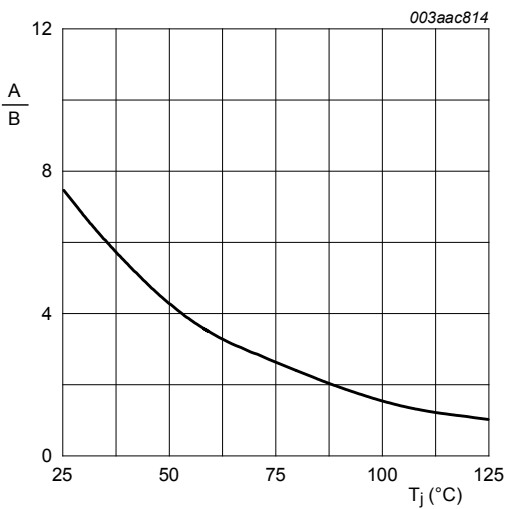
$V_o = 0.758\text{ V}$; $R_s = 0.263\ \Omega$
(1) $T_j = 125^\circ\text{C}$; typical values
(2) $T_j = 125^\circ\text{C}$; maximum values
(3) $T_j = 25^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage



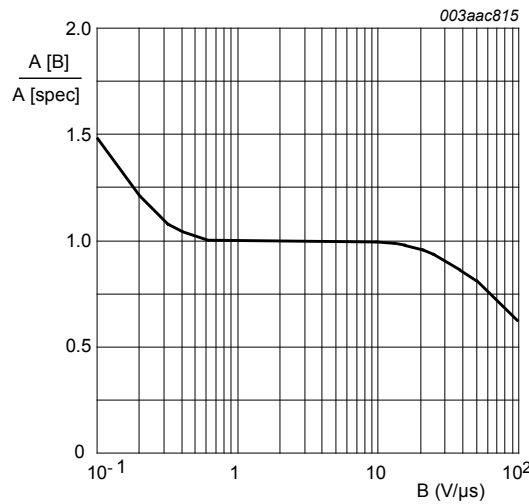
$A = dV_D/dt$ at condition T_j °C
 $B = dV_D/dt$ at condition T_j [125] °C

Fig. 11. Normalized rate of rise of off-state voltage as a function of junction temperature



$A = dI_{com}/dt$ at condition T_j °C
 $B = dI_{com}/dt$ at condition T_j [125] °C
 $V_D = 400$ V

Fig. 12. Normalized critical rate of rise of commutating current as a function of junction temperature



$A[B] = dI_{com}/dt$ at condition B, dV_{com}/dt
 $A[spec]$ is the data sheet value for dI_{com}/dt
turn-off time is less than 20 ms

Fig. 13. Normalized critical rate of change of commutating current as a function of critical rate of change of commutating voltage; minimum values

10. Package outline

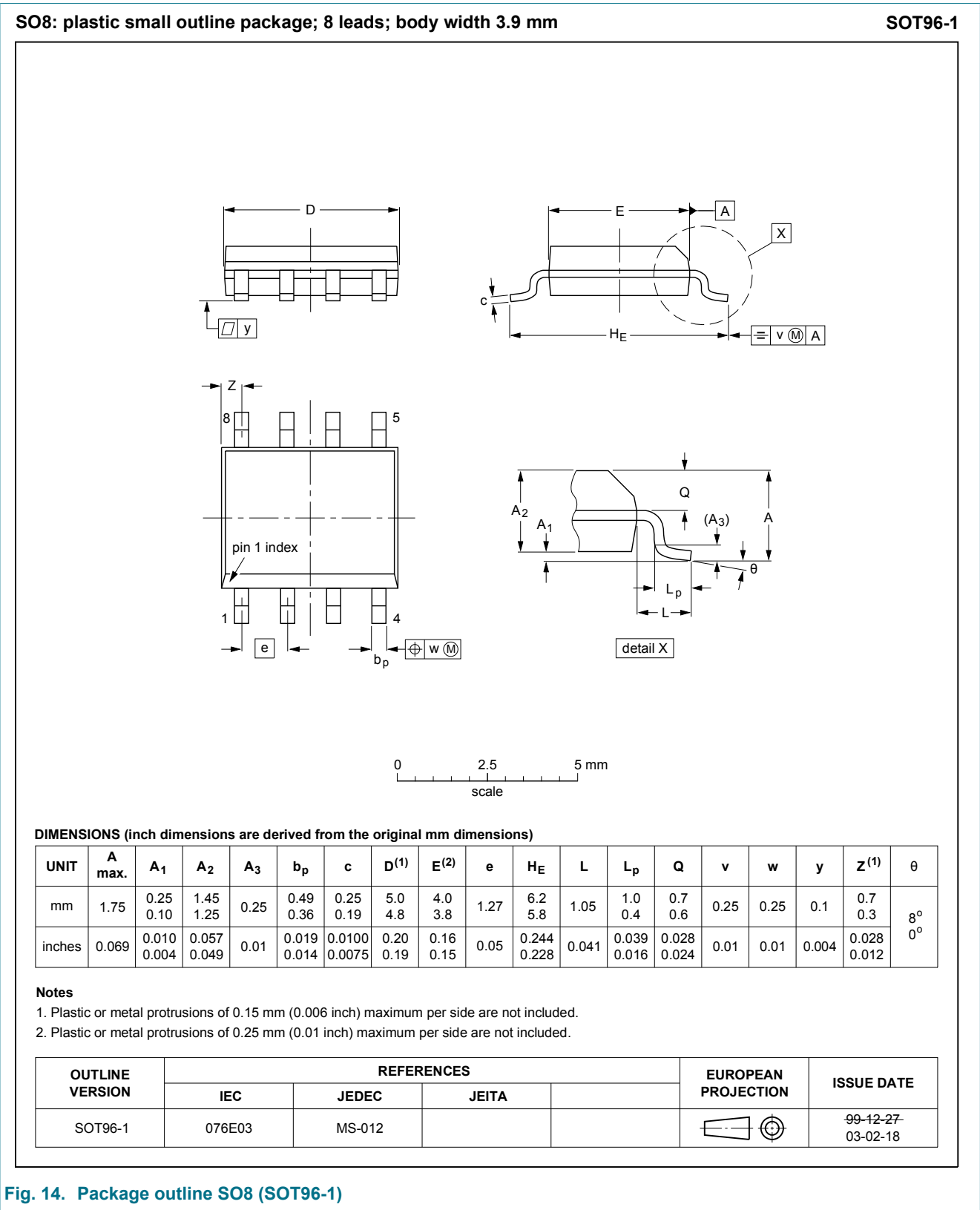


Fig. 14. Package outline SO8 (SOT96-1)

11. Soldering

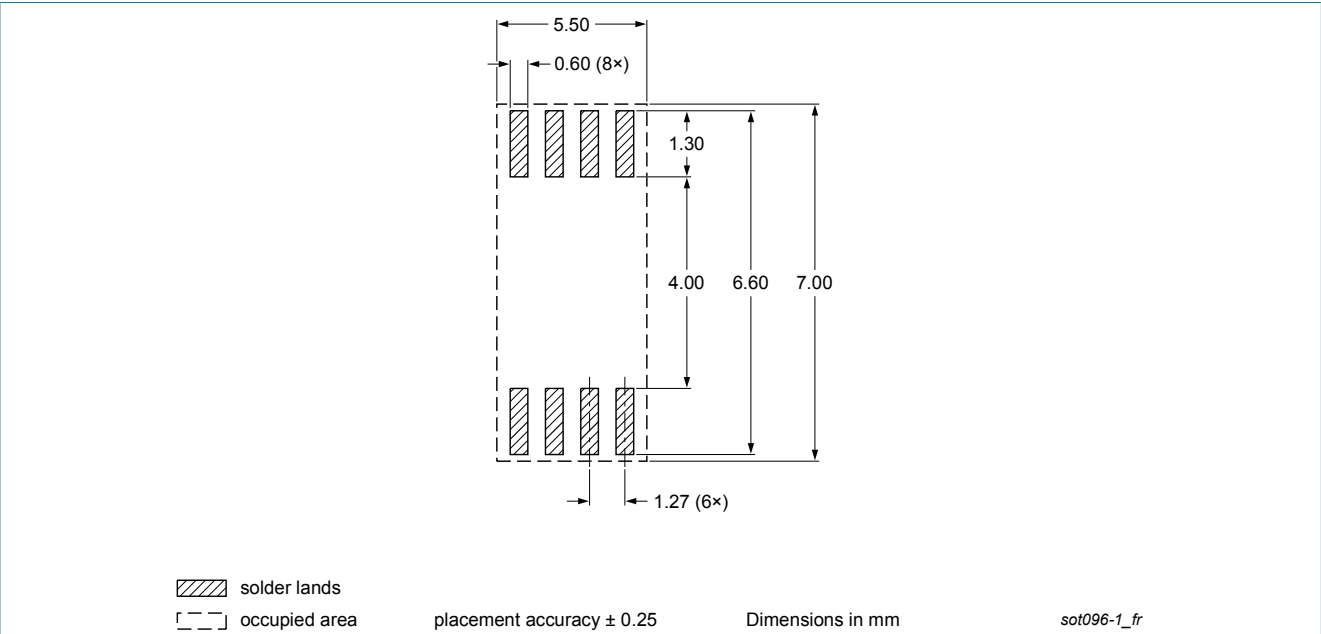


Fig. 15. Reflow soldering footprint for SO8 (SOT96-1)

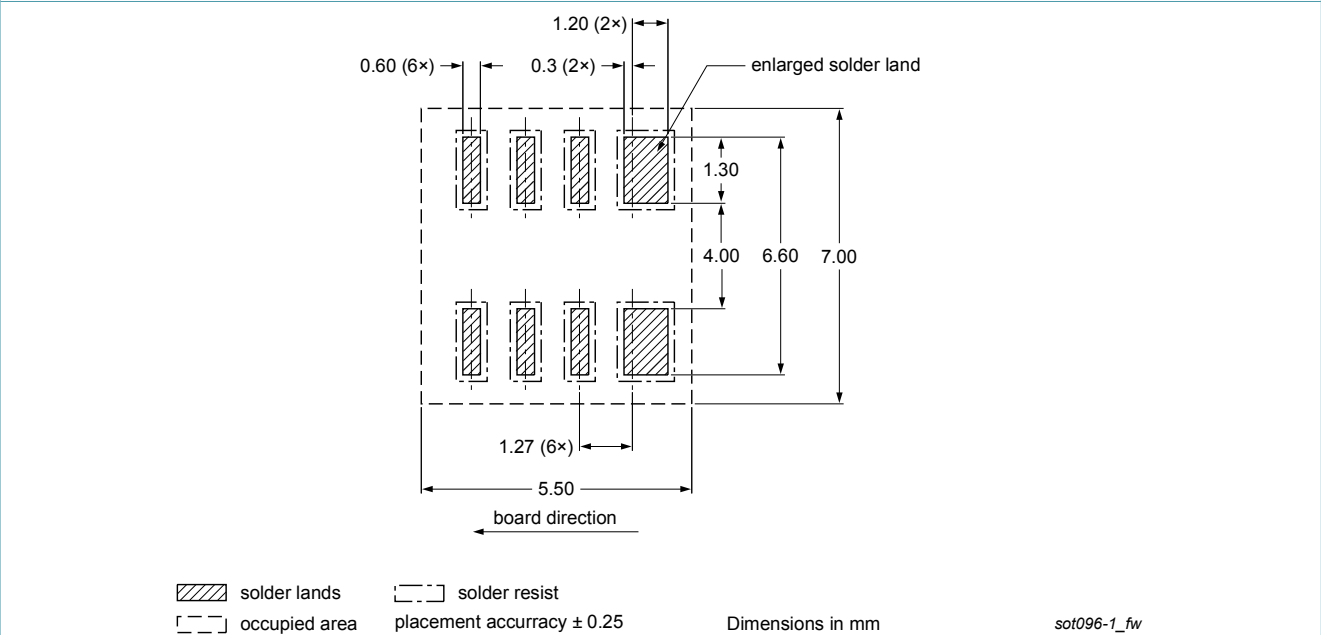


Fig. 16. Wave soldering footprint for SO8 (SOT96-1)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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