

P-Channel NexFET™ Power MOSFET

Check for Samples: [CSD25201W15](#)

FEATURES

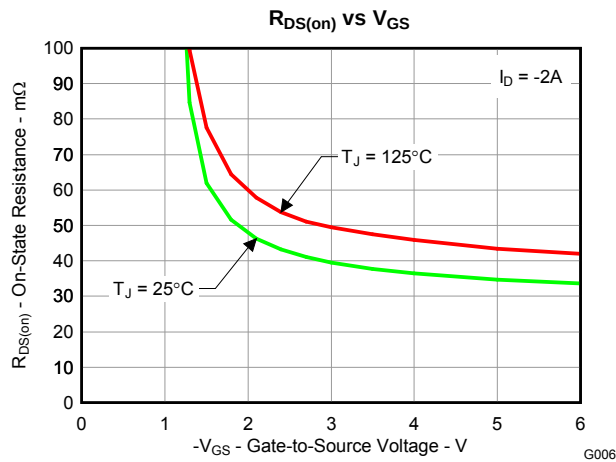
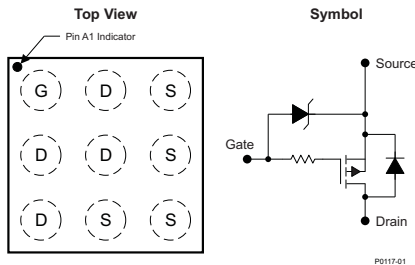
- Low Resistance
- Small Footprint 1.5-mm × 1.5-mm
- Gate ESD Protection –3kV
- Pb Free
- RoHS Compliant
- Halogen Free
- Gate-Source Voltage Clamp

APPLICATIONS

- Battery Management
- Battery Protection

DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile. Low on resistance coupled with the small footprint and low profile make the device ideal for battery operated space constrained applications.



PRODUCT SUMMARY

V_{DS}	Drain to Drain Voltage	–20	V
Q_g	Gate Charge Total (–4.5V)	4.3	nC
Q_{gd}	Gate Charge Gate to Drain	0.7	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -1.8V$	52 mΩ
		$V_{GS} = -2.5V$	42 mΩ
		$V_{GS} = -4.5V$	33 mΩ
$V_{GS(th)}$	Threshold Voltage	–0.7	V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD25201W15	1.5-mm × 1.5-mm Wafer Level Package	7-Inch Reel	3000	Tape and Reel

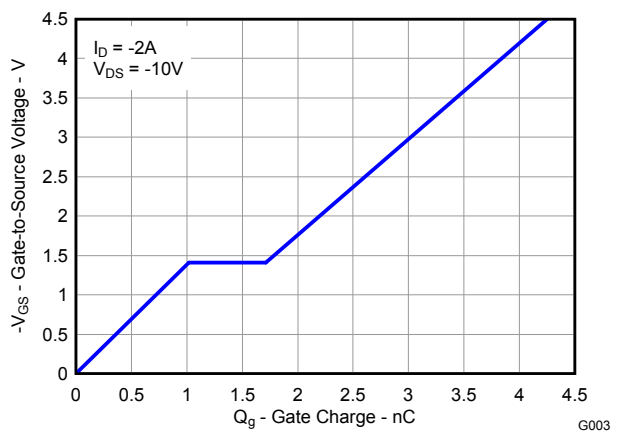
ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	–20	V
V_{GS}	Gate to Source Voltage	–6	V
I_D	Continuous Drain Current ⁽¹⁾⁽²⁾	4	A
	Pulsed Drain Current ⁽¹⁾⁽²⁾	4	A
I_G	Continuous Gate Current ⁽¹⁾⁽²⁾	0.5	A
	Pulsed Gate Current ⁽¹⁾⁽²⁾	7	A
P_D	Power Dissipation ⁽¹⁾	1.5	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C

(1) Based on Min Cu footprint

(2) Ball limited

GATE CHARGE



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV _{DSS}	Drain to Source Voltage	V _{GS} = 0V, I _{DS} = −250μA	−20			V
BV _{GSS}	Gate to Source Voltage	V _{DS} = 0V, I _G = −250μA	−6.1		−7.2	V
I _{DDS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = −16V			−1	μA
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = −6V			−100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = −250μA	−0.4	−0.7	−1.1	V
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = −1.8V, I _{DS} = −2A	52		70	mΩ
		V _{GS} = −2.5V, I _{DS} = −2A	42		50	mΩ
		V _{GS} = −4.5V, I _{DS} = −2A	33		40	mΩ
g _{fs}	Transconductance	V _{DS} = −10V, I _{DS} = −2A	12			S
Dynamic Characteristics						
C _{ISS}	Input Capacitance	V _{GS} = 0V, V _{DS} = −10V, f = 1MHz	490		640	pF
C _{OSS}	Output Capacitance		215		280	pF
C _{RSS}	Reverse Transfer Capacitance		70		91	pF
R _G	Series Gate Resistance ⁽¹⁾	V _{DS} = −10V, I _O = −2A	26		35	Ω
Q _g	Gate Charge Total (−4.5V)		4.3		5.6	nC
Q _{gd}	Gate Charge - Gate to Drain		0.7			nC
Q _{gs}	Gate Charge - Gate to Source		1			nC
Q _{g(th)}	Gate Charge at V _{th}		0.3			nC
Q _{OSS}	Output Charge	V _{DS} = −9.5V, V _{GS} = 0V	3.1			nC
t _{d(on)}	Turn On Delay Time ⁽²⁾	V _{DS} = −10V, V _{GS} = −4.5V, I _{DS} = −2A, R _G = 2Ω	9.5			ns
t _r	Rise Time ⁽²⁾		11			ns
t _{d(off)}	Turn Off Delay Time ⁽²⁾		51			ns
t _f	Fall Time ⁽²⁾		38			ns
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _{DS} = −2A, V _{GS} = 0V	0.7		1	V
Q _{rr}	Reverse Recovery Charge	V _{DD} = −9.5V, I _F = −2A, di/dt = 200A/μs	5.7			nC
t _{rr}	Reverse Recovery Time		10			ns

(1) Includes gate clamp resistor

(2) External R_G is in addition to the internal gate clamp resistor

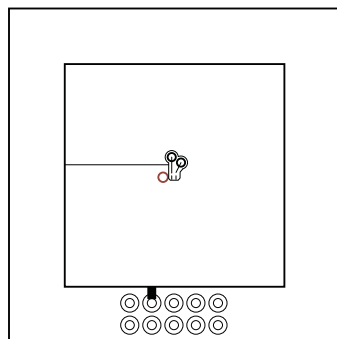
THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

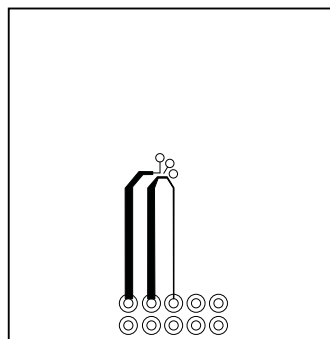
PARAMETER		MIN	TYP	MAX	UNIT
R _{θJA}	Junction to Ambient Thermal Resistance ⁽¹⁾			283	°C/W
	Junction to Ambient Thermal Resistance ⁽²⁾			185	°C/W

(1) Device mounted on FR4 material with minimum Cu mounting area.

(2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



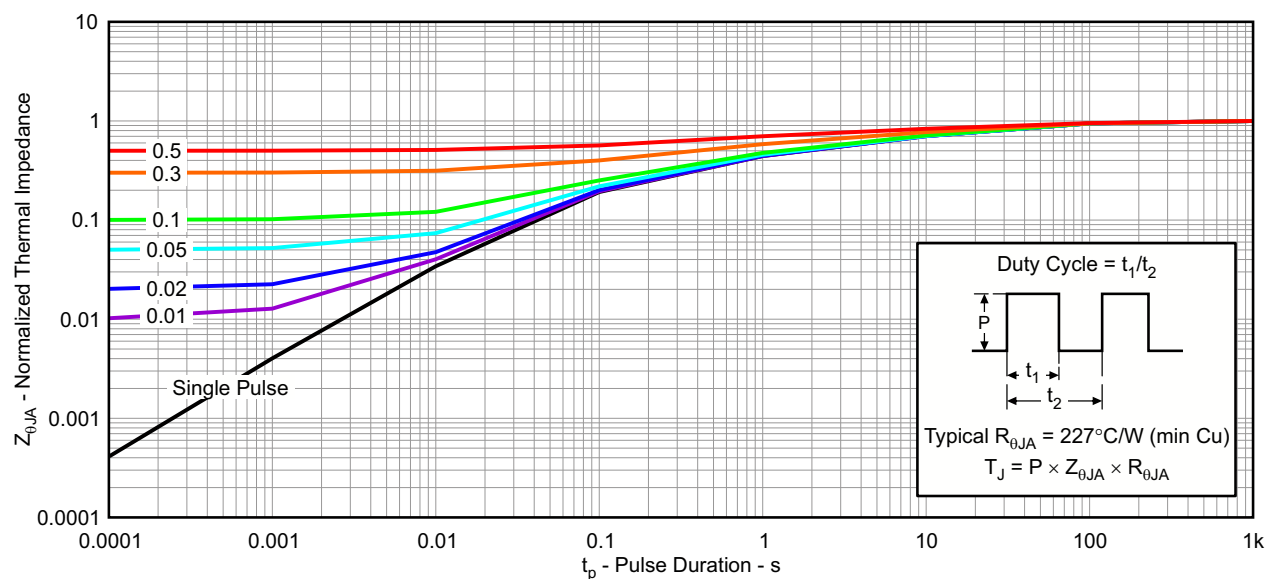
Max $R_{\theta JA} = 185^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.



Max $R_{\theta JA} = 283^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

TYPICAL MOSFET CHARACTERISTICS

$T_A = 25^{\circ}\text{C}$, unless stated otherwise.



G012

Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, unless stated otherwise.

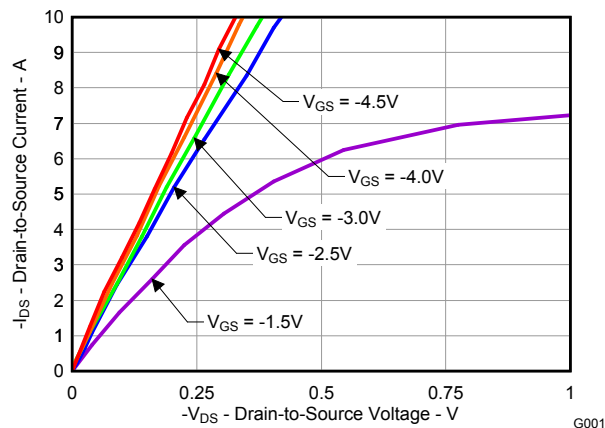


Figure 2. Saturation Characteristics

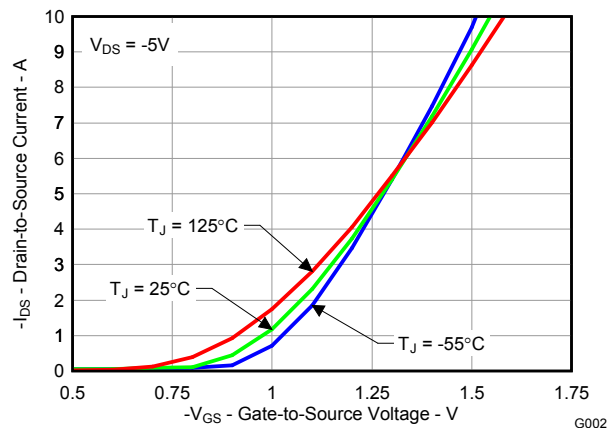


Figure 3. Transfer Characteristics

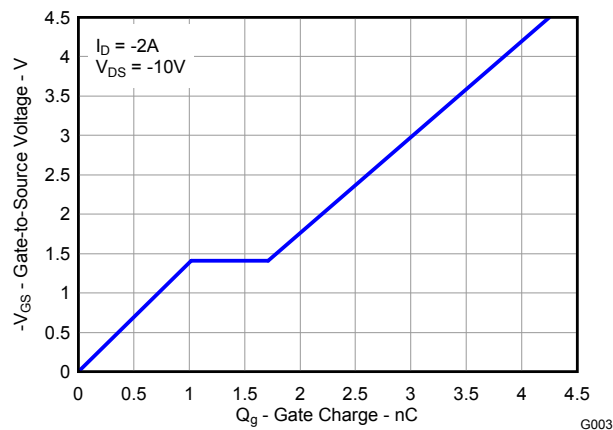


Figure 4. Gate Charge

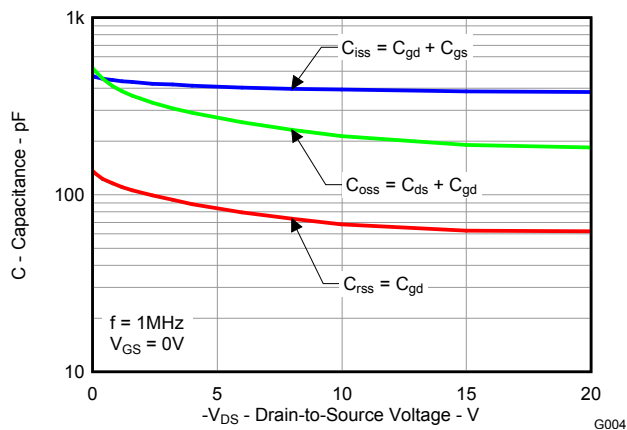


Figure 5. Capacitance

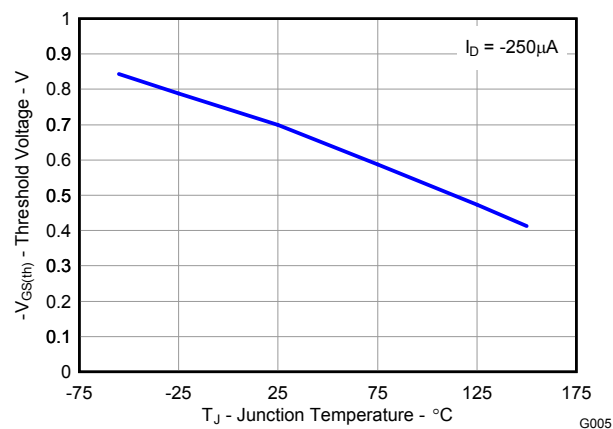


Figure 6. Threshold Voltage vs. Temperature

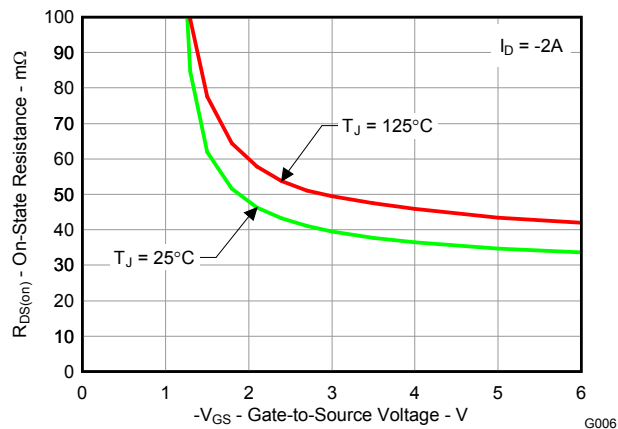


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, unless stated otherwise.

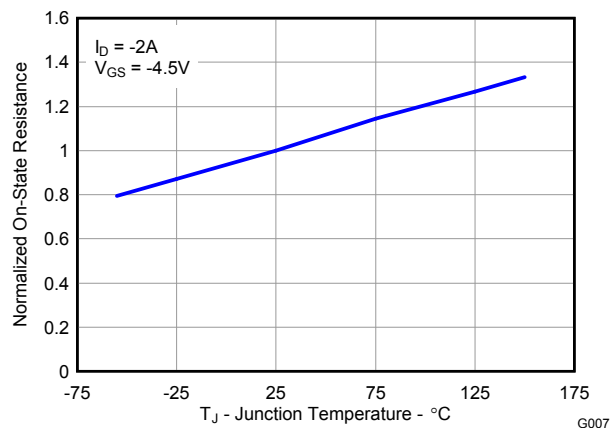


Figure 8. Normalized On-State Resistance vs. Temperature

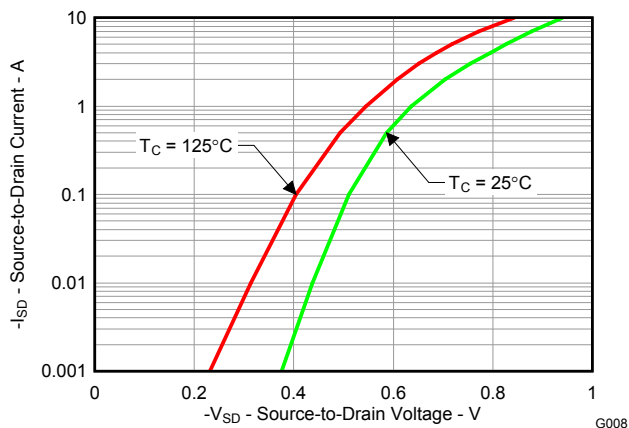


Figure 9. Typical Diode Forward Voltage

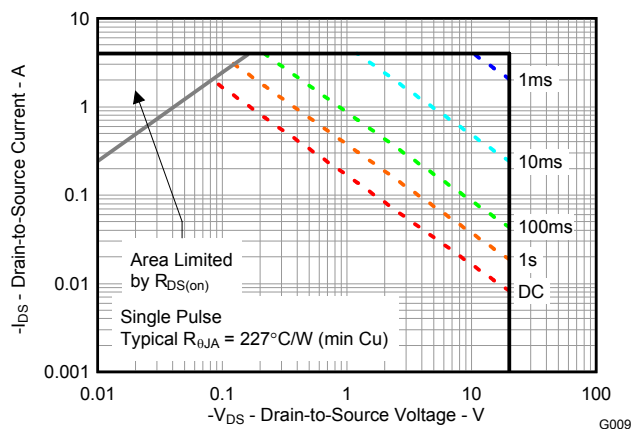


Figure 10. Maximum Safe Operating Area

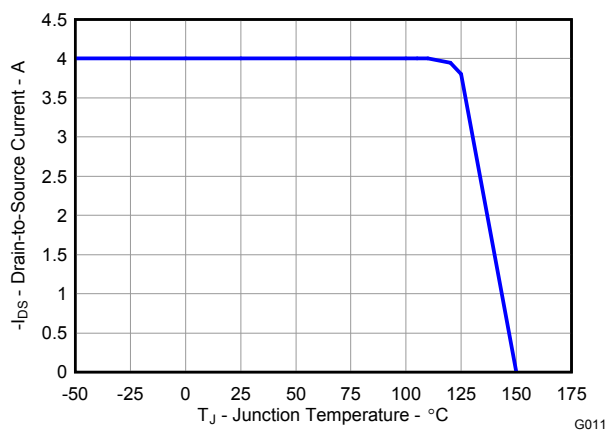
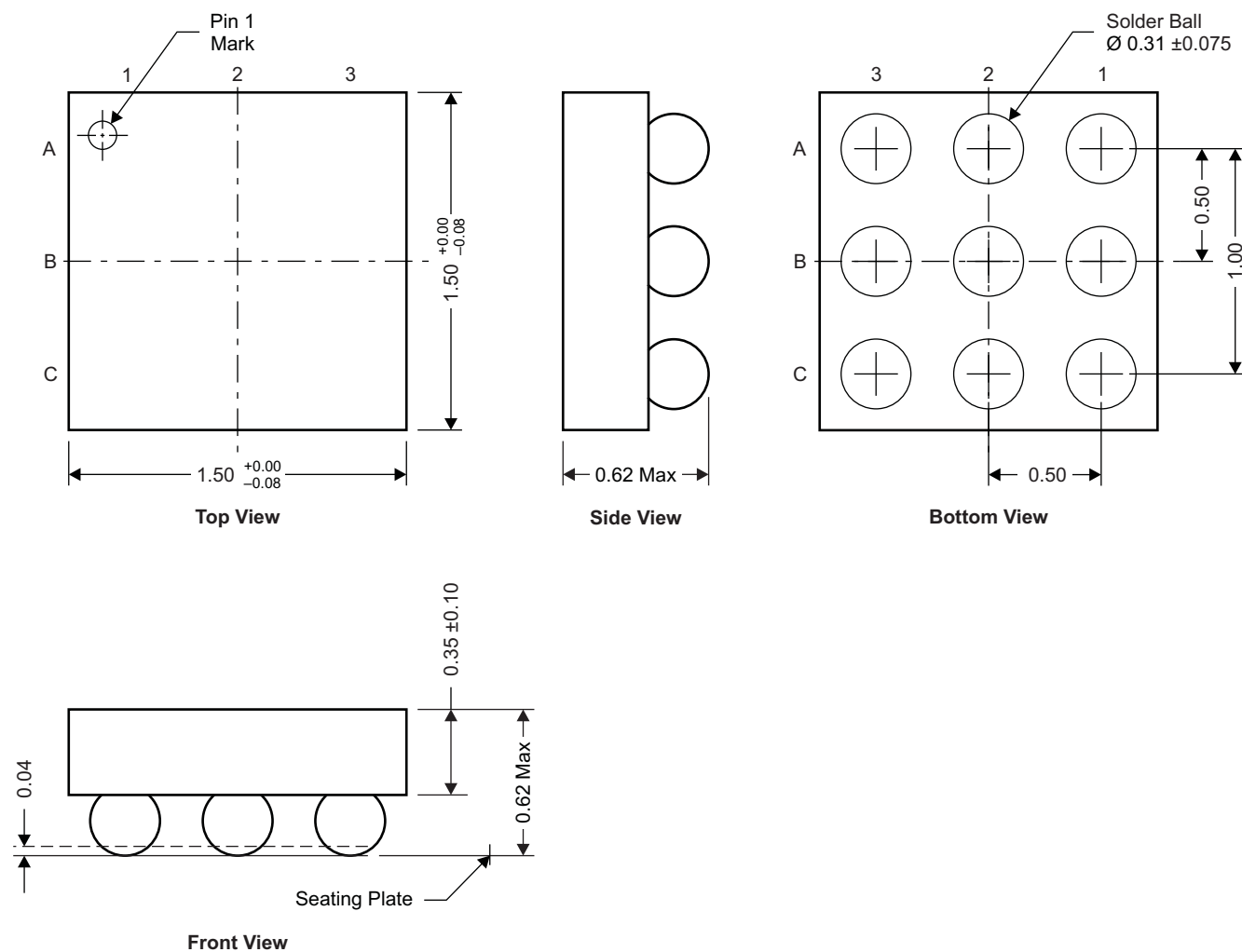


Figure 11. Maximum Drain Current vs. Temperature

MECHANICAL DATA

CSD25201W15 Package Dimensions



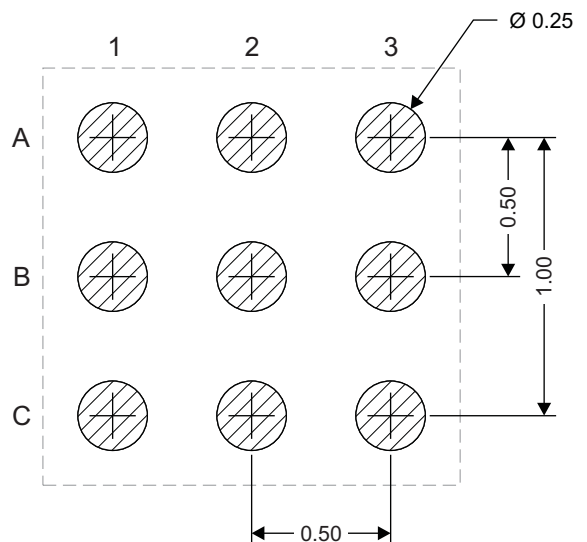
NOTE: All dimensions are in mm (unless otherwise specified)

M0171-01

Pinout

POSITION	DESIGNATION
A1	Gate
A2, B1, B2, C1	Drain
A3, B3, C2, C3	Source

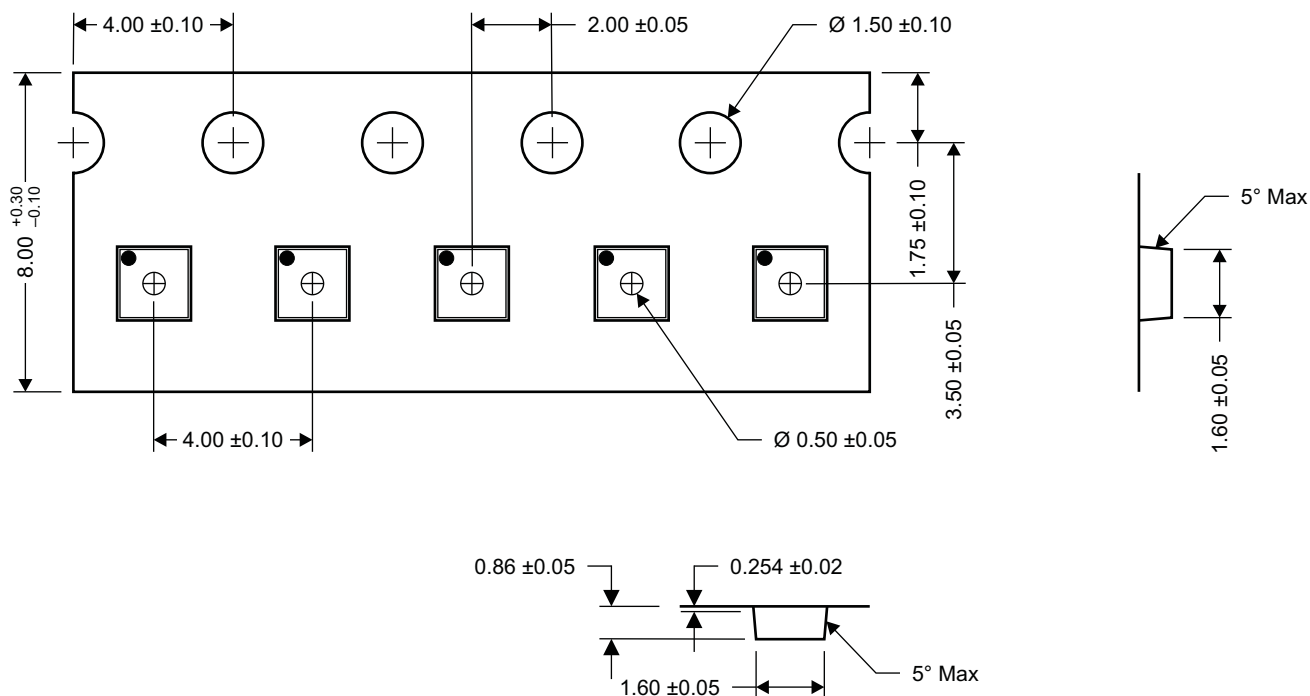
Recommended Land Pattern



M0172-01

NOTE: All dimensions are in mm (unless otherwise specified)

Tape and Reel Information



M0173-01

- NOTES:
1. 10-sprocket hole-pitch cumulative tolerance ± 0.2
 2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
 3. Material: black static-dissipative polystyrene
 4. All dimensions are in mm (unless otherwise specified)
 5. Thickness: 0.30 ± 0.05 mm
 6. MSL1 260°C (IR and convection) PbF reflow compatible

REVISION HISTORY

Changes from Original (June 2010) to Revision A	Page
• Changed the C_{ISS} Input Capacitance Typ and Max Values From: 390 and 510 pF To: 490 and 640 pF	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25201W15	OBSOLETE	DSBGA	YZF	9		TBD	Call TI	Call TI	-55 to 150		

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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