

BUK9Y58-75B

N-channel TrenchMOS logic level FET

Rev. 04 — 7 April 2010

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V, 24 V and 42 V loads
- Automotive systems
- DC-to-DC converters
- General purpose power switching
- solenoid drives

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	75	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ; see Figure 4	-	-	20.7 3	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	60.4	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 10\text{ A}$; $T_j = 25\text{ °C}$; see Figure 13	-	52	58	mΩ
		$V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; $T_j = 25\text{ °C}$	-	47	53	mΩ

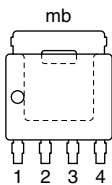
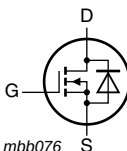


Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 20.73\text{ A}$; $V_{sup} \leq 75\text{ V}$; $R_{GS} = 50\ \Omega$; $V_{GS} = 5\text{ V}$; $T_{J(init)} = 25\text{ }^\circ\text{C}$; unclamped	-	-	34	mJ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 5\text{ V}$; $I_D = 10\text{ A}$; $V_{DS} = 60\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; see Figure 14	-	5	-	nC

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

SOT669 (LFAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9Y58-75B	LFAK	plastic single-ended surface-mounted package (LFAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	75	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$; $T_{mb} \geq 25\text{ °C}$; $T_{mb} \leq 175\text{ °C}$	-	-	75	V
V_{GS}	gate-source voltage		-15	-	15	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; see Figure 1 ; see Figure 4	-	-	20.73	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; see Figure 1	-	-	14.66	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; $t_p \leq 10\text{ }\mu\text{s}$; pulsed; see Figure 4	-	-	82.9	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	60.4	W
T_{stg}	storage temperature		-55	-	175	°C
T_j	junction temperature		-55	-	175	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	-	-	20.73	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$	-	-	82.9	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 20.73\text{ A}$; $V_{sup} \leq 75\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped	-	-	34	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see Figure 3	[1] [2] [3]	-	-	J

[1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[2] Repetitive avalanche rating limited by average junction temperature of 170 °C.

[3] Refer to application note AN10273 for further information.

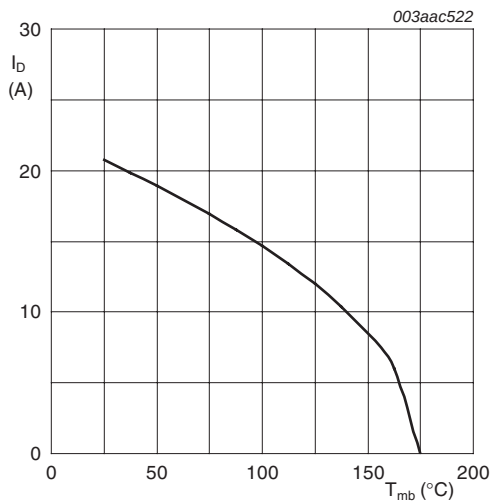
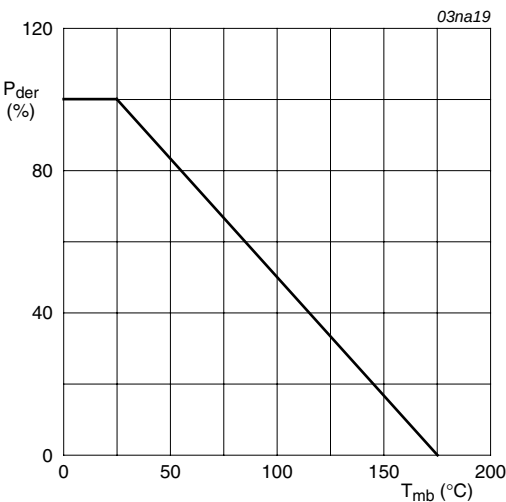


Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

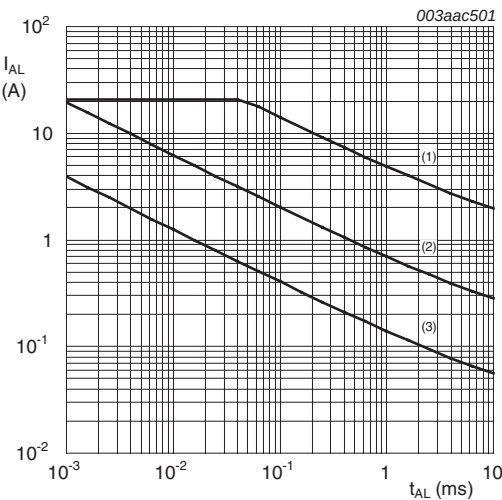
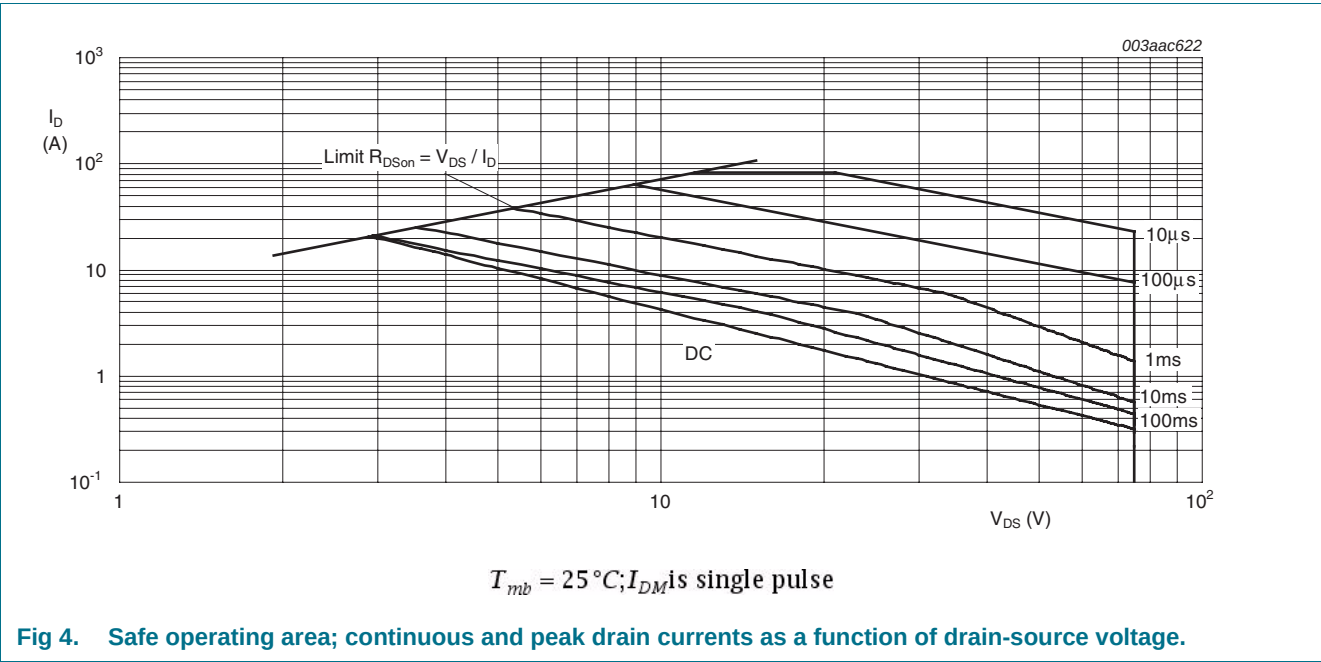


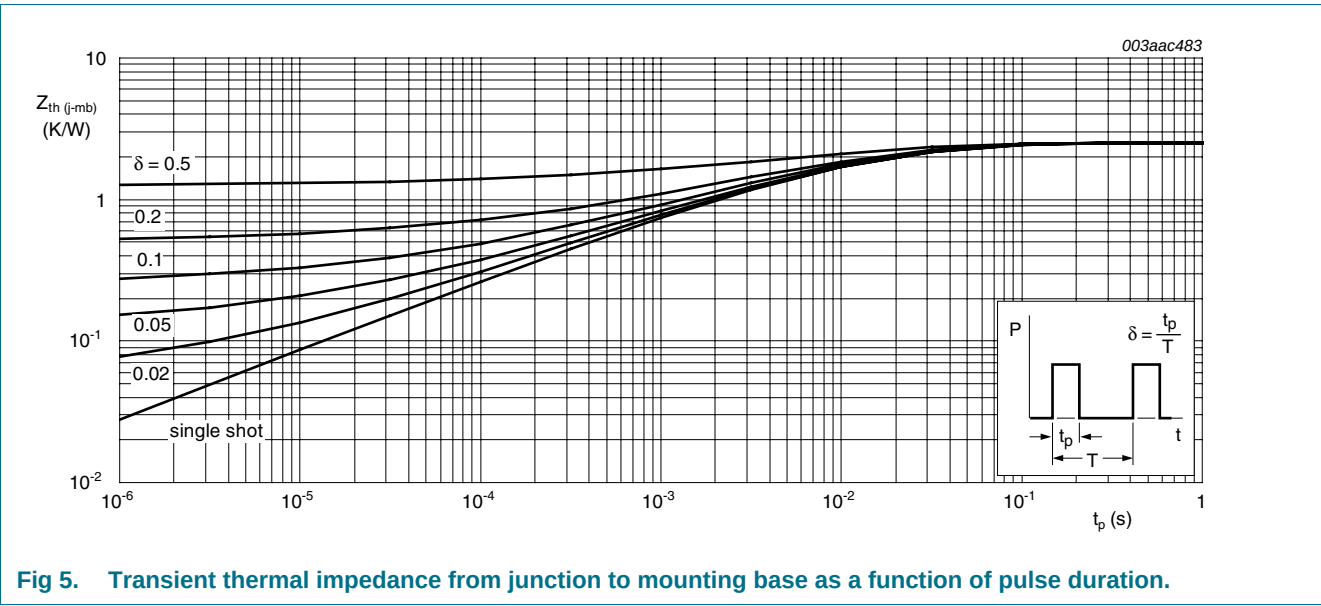
Fig 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time



5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	2.53	K/W



6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V; T _j = 25 °C	75	-	-	V
		I _D = 0.25 mA; V _{GS} = 0 V; T _j = -55 °C	70	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; see Figure 10 ; see Figure 11	0.5	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 10 ; see Figure 11	1.25	1.65	2.15	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; see Figure 10 ; see Figure 11	-	-	2.45	V
I _{DSS}	drain leakage current	V _{DS} = 75 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
		V _{DS} = 75 V; V _{GS} = 0 V; T _j = 25 °C	-	0.02	1	μA
I _{GSS}	gate leakage current	V _{DS} = 0 V; V _{GS} = +15 V; T _j = 25 °C	-	2	100	nA
		V _{DS} = 0 V; V _{GS} = -15 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 10 A; T _j = 25 °C	-	-	61	mΩ
		V _{GS} = 5 V; I _D = 10 A; T _j = 175 °C; see Figure 12	-	-	145	mΩ
		V _{GS} = 5 V; I _D = 10 A; T _j = 25 °C; see Figure 13	-	52	58	mΩ
		V _{GS} = 10 V; I _D = 10 A; T _j = 25 °C	-	47	53	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 10 A; V _{DS} = 60 V; V _{GS} = 5 V; T _j = 25 °C; see Figure 14	-	10.7	-	nC
Q _{GS}	gate-source charge		-	2.3	-	nC
Q _{GD}	gate-drain charge		-	5	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; see Figure 15	-	853	1137	pF
C _{oss}	output capacitance		-	106	127	pF
C _{rss}	reverse transfer capacitance		-	52	71	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 3 Ω; V _{GS} = 5 V; R _{G(ext)} = 10 Ω; T _j = 25 °C	-	15	-	ns
t _r	rise time		-	16	-	ns
t _{d(off)}	turn-off delay time		-	30	-	ns
t _f	fall time		-	9	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 10 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 16	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = -10 V; V _{DS} = 30 V; T _j = 25 °C	-	53	-	ns
Q _r	recovered charge		-	122	-	nC

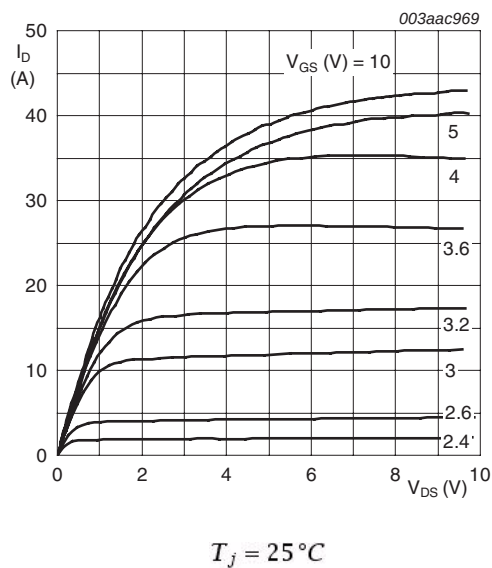


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values.

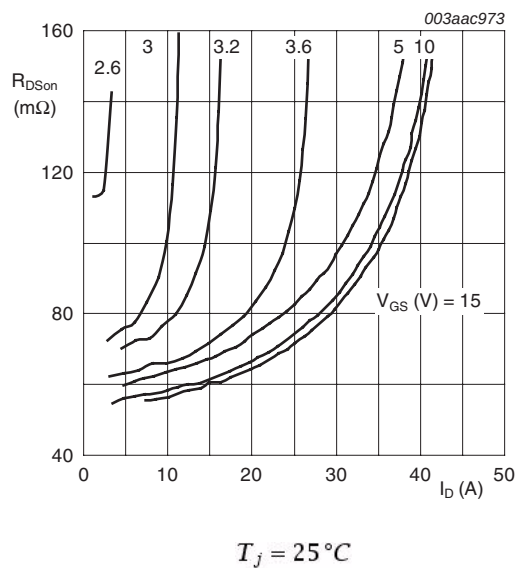


Fig 7. Drain-source on-state resistance as a function of drain current; typical values.

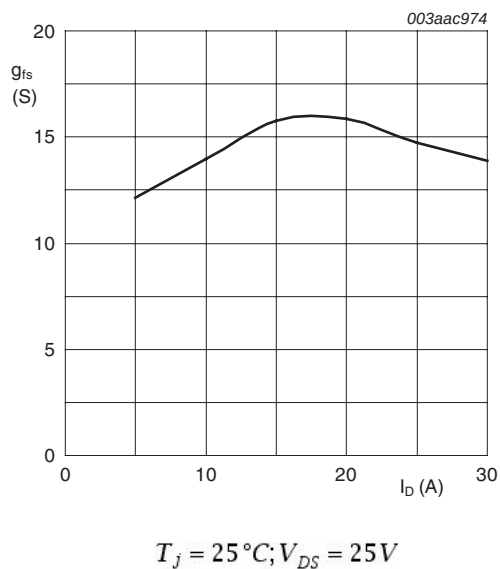


Fig 8. Forward transconductance as a function of drain current; typical values.

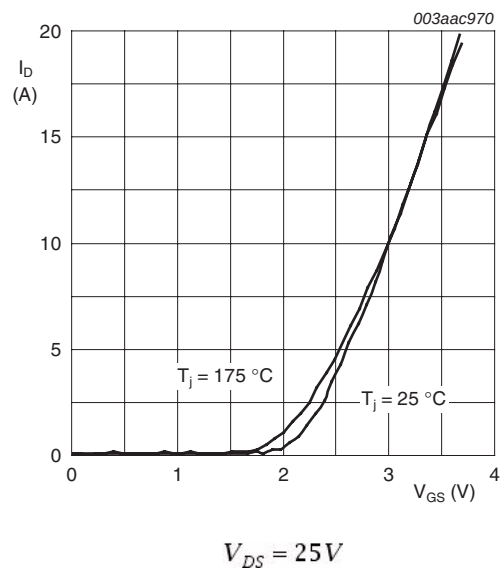
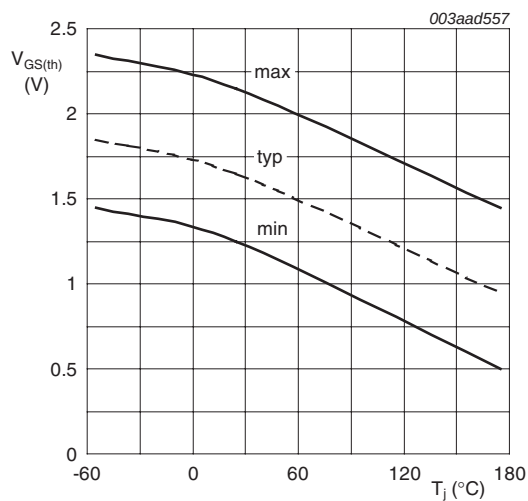
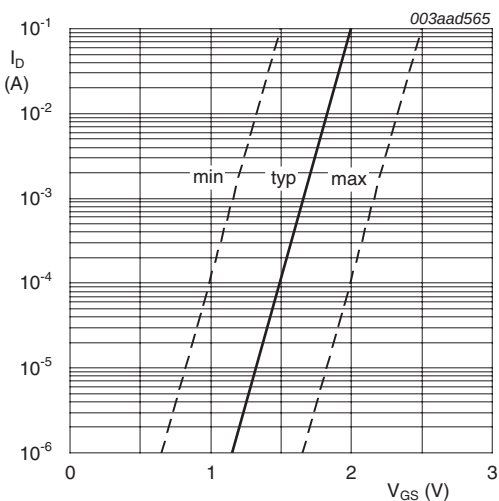


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



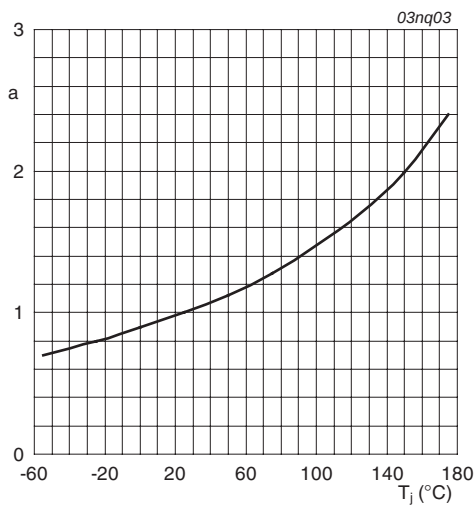
$I_D = 1\text{mA}; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



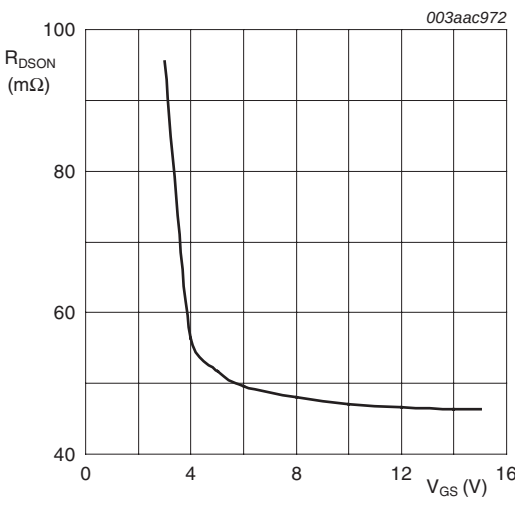
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = V_{GS}$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25\text{ }^\circ\text{C}; I_D = 10\text{A}$

Fig 13. Drain-source on-state resistance as a function of gate-source voltage; typical values.

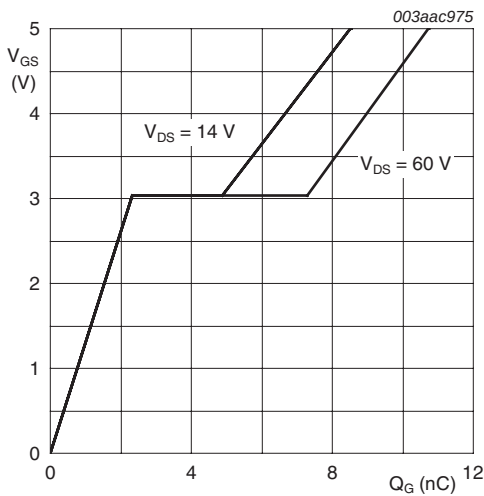


Fig 14. Gate-source voltage as a function of gate charge; typical values.

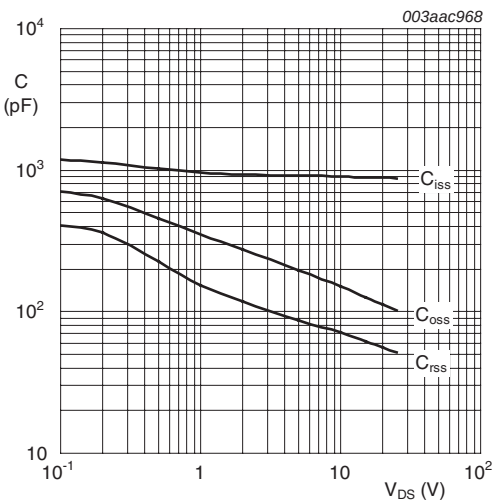


Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.

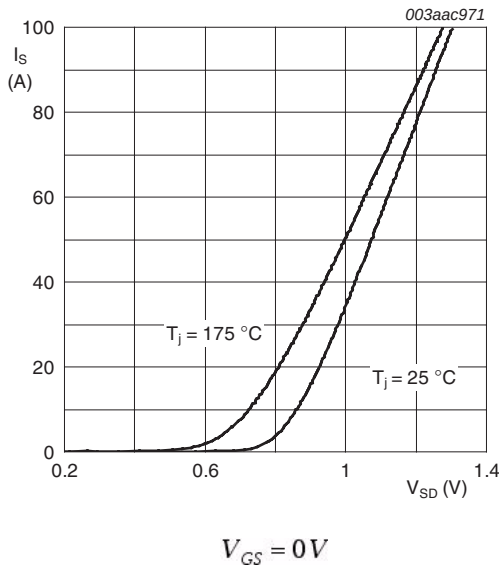


Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

7. Package outline

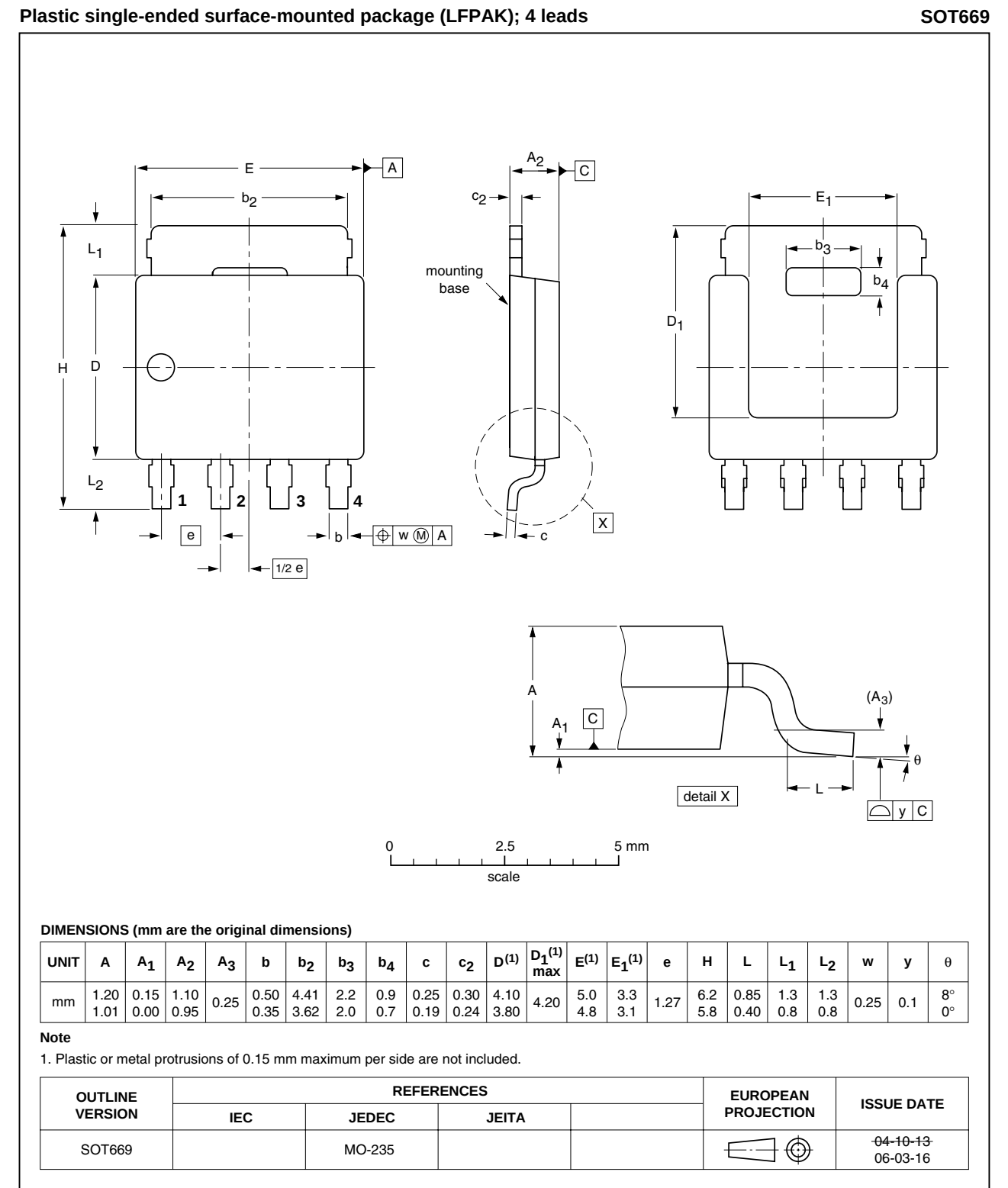


Fig 17. Package outline SOT669 (LPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9Y58-75B_4	20100407	Product data sheet	-	BUK9Y58-75B_3
Modifications:	• Status changed from objective to product.			
BUK9Y58-75B_3	20100216	Objective data sheet	-	BUK9Y58-75B_2

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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