



# N-Channel 150 V (D-S) MOSFET

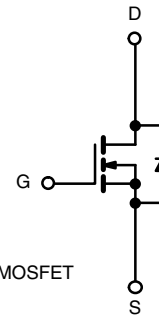
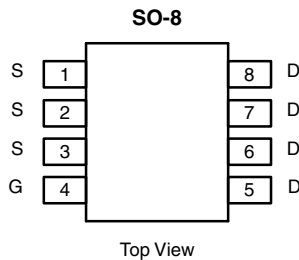
PRODUCT SUMMARY		
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
150	0.050 at V <sub>GS</sub> = 10 V	5

## FEATURES

- TrenchFET® Power MOSFETs
- Material categorization:  
For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available



Ordering Information: Si4488DY-T1-E3 (Lead (Pb)-free)  
Si4488DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)					
Parameter	Symbol	10 s	Steady State	Unit	
Drain-Source Voltage	V <sub>DS</sub>	150		V	
Gate-Source Voltage	V <sub>GS</sub>	± 20			
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	I <sub>D</sub>	T <sub>A</sub> = 25 °C	5	3.5	A
		T <sub>A</sub> = 70 °C	4	2.8	
Pulsed Drain Current	I <sub>DM</sub>	50			
Avalanche Current	I <sub>AS</sub>	25			
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	2.8	1.4		
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>A</sub> = 25 °C	3.1	1.56	W
		T <sub>A</sub> = 70 °C	2	1	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	t ≤ 10 s	R <sub>thJA</sub>	33	40	°C/W
	Steady State		65	80	
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	17	21	

Notes:  
a. Surface mounted on 1" x 1" FR4 board.

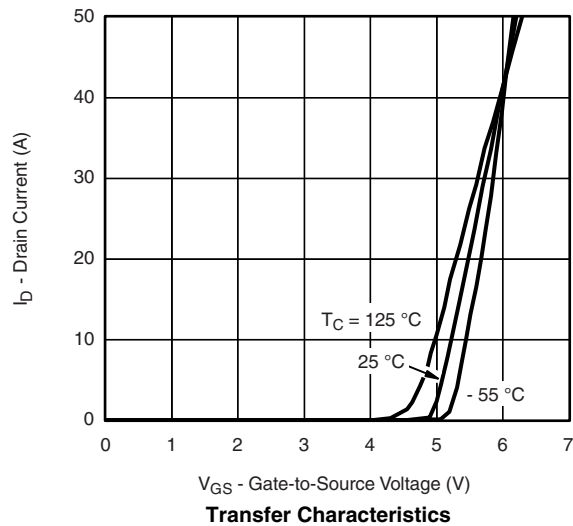
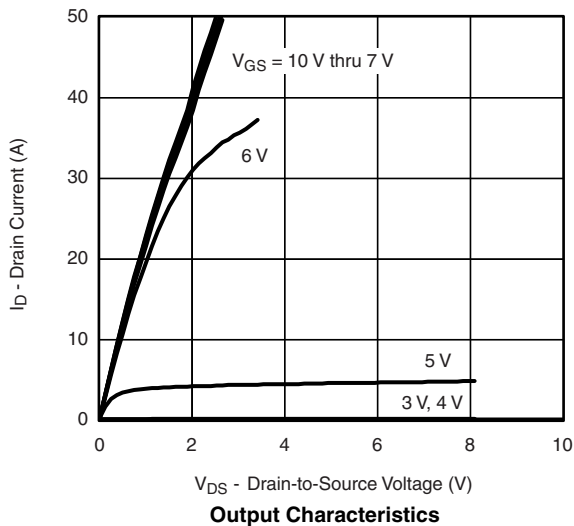
<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 120\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 120\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			5	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	50			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 5\text{ A}$		0.041	0.050	$\Omega$
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 5\text{ A}$		18		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 2.8\text{ A}, V_{GS} = 0\text{ V}$		0.75	1.1	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 75\text{ V}, V_{GS} = 10\text{ V}, I_D = 5\text{ A}$		30	45	nC
Gate-Source Charge	$Q_{gs}$			8.5		
Gate-Drain Charge	$Q_{gd}$			8.5		
Gate Resistance	$R_g$		0.2	0.85	1.2	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 75\text{ V}, R_L = 15\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 6\text{ }\Omega$		12	18	ns
Rise Time	$t_r$			7	11	
Turn-Off Delay Time	$t_{d(off)}$			22	33	
Fall Time	$t_f$			10	15	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 2.8\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$		40	70	

Notes:

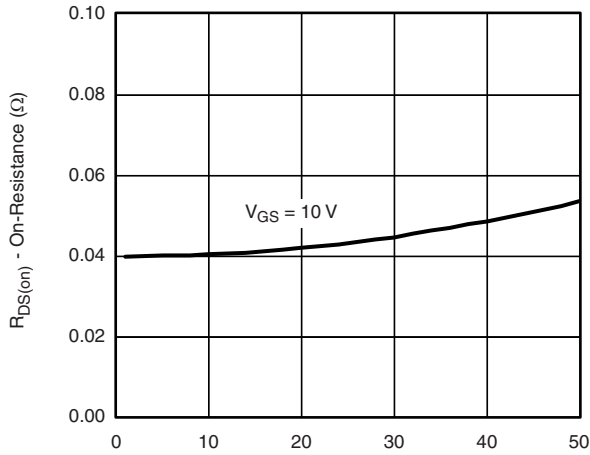
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

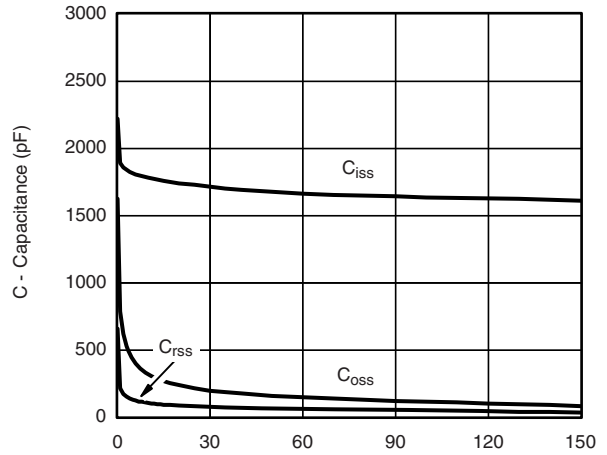
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



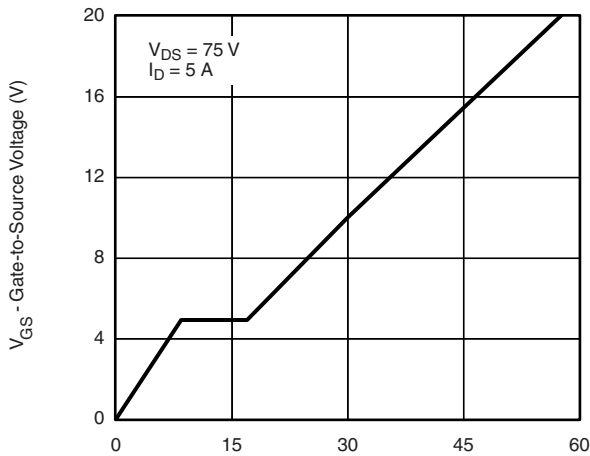
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



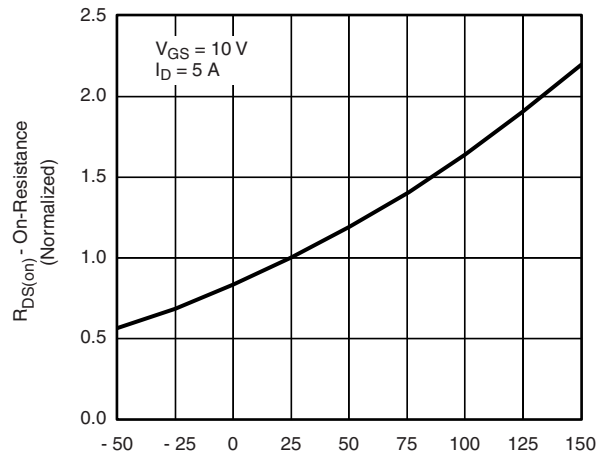
$I_D$  - Drain Current (A)  
**On-Resistance vs. Drain Current**



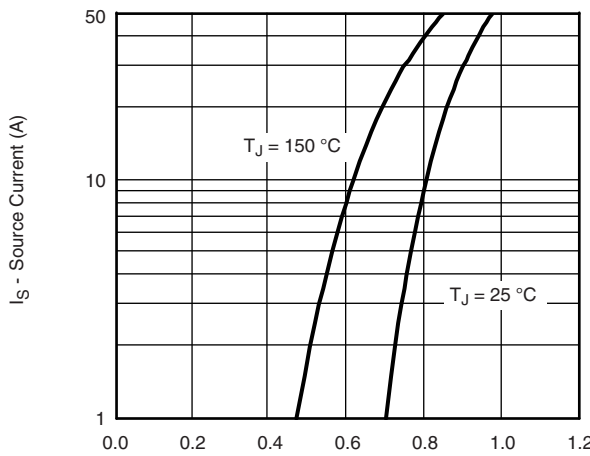
$V_{DS}$  - Drain-to-Source Voltage (V)  
**Capacitance**



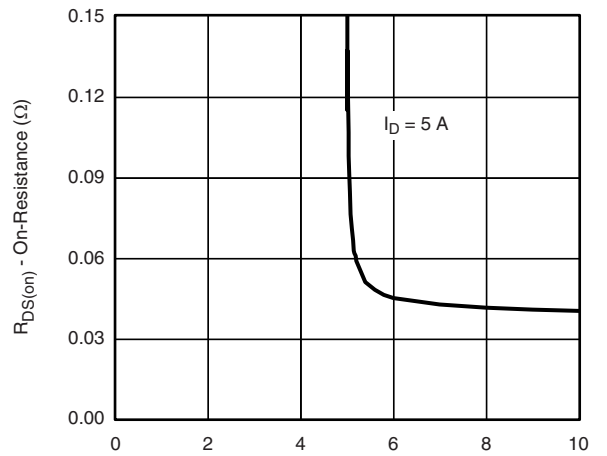
$Q_g$  - Total Gate Charge (nC)  
**Gate Charge**



$T_J$  - Junction Temperature ( $^{\circ}\text{C}$ )  
**On-Resistance vs. Junction Temperature**

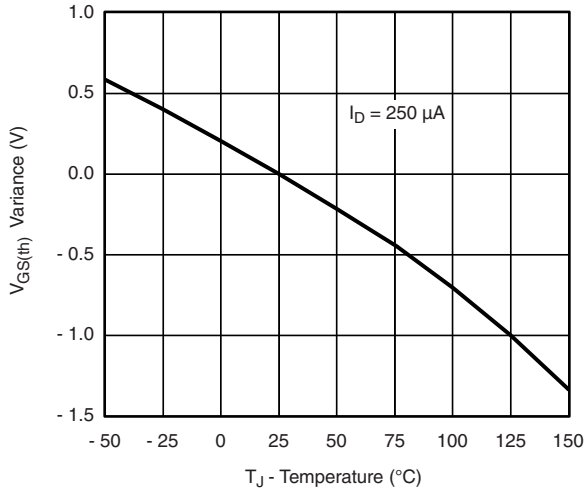


$V_{SD}$  - Source-to-Drain Voltage (V)  
**Source-Drain Diode Forward Voltage**

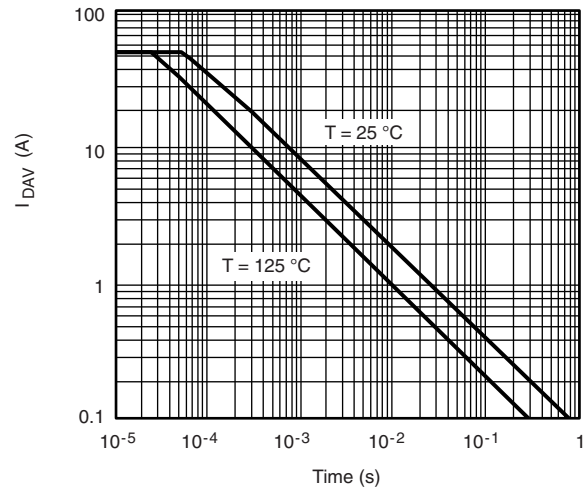


$V_{GS}$  - Gate-to-Source Voltage (V)  
**On-Resistance vs. Gate-to-Source Voltage**

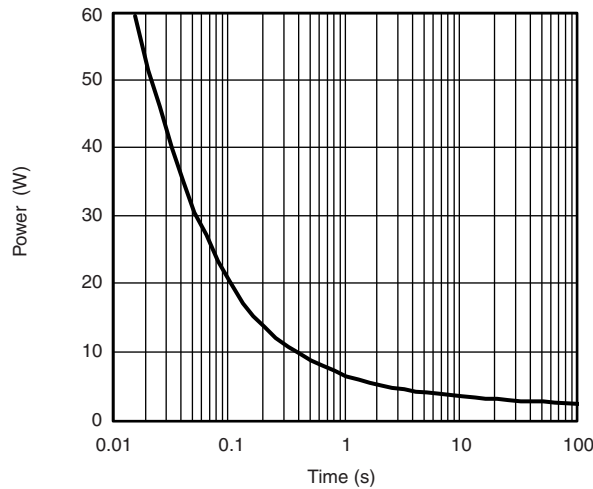
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



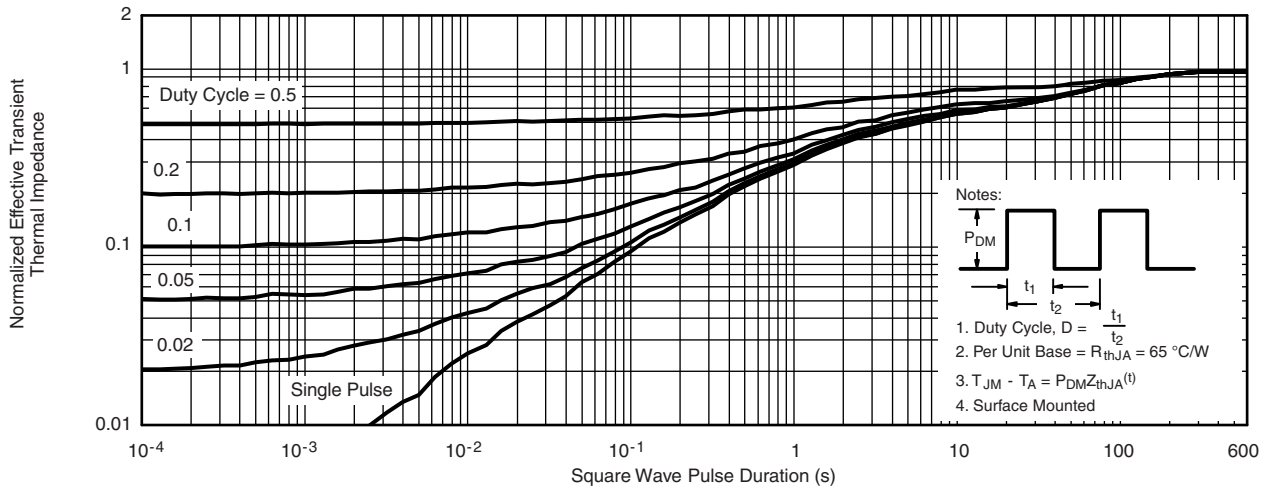
**Threshold Voltage**



**Avalanche Current vs. Time**



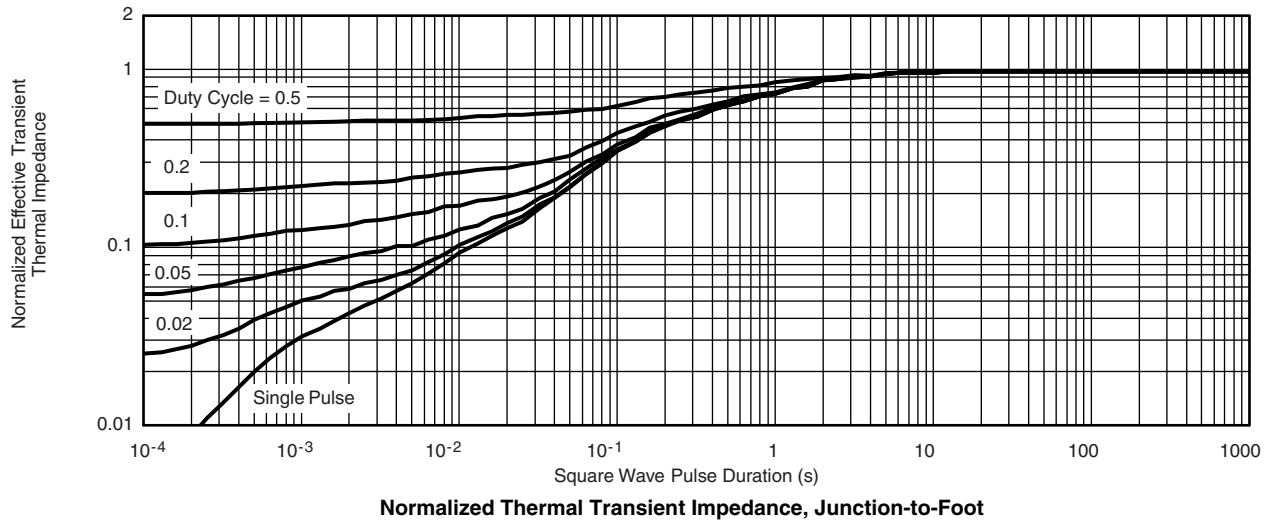
**Single Pulse Power**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

- Notes:
- 
1. Duty Cycle,  $D = \frac{t_1}{t_2}$
  2. Per Unit Base =  $R_{thJA} = 65 \text{ }^\circ\text{C/W}$
  3.  $T_{JM} - T_A = P_{DM}Z_{thJA}(t)$
  4. Surface Mounted

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



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## SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

## RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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