

BLF573; BLF573S

HF / VHF power LDMOS transistor

Rev. 3 — 8 July 2010

Product data sheet

1. Product profile

1.1 General description

A 300 W LDMOS RF power transistor for broadcast applications and industrial, scientific and medical applications in the HF to 500 MHz band.

Table 1. Production test information

Mode of operation	f (MHz)	V _{DS} (V)	P _L (W)	G _p (dB)	η_D (%)
CW	225	50	300	27.2	70

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features and benefits

- Typical CW performance at frequency of 225 MHz, a supply voltage of 50 V and an I_{DQ} of 900 mA:
 - ◆ Average output power = 300 W
 - ◆ Power gain = 27.2 dB
 - ◆ Efficiency = 70 %
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF and VHF band)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

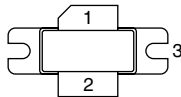
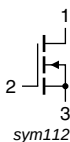
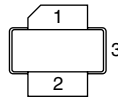
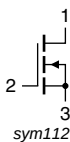
1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications



2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF573 (SOT502A)			
1	drain		 sym112
2	gate		
3	source [1]		
BLF573S (SOT502B)			
1	drain		 sym112
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF573	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF573S	-	earless flanged LDMOST ceramic package, 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	110	V
V_{GS}	gate-source voltage		-0.5	+11	V
I_D	drain current		-	42	A
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}$; $P_L = 300\text{ W}$ [1]	0.21	K/W

[1] $R_{th(j-c)}$ is measured under RF conditions.

6. Characteristics

Table 6. DC characteristics

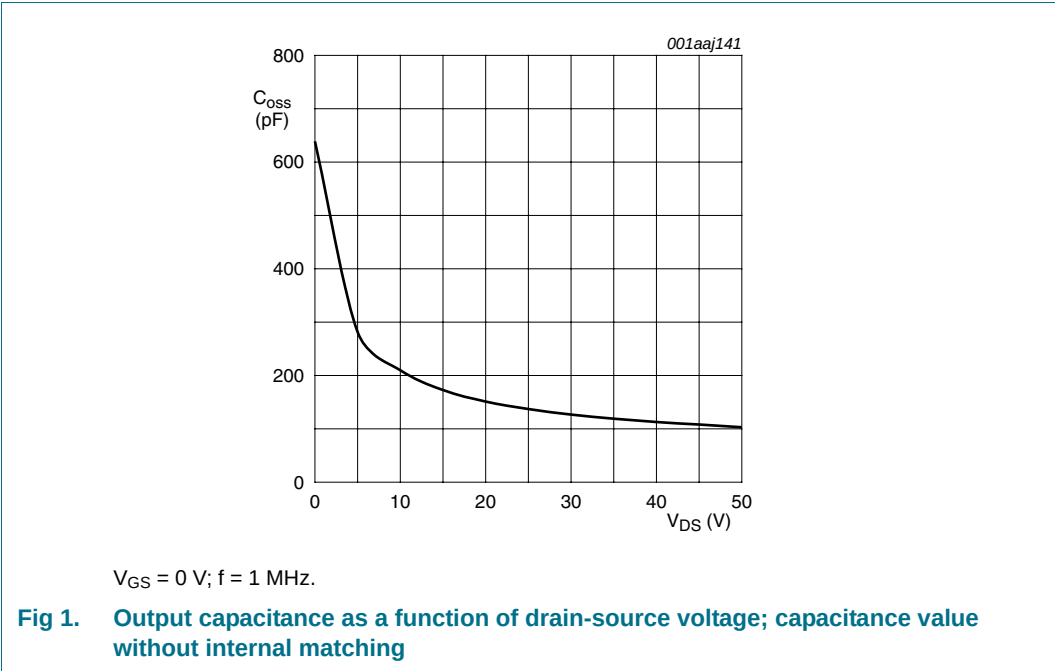
$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 3.75\text{ mA}$	110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 375\text{ mA}$	1.25	1.7	2.25	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 50\text{ V}; I_D = 900\text{ mA}$	1.45	1.95	2.45	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}$	-	-	4.2	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V};$ $V_{DS} = 10\text{ V}$	44	56	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	420	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 18.75\text{ A}$	-	20	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V};$ $I_D = 12.49\text{ A}$	-	0.09	-	Ω
C_{rs}	feedback capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V};$ $f = 1\text{ MHz}$	-	2.3	-	pF
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V};$ $f = 1\text{ MHz}$	-	300	-	pF
C_{oss}	output capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V};$ $f = 1\text{ MHz}$	-	103	-	pF

Table 7. RF characteristics

Mode of operation: CW; $f = 225\text{ MHz}$; RF performance at $V_{DS} = 50\text{ V}; I_{Dq} = 900\text{ mA}; T_{case} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_L = 300\text{ W}$	26	27.2	28.4	dB
RL_{in}	input return loss	$P_L = 300\text{ W}$	10	13	-	dB
η_D	drain efficiency	$P_L = 300\text{ W}$	67	70	-	%



6.1 Ruggedness in class-AB operation

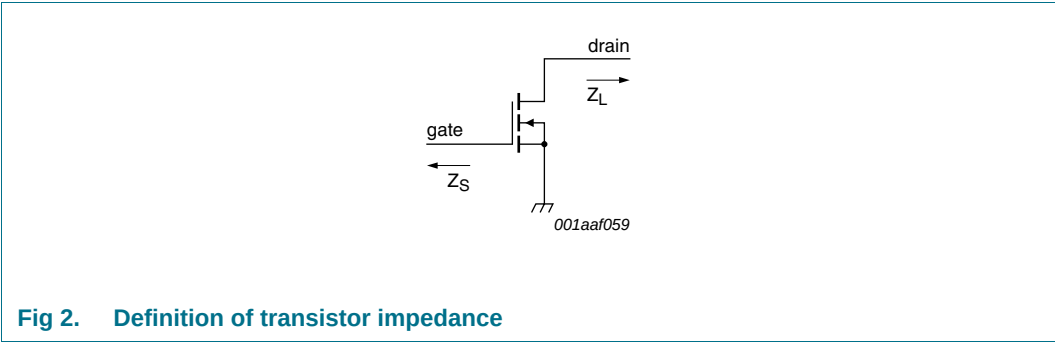
The BLF573 and BLF573S are capable of withstanding a load mismatch corresponding to $V_{SWR} = 13 : 1$ through all phases under the following conditions: $V_{DS} = 50\text{ V}$; $I_{Dq} = 900\text{ mA}$; $P_L = 300\text{ W}$; $f = 225\text{ MHz}$.

7. Application information

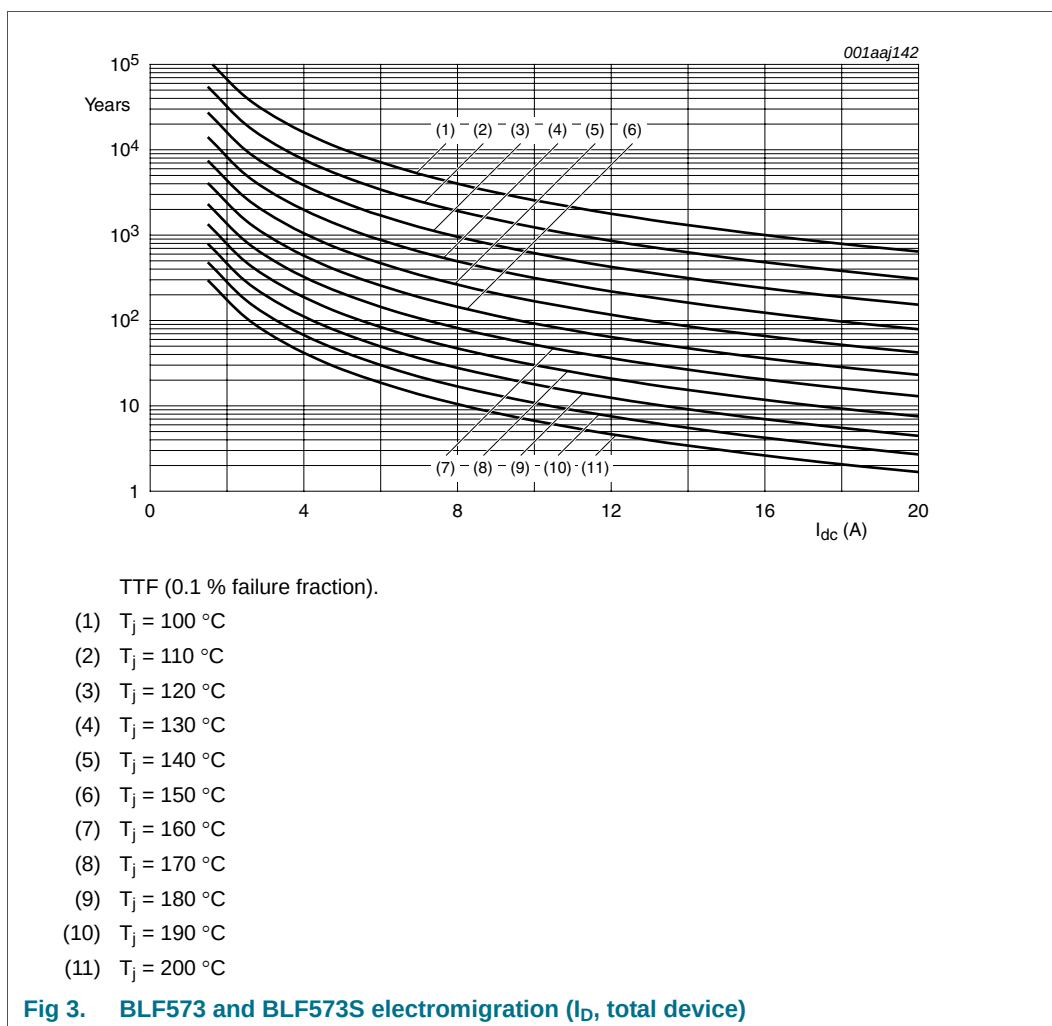
7.1 Impedance information

Table 8. Typical impedance
Measured Z_S and Z_L test circuit impedances.

f	Z_S	Z_L
MHz	Ω	Ω
225	$0.7 + j2.0$	$1.95 + j2.0$



7.2 Reliability

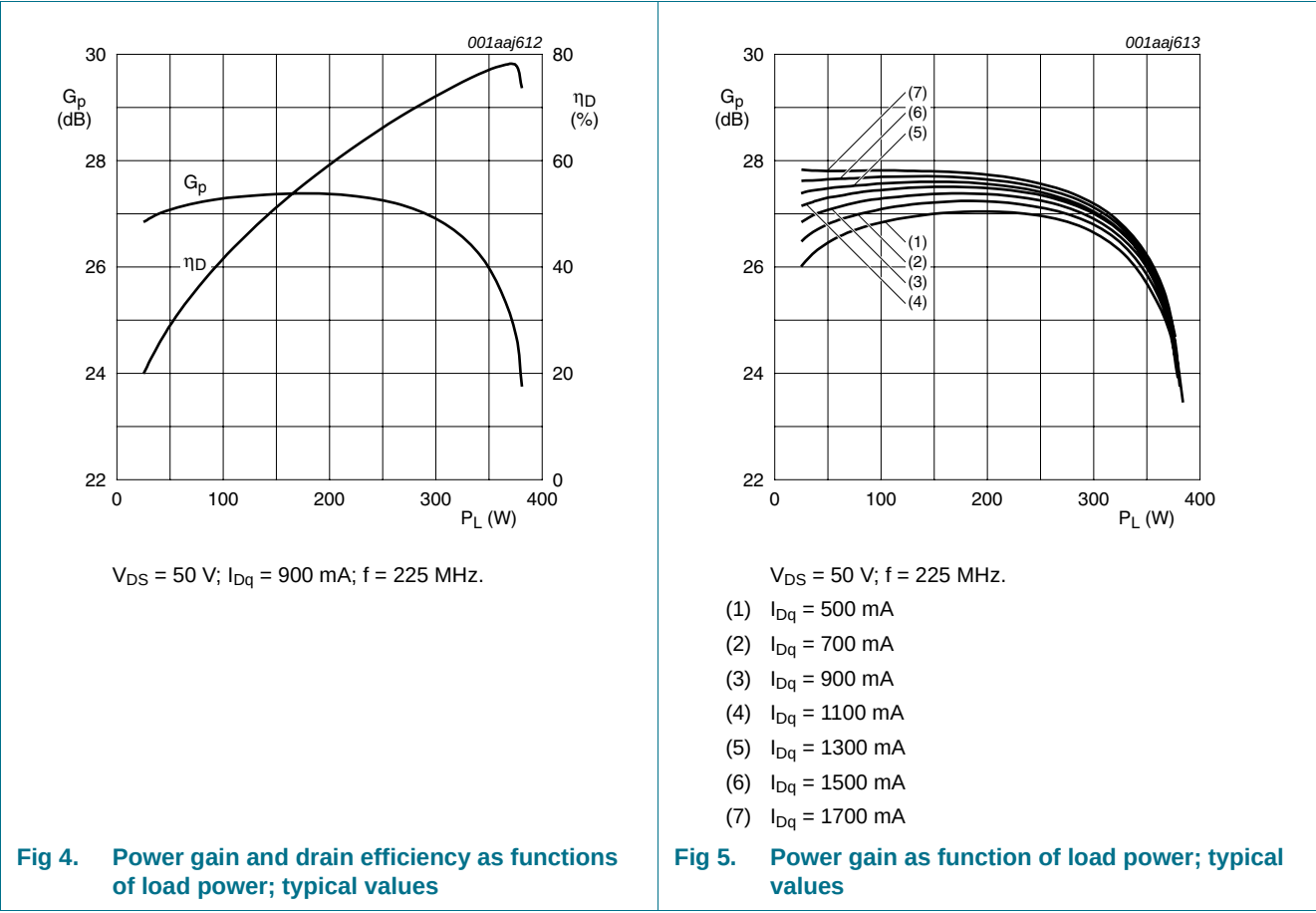


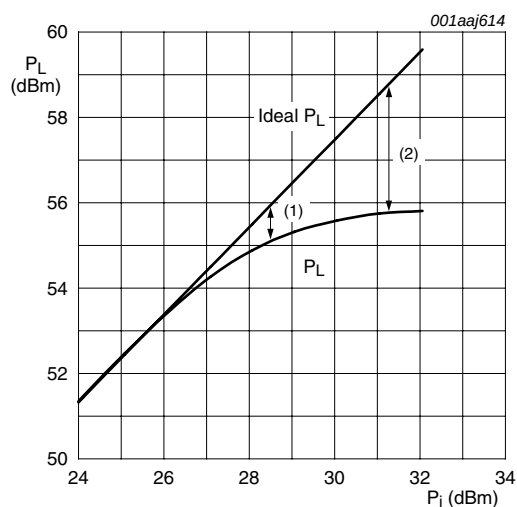
8. Test information

8.1 RF Performance

The following figures are measured in a class-AB production test circuit.

8.1.1 1-Tone CW



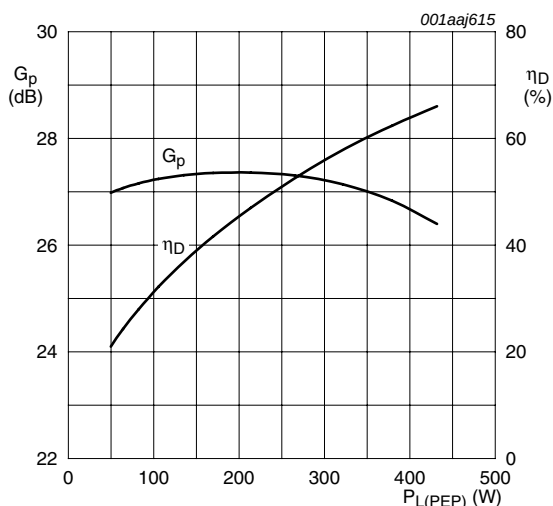


$V_{DS} = 50 \text{ V}$; $I_{DQ} = 900 \text{ mA}$; $f = 225 \text{ MHz}$.

- (1) $P_{L(1dB)} = 55.2 \text{ dBm}$ (330 W)
- (2) $P_{L(3dB)} = 55.8 \text{ dBm}$ (380 W)

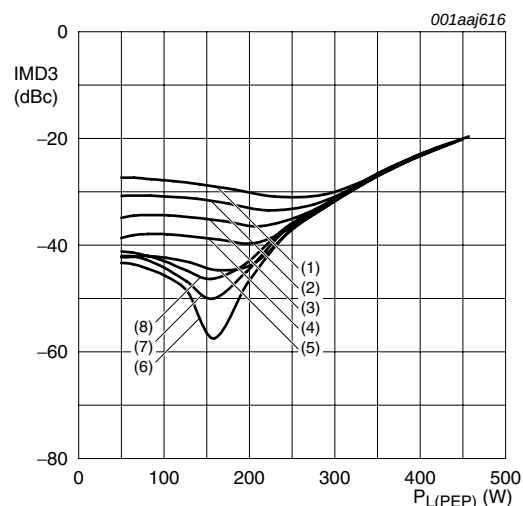
Fig 6. Load power as function of input power; typical values

8.1.2 2-Tone CW



$V_{DS} = 50 \text{ V}$; $I_{DQ} = 900 \text{ mA}$; $f_1 = 224.95 \text{ MHz}$;
 $f_2 = 225.05 \text{ MHz}$.

Fig 7. Power gain and drain efficiency as functions of peak envelope load power; typical values



$V_{DS} = 50 \text{ V}$; $f_1 = 224.95 \text{ MHz}$; $f_2 = 225.05 \text{ MHz}$.

- (1) $I_{DQ} = 500 \text{ mA}$
- (2) $I_{DQ} = 700 \text{ mA}$
- (3) $I_{DQ} = 900 \text{ mA}$
- (4) $I_{DQ} = 1100 \text{ mA}$
- (5) $I_{DQ} = 1300 \text{ mA}$
- (6) $I_{DQ} = 1500 \text{ mA}$
- (7) $I_{DQ} = 1700 \text{ mA}$
- (8) $I_{DQ} = 1800 \text{ mA}$

Fig 8. Third order intermodulation distortion as a function of peak envelope load power; typical values

8.2 Test circuit

Table 9. List of components

For production test circuit, see [Figure 9](#) and [Figure 10](#).

Printed-Circuit Board (PCB): Rogers 5880; $\epsilon_r = 2.2 \text{ F/m}$; height = 0.79 mm; Cu (top/bottom metallization); thickness copper plating = 35 μm .

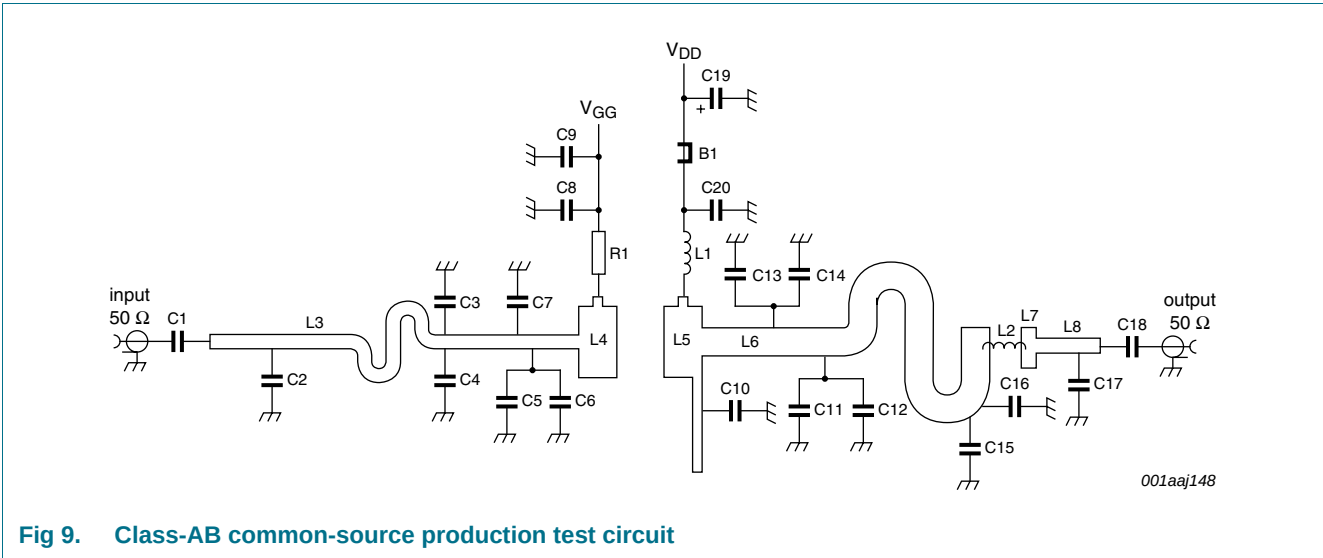
Component	Description	Value	Remarks
B1	ferrite SMD bead	100 Ω ; 100 MHz	Ferroxcube BDS3/3/8.9-4S2 or equivalent
C1, C18	multilayer ceramic chip capacitor	100 pF	[1]
C2	multilayer ceramic chip capacitor	39 pF	[1]
C3, C4	multilayer ceramic chip capacitor	180 pF	[1]
C5, C6, C7	multilayer ceramic chip capacitor	220 pF	[1]
C8, C20	multilayer ceramic chip capacitor	1 nF	[1]
C9	multilayer ceramic chip capacitor	4.7 μF	TDK C4532X7R1E475MT020U or equivalent
C10	multilayer ceramic chip capacitor	30 pF	[1]
C11, C12, C13	multilayer ceramic chip capacitor	51 pF	[1]
C14	multilayer ceramic chip capacitor	43 pF	[1]

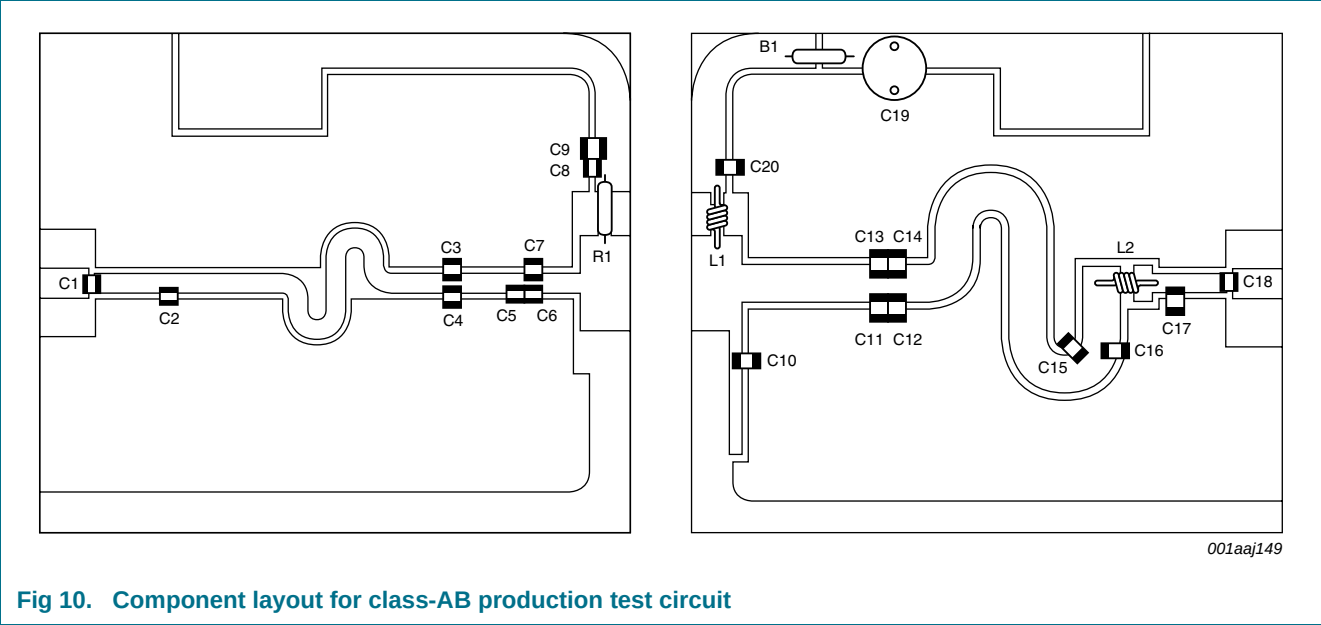
Table 9. List of components ...continued

For production test circuit, see Figure 9 and Figure 10.
Printed-Circuit Board (PCB): Rogers 5880; $\epsilon_r = 2.2$ F/m; height = 0.79 mm; Cu (top/bottom metallization);
thickness copper plating = 35 μm .

Component	Description	Value	Remarks
C15	multilayer ceramic chip capacitor	33 pF	[1]
C16	multilayer ceramic chip capacitor	36 pF	[1]
C17	multilayer ceramic chip capacitor	16 pF	[1]
C19	electrolytic capacitor	220 μF ; 63 V	
L1	2 turns enamelled copper wire	D = 3 mm; d = 1 mm; length = 2 mm; leads = 2 $\times$ 6 mm	
L2	4 turns enamelled copper wire	D = 2 mm; d = 1 mm; length = 13 mm; leads = 2 $\times$ 5 mm	
L3	stripline	-	(L $\times$ W) 96 mm $\times$ 3 mm
L4, L5	stripline	-	(L $\times$ W) 15 mm $\times$ 8 mm
L6	stripline	-	(L $\times$ W) 105 mm $\times$ 6 mm
L7	stripline	-	(L $\times$ W) 3 mm $\times$ 6 mm
L8	stripline	-	(L $\times$ W) 12 mm $\times$ 6 mm
R1	metal film resistor	100 Ω ; 0.6 W	

[1] American Technical Ceramics type 100B or capacitor of same quality.





9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A

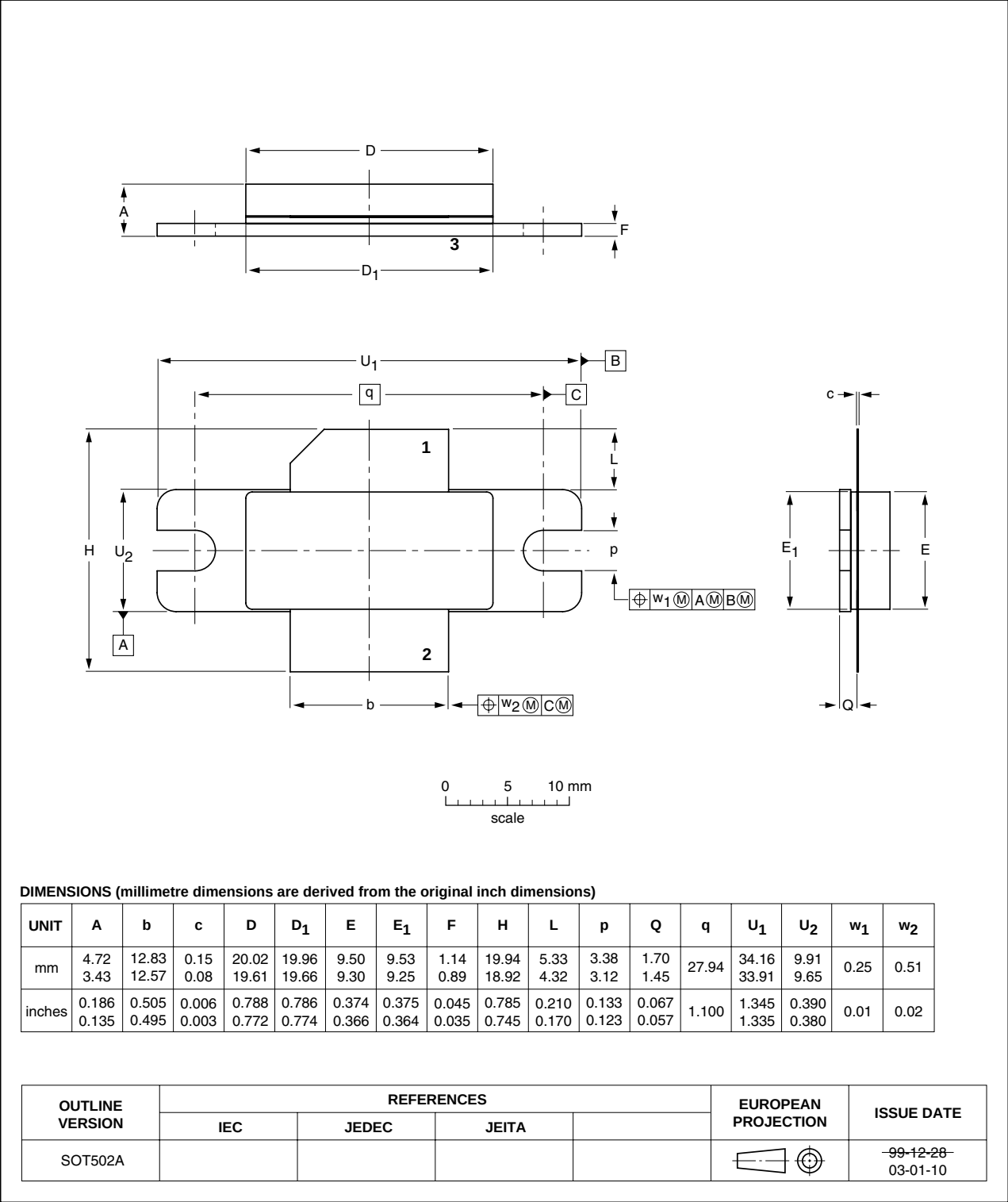
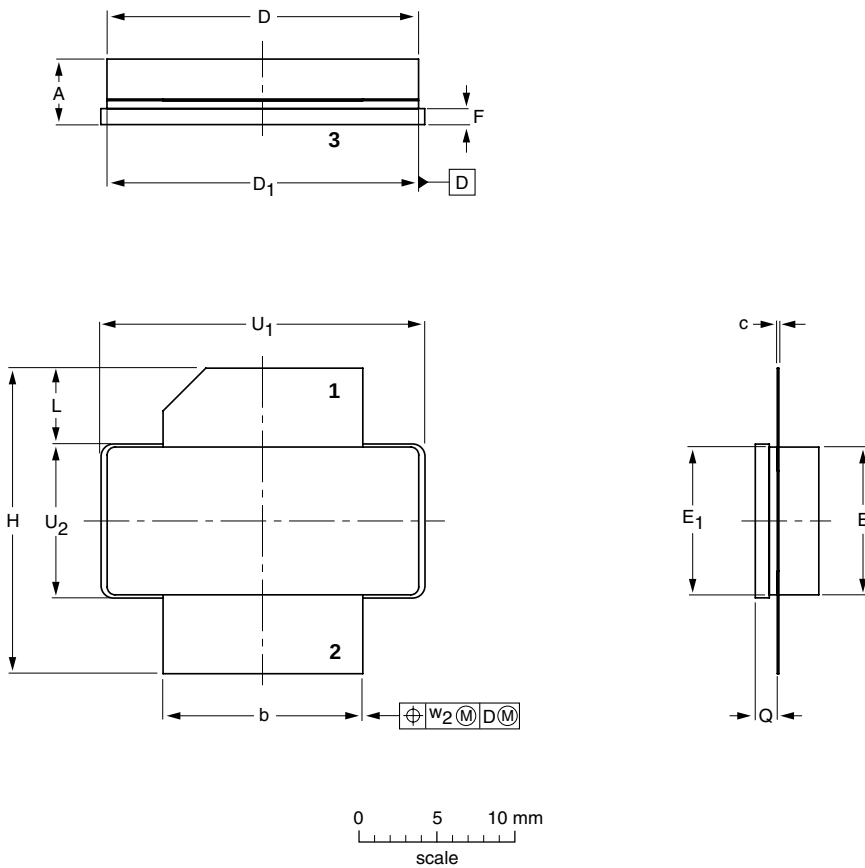


Fig 11. Package outline SOT502A

Earless flanged LDMOST ceramic package; 2 leads

SOT502B



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	Q	U ₁	U ₂	w ₂
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						03-01-10- 07-05-09

Fig 12. Package outline SOT502B

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
EDGE	Enhanced Data rates for GSM Evolution
GSM	Global System for Mobile communications
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
SMD	Surface Mount Device
TTF	Time To Failure
VHF	Very High Frequency
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF573_BLF573S v.3	20100708	Product data sheet	-	BLF573S v.2
Modifications:	The document now describes both the eared and earless version of this product: BLF573 and BLF573S respectively.			
BLF573S v.2	20090217	Product data sheet	-	BLF573S v.1
BLF573S v.1	20081208	Preliminary data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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