

OLED DISPLAY MODULE

Product Specification

CUSTOMER	Standard	
PRODUCT NUMBER	DD-12864WE-4A	
CUSTOMER APPROVAL		Date

INTERNAL APPROVALS		
Product Mgr	Doc. Control	Electr. Eng
Bazile Peter	Anthony Perkins	Rekha Mani
Date: 20/10/09	Date: 20/10/09	Date: 20/10/09

TABLE OF CONTENTS

1	MAIN FEATURES	4
2	MECHANICAL SPECIFICATION.....	5
2.1	MECHANICAL CHARACTERISTICS	5
2.2	MECHANICAL DRAWING	6
3	ELECTRICAL SPECIFICATION.....	7
3.1	ABSOLUTE MAXIMUM RATINGS	7
3.2	ELECTRICAL CHARACTERISTICS	8
3.3	INTERFACE PIN ASSIGNMENT	9
3.4	BLOCK DIAGRAM	11
3.5	AC CHARACTERISTICS	13
4	OPTICAL SPECIFICATION.....	18
4.1	OPTICAL CHARACTERISTICS.....	18
5	FUNCTIONAL SPECIFICATION	19
5.1	COMMANDS	19
5.2	POWER UP/DOWN SEQUENCE.....	19
5.3	RESET CIRCUIT	19
5.4	ACTUAL APPLICATION EXAMPLE.....	20
6	PACKAGING AND LABELLING SPECIFICATION.....	21
6.1	LABELLING & MARKING.....	22
7	QUALITY ASSURANCE SPECIFICATION	22
7.1	CONFORMITY	22
7.2	DELIVERY ASSURANCE	22
7.3	DEALING WITH CUSTOMER COMPLAINTS	26
8	RELIABILITY SPECIFICATION	27
8.1	RELIABILITY TESTS	27
8.2	LIFE TIME	27
8.3	FAILURE CHECK STANDARD	27
9	PRECAUTIONS.....	28
9.1	HANDLING.....	28
9.2	STORAGE	29
9.3	DESIGNING	29
9.4	DISPOSING.....	29
9.5	OTHER.....	30

Product No.	DD-12864WE-4A	REV. A

Page	2 / 30
------	--------

REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	20 October 09			First Issue	

Product No.	DD-12864WE-4A	REV. A

Page	3 / 30
------	--------

1 MAIN FEATURES

ITEM	CONTENTS
Display Format	128 x 64 Dots
Overall Dimensions(W*H*T)	26.70×19.26× 1.45 mm
Active Area(W*H)	21.744 × 10.864 mm
Viewing Area(W*H)	23.744 x 12.864 mm
Display Mode	Passive Matrix (0.96'')
Display Colour	White Colour
Driving Method	1 / 64 duty
Driver IC	SSD1306
Operating temperature	-30°C ~ +70°C
Storage temperature	-40°C ~ +80°C

Product No.	DD-12864WE-4A	REV. A

Page	4 / 30
------	--------

2 MECHANICAL SPECIFICATION

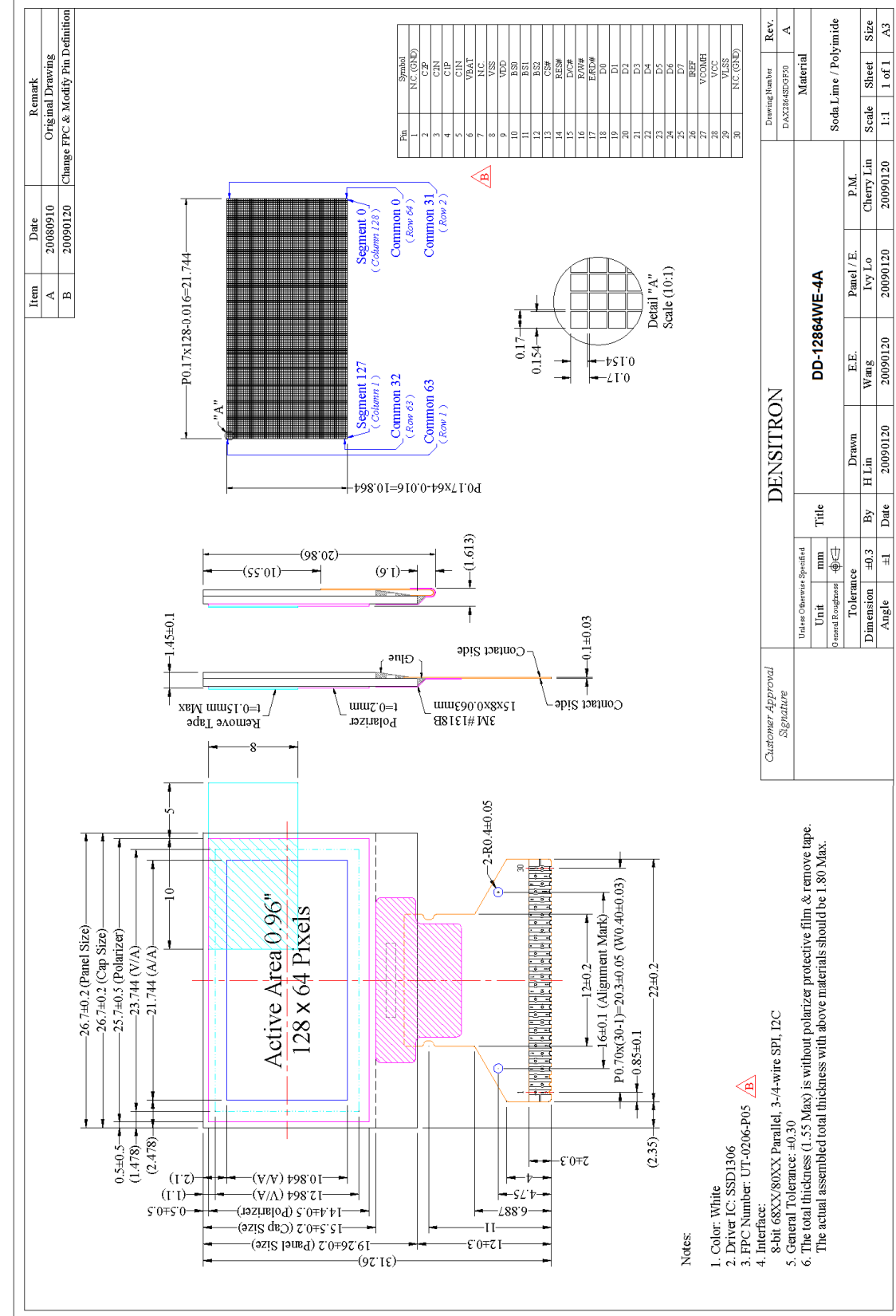
2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Display Format	128 x 64	Dots
Overall Dimensions	26.70×19.26× 1.45	mm
Viewing Area	23.744 x 12.864	mm
Active Area	21.744 × 10.864	mm
Dot Size	0.154 × 0.154	mm
Dot Pitch	0.17 × 0.17	mm
Weight	1.54	g
IC Controller/Driver	SSD1306	

Product No.	DD-12864WE-4A	REV. A

Page	5 / 30
------	--------

2.2 MECHANICAL DRAWING



Product No.	DD-12864WE-4A	REV. A

Page	6 / 30
------	--------

3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

VSS = 0 V, Ta = 25 °C

Item	Symbol	Min	Max	Unit	Note
Supply Voltage for Operation	V _{DD}	-0.3	4	V	Note 1, 2
Supply Voltage for Display	V _{CC}	0	11	V	
Operating Temperature	T _{op}	-30	70	°C	
Storage Temperature	T _{stg}	-40	80	°C	
Static Electricity	Be sure that you are grounded when handling displays.				

Note 1: All the above voltages are on the basis of “VSS=0V”.

Note 2: When this module is used beyond above absolute maximum ratings, permanent damage to the module may occur. Also for normal operations it's desirable to use this module under the conditions according to Section 3.2 “Electrical Characteristics” and section 4 “optical characteristic. If this module is used beyond these conditions the module may malfunction and the reliability could deteriorate.

3.2 ELECTRICAL CHARACTERISTICS

3.2.1 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	2.8	3.3	V
Supply Voltage for Display	V_{CC}	Note 3	8.5	9	9.5	V
Supply Voltage for DC/DC	V_{BAT}	Internal DC/DC	3.5	-	4.2	V
Supply Voltage for Display (Generated by Internal DC/DC)	V_{CC}	Note 4	7	7.35	7.5	V
High Level Input	V_{IH}	-	$0.8 \times V_{DD}$	-	V_{DD}	V
Low Level Input	V_{IL}	-	0	-	$0.2 \times V_{DD}$	V
High Level Output	V_{OH}	$I_{out}=100\mu A, 3.3$ MHz	$0.9 \times V_{DD}$	-	V_{DD}	V
Low Level Output	V_{OL}	$I_{out}=100\mu A, 3.3$ MHz	0	-	$0.1 \times V_{DD}$	V
Operating Current for VDD	I_{DD}	-	-	180	300	μA
Operating Current for VCC	I_{CC}	Note 1	-	6	7.5	mA
		Note 2	-	10.8	13.5	mA
Operating Current for VBAT(VCC Generated by Internal DC/DC)	I_{BAT}	Note 5	-	11.6	14.5	mA
		Note 2	-	20.9	26.1	mA
Sleep Mode Current for VCI	$I_{DD, SLEEP}$	-	-	1	5	μA
Sleep Mode Current for VCC	$I_{CC, SLEEP}$	-	-	1	5	μA

Note 1 $V_{DD}=2.8V$, $V_{CC}=9V$, 50% Display area turned on.

Note 2 $V_{DD}=2.8V$, $V_{CC}=9V$, 100% Display area turned on

Note 3 Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) is subject to the change of the panel characteristics and the customer's request.

Note 4 $V_{DD}=2.8V$, $V_{CC}=7.35V$, 50% Display area turned on.

Note 5 $V_{DD}=2.8V$, $V_{CC}=7.35V$, 100% Display area turned on

Product No.	DD-12864WE-4A	REV. A

Page	8 / 30
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3.3 INTERFACE PIN ASSIGNMENT

No.	Symbol	I/O	Function																								
1	N.C. (GND)	-	Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.																								
2	C2P	I	Positive Terminal of the Flying Inverting Capacitor Negative Terminal of the Flying Boost Capacitor The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.																								
3	C2N	I																									
4	C1P	I																									
5	C1N	I																									
6	VBAT	P	Power Supply for DC/DC Converter Circuit This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to VDD when the converter is not used.																								
7	N.C.	-	Reserved Pin The NC pins between function pins are reserved for compatible and flexible design.																								
8	VSS	P	Ground of Logic Circuit This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.																								
9	VDD	P	Power Supply for Logic This is a voltage supply pin. It must be connected to external source																								
10	BS0	I	Communicating Protocol Select These pins are MCU interface selection input. See the following table: <table><tr><td></td><td>BS0</td><td>BS1</td><td>BS2</td></tr><tr><td>I2C</td><td>0</td><td>1</td><td>0</td></tr><tr><td>3-wire SPI</td><td>1</td><td>0</td><td>0</td></tr><tr><td>4-wire SPI</td><td>0</td><td>0</td><td>0</td></tr><tr><td>68XX-parallel</td><td>0</td><td>0</td><td>1</td></tr><tr><td>80XX-parallel</td><td>0</td><td>1</td><td>1</td></tr></table>		BS0	BS1	BS2	I2C	0	1	0	3-wire SPI	1	0	0	4-wire SPI	0	0	0	68XX-parallel	0	0	1	80XX-parallel	0	1	1
	BS0			BS1	BS2																						
I2C	0			1	0																						
3-wire SPI	1			0	0																						
4-wire SPI	0			0	0																						
68XX-parallel	0	0		1																							
80XX-parallel	0	1	1																								
11	BS1																										
12	BS2																										
13	CS#	I	Chip Select This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.																								
14	RES#	I	Power Reset for Controller and Driver This pin is reset signal input.. When the pin is low, initialization of the chip is executed.																								

Product No.	DD-12864WE-4A	REV. A

Page	9 / 30
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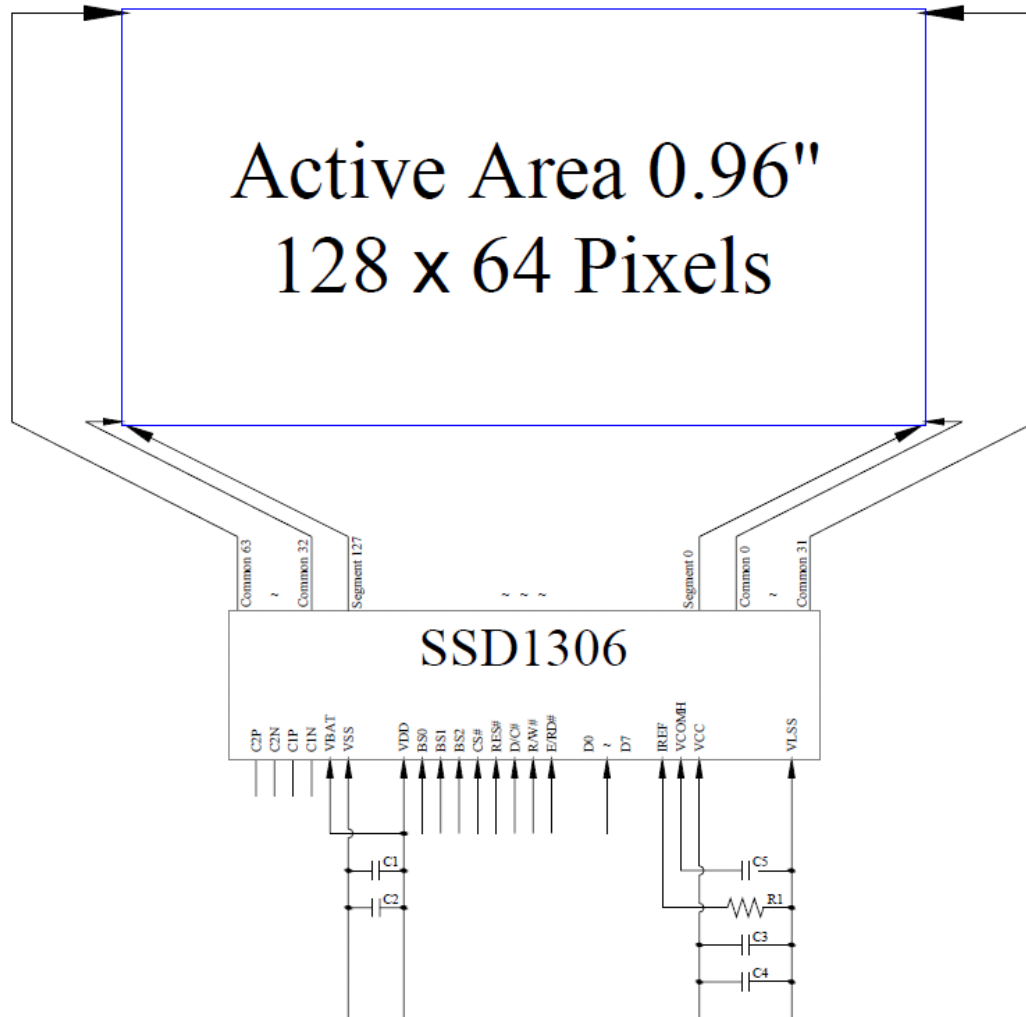
No.	Symbol	I/O	Function
15	D/C#	I	Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams. When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection.
16	R/W#	I	Read/Write Select or Write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
17	E/RD#	I	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
18~25	D7~D0	I/O	Host Data Input/output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2C mode is selected, D2 & D1 should be tied together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL.
26	IREF	I	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 12.5μA.
27	VCOMH	O	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
28	VCC	P	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be connected to external source when the converter is not used.
29	VLSS		Ground of Analogue Circuit This is an analogue ground pin. It should be connected to VSS externally.
30	N.C. (GND)	-	Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.

Product No.	DD-12864WE-4A	REV. A

Page	10 / 30
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3.4 BLOCK DIAGRAM

3.4.1 VCC SUPPLIED EXTERNAL



MCU Interface Selection:

Pins connected to MCU interface:

BS0, BS1 and BS2

CS#, RES#, D/C#, R/W#, E/RD#, and
D0~D7

C1, C3:

0.1μF

C2, C4, C5:

4.7μF

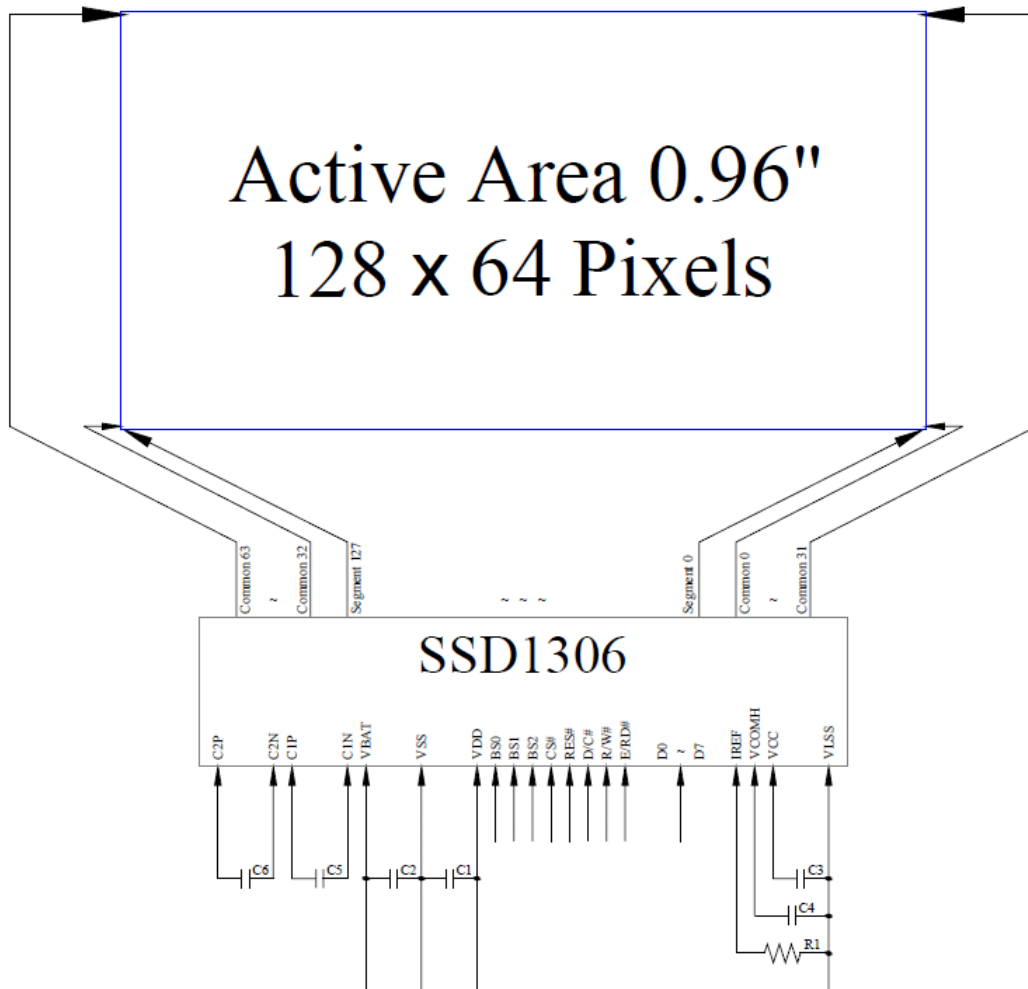
R1:

560kΩ, $R1 = (\text{Voltage at IREF} - VSS) / IREF$

Product No.	DD-12864WE-4A	REV. A

Page	11 / 30
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3.4.1 VCC SUPPLIED using internal DC/DC



MCU Interface Selection:

Pins connected to MCU interface:

BS0, BS1 and BS2

CS#, RES#, D/C#, R/W#, E/RD#, and
D0~D7

C1, C2, C5, C6:

1 μ F

C3, C4:

4.7 μ F

R1:

390k Ω , $R1 = (\text{Voltage at IREF} - VSS) / IREF$

Product No.	DD-12864WE-4A	REV. A

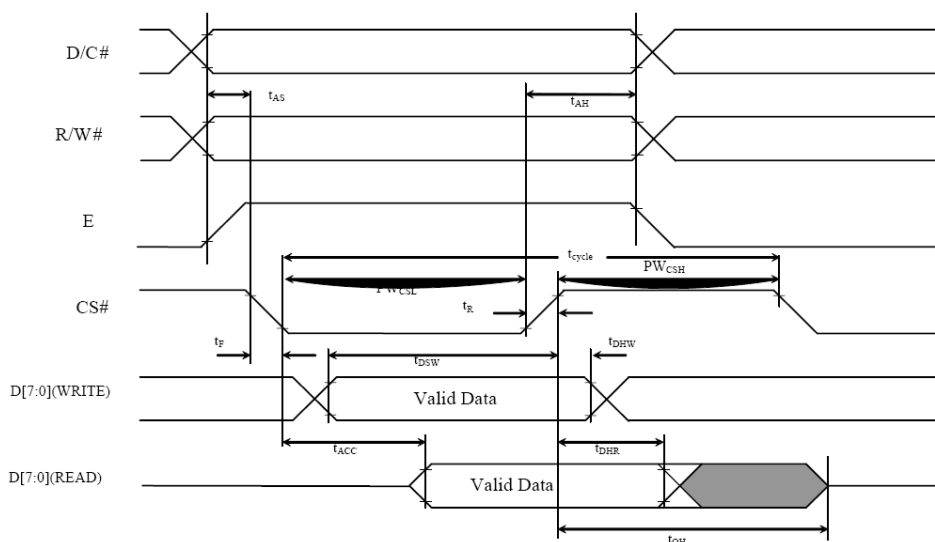
Page	12 / 30
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3.5 AC CHARACTERISTICS

3.5.1 68XX-Series MPU Parallel Interface Timing Characteristics

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t_{cycle}	300	-	ns
Address Setup Time	t_{AS}	0	-	ns
Address Hold Time	t_{AH}	0	-	ns
Write Data Setup Time	t_{DSW}	40	-	ns
Write Data Hold Time	t_{DHW}	7	-	ns
Read Data Hold Time	t_{DHR}	20	-	ns
Output Disable Time	t_{OH}	-	70	ns
Access Time	t_{ACC}	-	140	ns
Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	PW_{CSL}	120 60	-	ns
Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	PW_{CSH}	60 60	-	ns
Rise Time	t_{R}	-	40	ns
Fall Time	t_{F}	-	40	ns

($V_{\text{DD}} - V_{\text{SS}} = 1.65\text{V}$, $V_{\text{CI}} = 2.8\text{V}$, $T_{\text{a}} = 25^{\circ}\text{C}$)



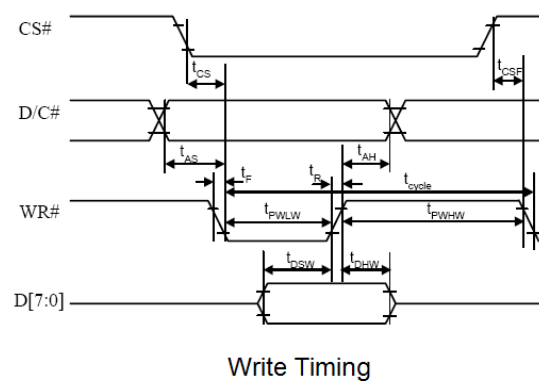
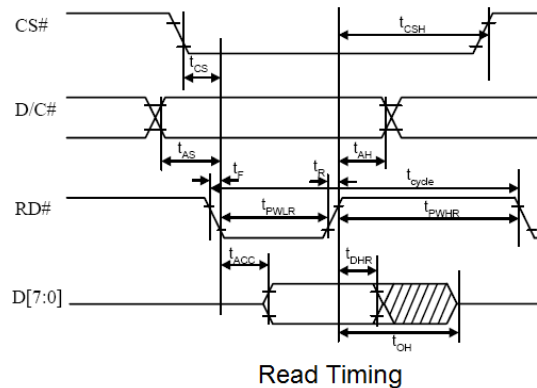
Product No.	DD-12864WE-4A	REV. A
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Page	13 / 30
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3.5.2 8080-Series MPU Parallel Interface Timing Characteristics

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t_{cycle}	300	-	ns
Address Setup Time	t_{AS}	10	-	ns
Address Hold Time	t_{AH}	0	-	ns
Write Data Setup Time	t_{DSW}	40	-	ns
Write Data Hold Time	t_{DHW}	7	-	ns
Read Data Hold Time	t_{DHR}	20	-	ns
Output Disable Time	t_{OH}	-	70	ns
Access Time	t_{ACC}	-	140	ns
Read Low Time	$t_{\text{PWL R}}$	120	-	ns
Write Low Time	$t_{\text{PWL W}}$	60	-	ns
Read High Time	$t_{\text{PWH R}}$	60	-	ns
Write High Time	$t_{\text{PWH W}}$	60	-	ns
Chip Select Setup Time	t_{CS}	0	-	ns
Chip Select Hold Time to Read Signal	t_{CSH}	0	-	ns
Chip Select Hold Time	t_{CSF}	20	-	ns
Rise Time	t_{R}	-	40	ns
Fall Time	t_{F}	-	40	ns

($V_{\text{DD}} - V_{\text{SS}}$ 1.65V to 2.8V, $T_a = 25^\circ\text{C}$)



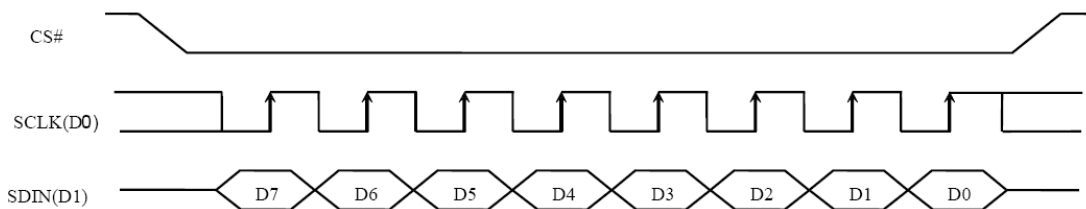
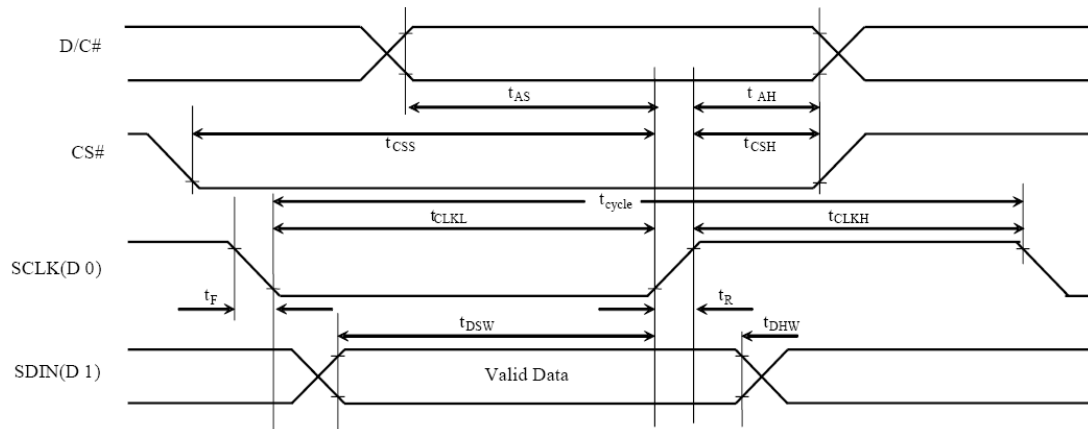
Product No.	DD-12864WE-4A	REV. A
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Page	14 / 30
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3.5.3 Serial Interface Timing Characteristics (4-wire SPI)

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t_{cycle}	100	-	ns
Address Setup Time	t_{AS}	15	-	ns
Address Hold Time	t_{AH}	15	-	ns
Chip Select Setup Time	t_{CSS}	20	-	ns
Chip Select Hold Time	t_{CSH}	10	-	ns
Write Data Setup Time	t_{DSW}	15	-	ns
Write Data Hold Time	t_{DHW}	15	-	ns
Clock Low Time	t_{CLKL}	20	-	ns
Clock High Time	t_{CLKH}	20	-	ns
Rise Time	t_{R}	-	15	ns
Fall Time	t_{F}	-	15	ns

(VDD – VSS = 1.65V to 3.3V, Ta = 25°C)



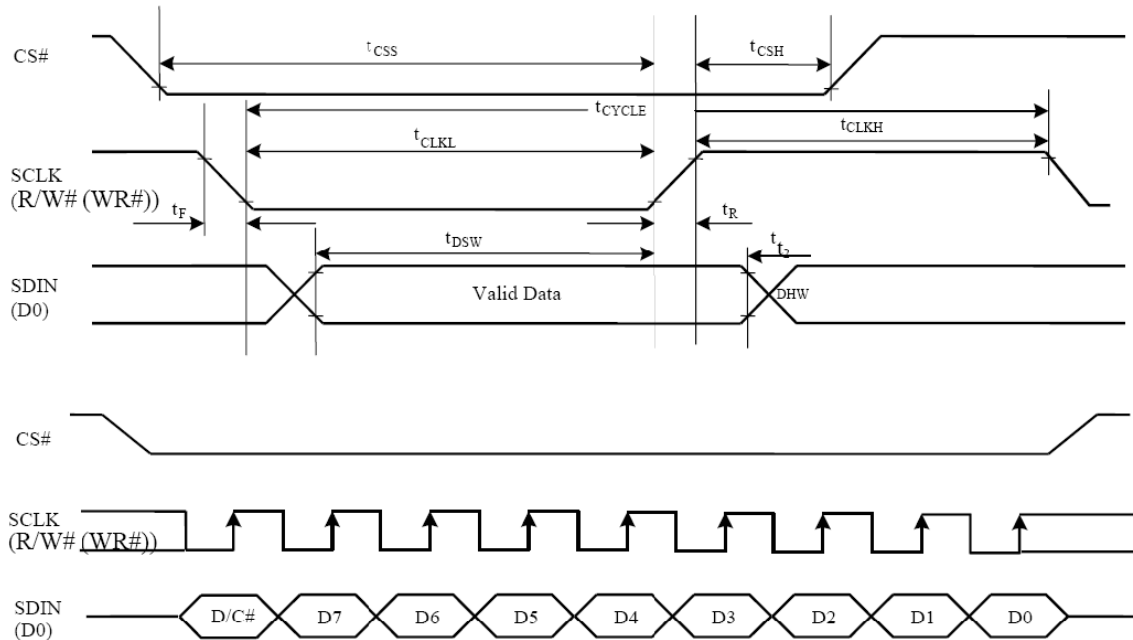
Product No.	DD-12864WE-4A	REV. A
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Page	15 / 30
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3.5.4 Serial Interface Timing Characteristics (3-wire SPI)

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t_{cycle}	100	-	ns
Chip Select Setup Time	t_{CSS}	20	-	ns
Chip Select Hold Time	t_{CSH}	10	-	ns
Write Data Setup Time	t_{DSW}	15	-	ns
Write Data Hold Time	t_{DHW}	15	-	ns
Clock Low Time	t_{CLKL}	20	-	ns
Clock High Time	t_{CLKH}	20	-	ns
Rise Time	t_{R}	-	40	ns
Fall Time	t_{F}	-	40	ns

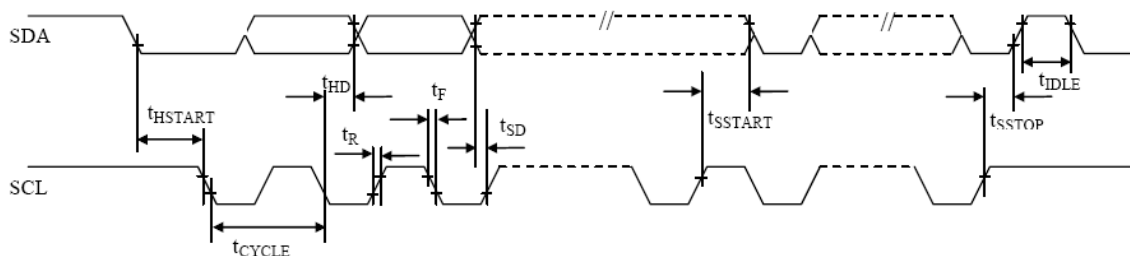
(VDD – VSS = 1.65V to 3.3, Ta = 25°C)



3.5.1 I2C Timing Characteristics

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t_{cycle}	2.5	-	us
Start Condition Hold Time	t_{HSTART}	0.6	-	us
Data Hold Time (for “SDA _{OUT} ” Pin)	t_{HD}	0	-	us
Data Hold Time (for “SDA _{IN} ” Pin)		300		
Data Setup Time	t_{SD}	100	-	us
Start Condition Setup Time (Only relevant for a repeated Start condition)	t_{SSTART}	0.6	-	us
Stop Condition Setup Time	t_{SSTOP}	0.6	-	us
Rise Time for Data and Clock Pin	t_{R}	-	300	ns
Fall Time for Data and Clock Pin	t_{F}	-	300	ns
Idle Time before a New Transmission can Start	t_{IDLE}	1.3		us

(VDD – VSS = 1.65V to 3.3, Ta = 25°C)



Product No.	DD-12864WE-4A	REV. A

Page	17 / 30
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4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Brightness (V _{CC} Supplied Externally)	L _{br}	With Polarizer Note 1	80	100	-	cd/m ²
Brightness (V _{CC} Generated internally)	L _{br}	With Polarizer Note 2	50	60	-	cd/m ²
C.I.E.(White)	(X)	Without Polarizer	0.28	0.32	0.36	-
	(Y)		0.29	0.33	0.37	
Dark Room Contrast	CR		-	>2000:1	-	-
Viewing Angle			>160	-	-	degree

Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 9V & 7.35V
 Software configuration follows Section 5.4 Initialization.

Product No.	DD-12864WE-4A	REV. A

Page	18 / 30
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5 FUNCTIONAL SPECIFICATION

5.1 COMMANDS

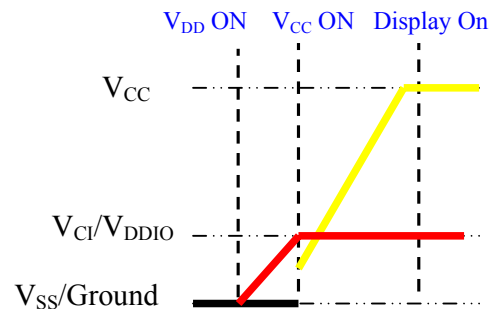
Please refer to the Technical Manual for the SSD1306

5.2 POWER UP/DOWN SEQUENCE

To protect panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the panel enough time to complete the action of charge and discharge before/after the operation.

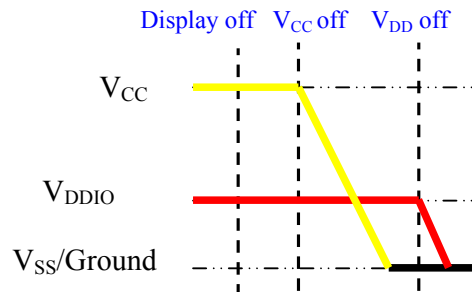
5.2.1 POWER UP SEQUENCE

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
(When V_{CC} is stable)
7. Send Display on command



5.2.2 POWER DOWN SEQUENCE

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
(When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DDIO}



5.3 RESET CIRCUIT

When RES# input is low, the chip is initialized with the following status:

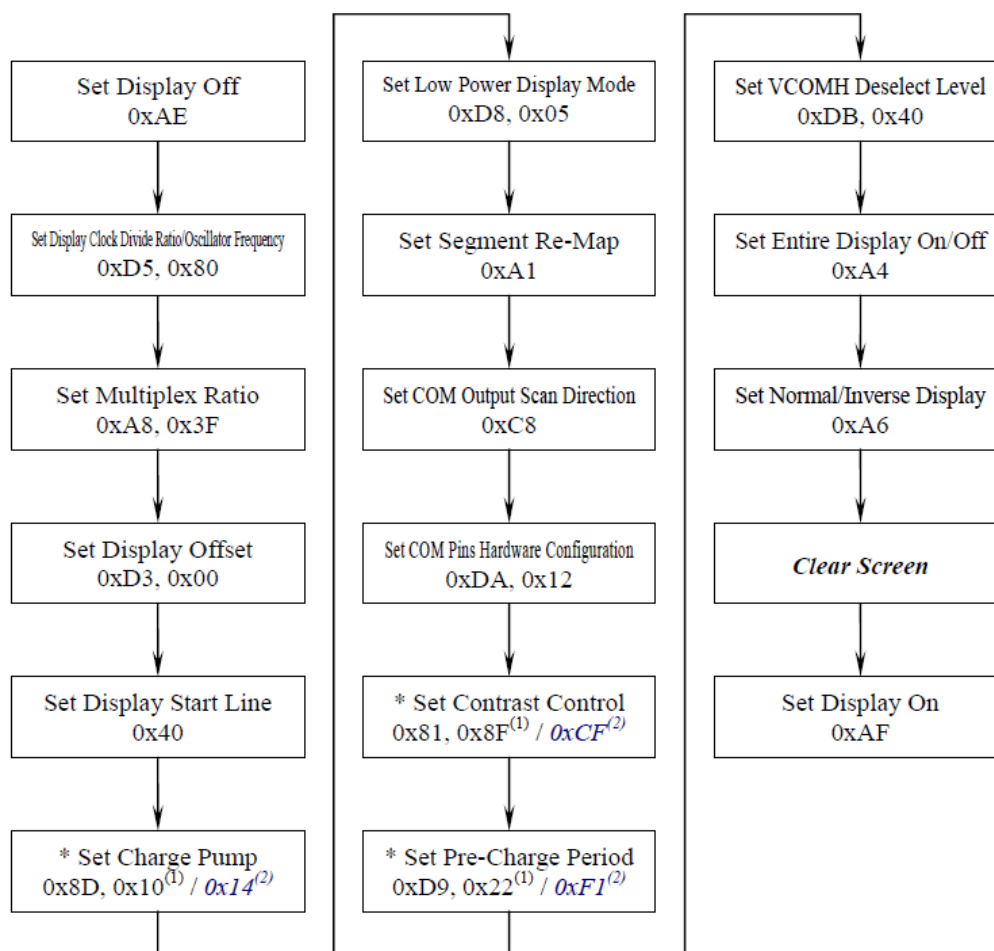
1. Display is OFF
2. 128×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

Product No.	DD-12864WE-4A	REV. A

Page	19 / 30
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5.4 ACTUAL APPLICATION EXAMPLE

Command usage and explanation of an actual example



Written Value for Parameters

(1) VCC Supplied Externally

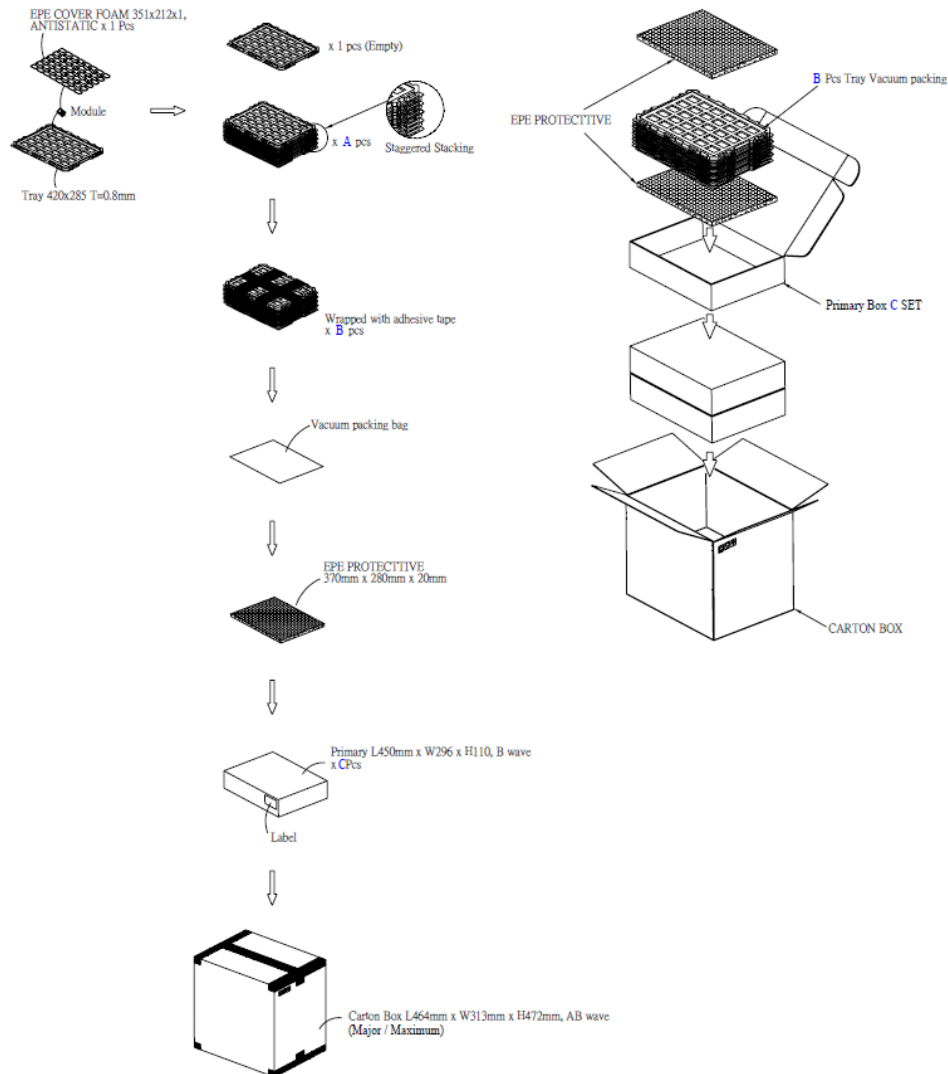
(2) VCC Generated by Internal DC/DC Circuit

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

Product No.	DD-12864WE-4A	REV. A

Page	20 / 30
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6 PACKAGING AND LABELLING SPECIFICATION



Item		Quantity	
Holding Trays	(A)	15	per Primary Box
Total Trays	(B)	16	per Primary Box (Including 1 Empty Tray)
Primary Box	(C)	1~4	per Carton (4 as Major / Maximum)

Product No.	DD-12864WE-4A	REV. A

Page	21 / 30
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6.1 LABELLING & MARKING

DENSITRON DD-12864WE-4A TW YY MM
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7 QUALITY ASSURANCE SPECIFICATION

7.1 CONFORMITY

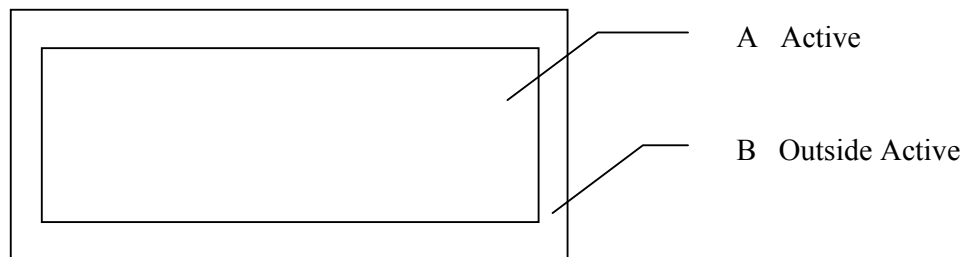
The performance, function and reliability of the shipped products conform to the Product Specification.

7.2 DELIVERY ASSURANCE

7.2.1 DELIVERY INSPECTION STANDARDS

IPC-AA610, class 2 electronic assembly's standard

7.2.2 Zone definition



7.2.3 Visual inspection

Test and measurement to be conducted under following conditions

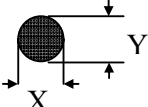
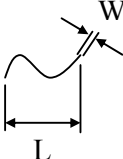
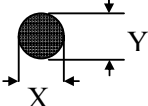
Temperature:	23±5°C
Humidity:	55±15%RH
Fluorescent lamp:	30 W
Distance between the Panel & Eyes of the Inspector:	≥30cm
Distance between the Panel & the lamp:	≥50cm

Product No.	DD-12864WE-4A	REV. A

Page	22 / 30
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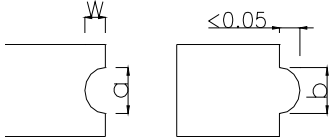
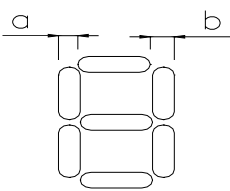
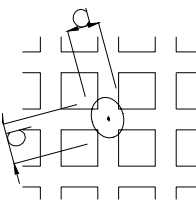
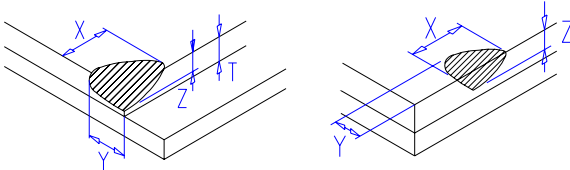
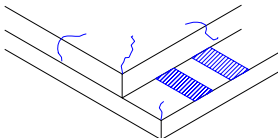
7.2.4 Standard of appearance inspection

Units: mm

Class	Item	Criteria																																			
Minor	Packing & Label	Outside & inside package	Presence of product no., lot no., quantity																																		
Critical		Product must not be mixed with others and quantity must not be different from that indicated on the label																																			
Major	Dimension	Product dimensions must be according to specification and drawing																																			
Major	Electrical	Product electrical characteristics must be according to specification																																			
Critical	OLED Display	Missing lines, short circuits or wrong patterns on OLED display are not allowed																																			
Minor	Black spot, white spot, dust	Round type: as per following drawing $\varnothing = (X+Y)/2$  <table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>$\varnothing < 0.1$</td><td>Any number</td><td rowspan="4">Any number</td></tr><tr><td>$0.1 < \varnothing < 0.2$</td><td>3</td></tr><tr><td>$0.2 < \varnothing < 0.25$</td><td>1</td></tr><tr><td>$0.25 < \varnothing$</td><td>0</td></tr></table> Line type: as per following drawing  <table><tr><th colspan="4">Acceptable quantity</th></tr><tr><th>Length</th><th>Width</th><th>Zone A</th><th>Zone B</th></tr><tr><td>--</td><td>$W \leq 0.05$</td><td>Any number</td><td rowspan="3">Any number</td></tr><tr><td>$L \leq 2.0$</td><td>$W \leq 0.1$</td><td>3</td></tr><tr><td>$L > 2.0$</td><td></td><td>0</td></tr></table> Total acceptable quantity: 3			Acceptable quantity			Size	Zone A	Zone B	$\varnothing < 0.1$	Any number	Any number	$0.1 < \varnothing < 0.2$	3	$0.2 < \varnothing < 0.25$	1	$0.25 < \varnothing$	0	Acceptable quantity				Length	Width	Zone A	Zone B	--	$W \leq 0.05$	Any number	Any number	$L \leq 2.0$	$W \leq 0.1$	3	$L > 2.0$		0
Acceptable quantity																																					
Size	Zone A	Zone B																																			
$\varnothing < 0.1$	Any number	Any number																																			
$0.1 < \varnothing < 0.2$	3																																				
$0.2 < \varnothing < 0.25$	1																																				
$0.25 < \varnothing$	0																																				
Acceptable quantity																																					
Length	Width	Zone A	Zone B																																		
--	$W \leq 0.05$	Any number	Any number																																		
$L \leq 2.0$	$W \leq 0.1$	3																																			
$L > 2.0$		0																																			
Minor	Polariser scratch	Scratch on protective film is permitted Scratch on polariser: same as No. 1																																			
Minor	Polariser bubble	$\varnothing = (X+Y)/2$  <table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>$\varnothing < 0.5$</td><td>Any number</td><td rowspan="2">Any number</td></tr><tr><td>$\varnothing > 0.5$</td><td>0</td></tr></table>			Acceptable quantity			Size	Zone A	Zone B	$\varnothing < 0.5$	Any number	Any number	$\varnothing > 0.5$	0																						
Acceptable quantity																																					
Size	Zone A	Zone B																																			
$\varnothing < 0.5$	Any number	Any number																																			
$\varnothing > 0.5$	0																																				

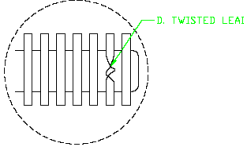
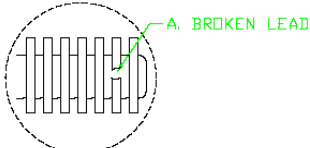
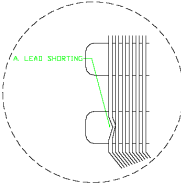
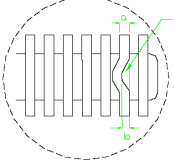
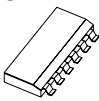
Product No.	DD-12864WE-4A	REV. A

Page	23 / 30
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Class	Item	Criteria																												
Minor	Segment deformation	1b. Pin hole on dot matrix display  <table><tr><th colspan="2">Acceptable quantity</th></tr><tr><th>Size</th><th></th></tr><tr><td>a,b<0.1</td><td>Any number</td></tr><tr><td>(a+b)/2<0.1</td><td>Any number</td></tr><tr><td>0.5<Ø<1.0</td><td>3</td></tr></table> Total acceptable quantity: 7 2. Segments / dots with different width  <table><tr><th colspan="2">Acceptable</th></tr><tr><td>a≥b</td><td>a/b≤4/3</td></tr><tr><td>a<b</td><td>a/b>4/3</td></tr></table> 3. Alignment layer defect Ø = (a+b)/2  <table><tr><th colspan="2">Acceptable quantity</th></tr><tr><th>Size</th><th></th></tr><tr><td>Ø≤0.4</td><td>Any number</td></tr><tr><td>0.4<Ø≤1.0</td><td>5</td></tr><tr><td>1.0<Ø≤1.5</td><td>3</td></tr><tr><td>1.5<Ø≤2.0</td><td>2</td></tr></table> Total acceptable quantity: 7	Acceptable quantity		Size		a,b<0.1	Any number	(a+b)/2<0.1	Any number	0.5<Ø<1.0	3	Acceptable		a≥b	a/b≤4/3	a<b	a/b>4/3	Acceptable quantity		Size		Ø≤0.4	Any number	0.4<Ø≤1.0	5	1.0<Ø≤1.5	3	1.5<Ø≤2.0	2
Acceptable quantity																														
Size																														
a,b<0.1	Any number																													
(a+b)/2<0.1	Any number																													
0.5<Ø<1.0	3																													
Acceptable																														
a≥b	a/b≤4/3																													
a<b	a/b>4/3																													
Acceptable quantity																														
Size																														
Ø≤0.4	Any number																													
0.4<Ø≤1.0	5																													
1.0<Ø≤1.5	3																													
1.5<Ø≤2.0	2																													
Minor	Panel Chipping	X ≤ 1/6 Panel length Y ≤ 1 Z ≤ T 																												
Minor	Panel Cracking	Cracks not allowed 																												
Minor	Copper exposed (pin or film)	Not allowed if visible by eye inspection																												
Minor	Film or Trace Damage	Not allowed if affect electrical function																												

Product No.	DD-12864WE-4A	REV. A

Page	24 / 30
------	---------

Class	Item	Criteria			
Minor	Contact Lead Twist	Not allowed			
Minor	Contact Lead Broken	Not allowed			
Minor	Contact Lead Bent	Not allowed if bent lead causes short circuit			
		Not allowed if bent lead extends horizontally more than 50% of its width			
Minor	Colour uniformity	Level of sample for approval set as limit sample			
Major	 PCB	No unmelted solder paste should be present on PCB			
Critical		Cold solder joints, missing solder connections, or oxidation are not allowed			
Minor		No residue or solder balls on PCB are allowed			
Critical		Short circuits on components are not allowed			
Minor	Tray particles		Size		Quantity
			On tray	$\varnothing < 0.2$	Any number
				$\varnothing > 0.25$	4
			On display	$\varnothing \geq 0.25$	2
				L = 3	1

Product No.	DD-12864WE-4A	REV. A

Page	25 / 30
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7.3 DEALING WITH CUSTOMER COMPLAINTS

7.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.
After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.

If the analysis cannot be completed on time, Densitron must inform the purchaser.

7.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.

Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.

Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

Product No.	DD-12864WE-4A	REV. A

Page	26 / 30
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8 RELIABILITY SPECIFICATION

8.1 RELIABILITY TESTS

Test Item	Test Condition	Evaluation and assessment
High Temperature Operation	70°C±2, 240 hours	The operational functions work
Low Temperature Operation	-30°C±2, 240 hours	
High Temperature Storage	80°C±2, 240 hours	
Low Temperature Storage	-40°C±2, 240 hours	
High Temperature & High Humidity Storage(Operation)	60°C±2, 90%RH, 120 hours	
Thermal Shock	-40°C to 85°C, 24 cycles 1 Hour	

- The samples used for above tests do not include polarizer.
- No moisture condensation is observed during tests.

8.1.1 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5 °C;55±15% RH

8.2 LIFE TIME

Item	Description
1	Function, performance, appearance, etc. shall be free from remarkable deterioration more than 10,000 hours under ordinary operating conditions of room temperature (25±10 °C), normal humidity (50% RH), and in area not exposed to direct sunlight. Storage Life time is 20,000 hr under room temperature (25±10 °C), normal humidity (50% RH)
2	End of lifetime is specified as 50% of initial brightness.

8.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

Product No.	DD-12864WE-4A	REV. A

Page	27 / 30
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9 PRECAUTIONS

9.1 Handling

Safety

If the panel breaks, be careful not to get the organic substance in your mouth or in your eyes.
If the organic substance touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design

Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.

Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during OLED cleaning

Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotrifluoroethane.

Do not wipe the display surface with dry or hard materials that will damage the polariser surface.

Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge

As the display uses C-MOS LSI drivers, connect any unused input terminal to V_{DD} or V_{SS} . Do not input any signals before power is turned on.

Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging

Displays use OLED elements, and must be treated as such. Avoid strong shock and drop from a height.

To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation

It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life.

Other Precautions

When a display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.

Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored.

Also, there will be no problem in the reliability of the module.

Storage

Store the display in a dark place where the temperature is $25^{\circ}\text{C} \pm 10^{\circ}\text{C}$ and the humidity below 50%RH.

Store the display in a clean environment, free from dust, organic solvents and corrosive gases.

Do not crash, shake or jolt the display (including accessories).

Product No.	DD-12864WE-4A	REV. A

Page	28 / 30
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9.2 STORAGE

When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Factory.)

At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.

If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

9.3 DESIGNING

The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.

To prevent occurrence of malfunctioning by noise: pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.

We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VCI). (Recommend value: 0.5A)

Pay sufficient attention to avoid occurrence of mutual noise interference with the neighbouring devices.

As for EMI, take necessary measures on the equipment side basically.

When fastening the OEL display module, fasten the external plastic housing section.

If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.

The electric potential to be connected to the rear face of the IC chip should be as follows: SSD1351

* Connection (contact) to any other potential than the above may lead to rupture of the IC.

9.4 Disposing

Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

Product No.	DD-12864WE-4A	REV. A

Page	29 / 30
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9.5 Other

When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.

To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.

- * Pins and electrodes
- * Pattern layouts such as the COF

With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.

- * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
- * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.

Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.

We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

Product No.	DD-12864WE-4A	REV. A

Page	30 / 30
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