

N- and P-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
N-Channel	40	0.0355 at V _{GS} = 10 V	6.8	5.3
		0.0425 at V _{GS} = 4.5 V	6.2	
P-Channel	- 40	0.045 at V _{GS} = - 10 V	- 5.8	11.8
		0.062 at V _{GS} = - 4.5 V	- 5.0	

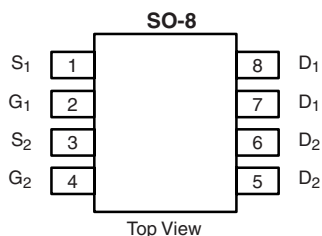
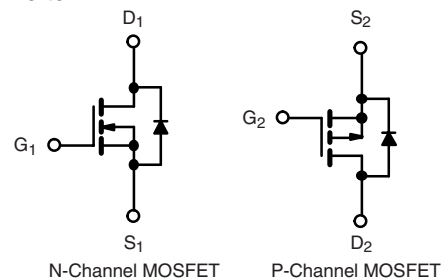
FEATURES

- Halogen-free
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested


RoHS
COMPLIANT

APPLICATIONS

- Backlight Inverter for LCD Display
- Full Bridge Converter


Ordering Information: Si4599DY-T1-GE3 (Lead (Pb)-free and Halogen-free)


ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	40	- 40	V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	6.8	- 5.8	A
	T _C = 70 °C		5.4	- 4.7	
	T _A = 25 °C		5.6 ^{b, c}	- 4.7 ^{b, c}	
	T _A = 70 °C		4.4 ^{b, c}	- 3.7 ^{b, c}	
Pulsed Drain Current		I _{DM}	20	- 20	
Source-Drain Current Diode Current	T _C = 25 °C	I _S	2.5	- 2.5	
	T _A = 25 °C		1.6 ^{b, c}	- 1.6 ^{b, c}	
Pulsed Source-Drain Current		I _{SM}	20	- 20	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	7	- 10	
Single Pulse Avalanche Energy		E _{AS}	2.45	5	mJ
Maximum Power Dissipation	T _C = 25 °C	P _D	3.0	3.1	W
	T _C = 70 °C		1.9	2	
	T _A = 25 °C		2.0 ^{b, c}	2.0 ^{b, c}	
	T _A = 70 °C		1.25 ^{b, c}	1.25 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	N-Channel		P-Channel		Unit
			Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	54	64	49	62.5	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	33	42	30	40	

Notes:

a. Based on T_C = 25 °C.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. Maximum under Steady State conditions is 120 °C/W.

SPECIFICATIONS T _J = 25 °C, unless otherwise noted								
Parameter	Symbol	Test Conditions		Min.	Typ. ^a	Max.	Unit	
Static								
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	N-Ch	40			V	
		V _{GS} = 0 V, I _D = - 250 μA	P-Ch	- 40				
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	N-Ch		44		mV/°C	
		I _D = - 250 μA	P-Ch		- 42			
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	N-Ch		- 5.5			
		I _D = - 250 μA	P-Ch		4.6			
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1.4		3.0	V	
		V _{DS} = V _{GS} , I _D = - 250 μA	P-Ch	- 1.2		- 2.5		
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	N-Ch P-Ch			100 - 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V	N-Ch			1	μA	
		V _{DS} = - 40 V, V _{GS} = 0 V	P-Ch			- 1		
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch			10		
		V _{DS} = - 40 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch			- 10		
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	N-Ch	10			A	
		V _{DS} = - 5 V, V _{GS} = - 10 V	P-Ch	- 10				
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 5 A	N-Ch		0.0295	0.0355	Ω	
		V _{GS} = - 10 V, I _D = - 5 A	P-Ch		0.037	0.045		
		V _{GS} = 4.5 V, I _D = 4 A	N-Ch		0.0355	0.0425		
		V _{GS} = - 4.5 V, I _D = - 4 A	P-Ch		0.050	0.062		
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 5 A	N-Ch		22		S	
		V _{DS} = - 15 V, I _D = - 5 A	P-Ch		14			
Dynamic ^a								
Input Capacitance	C _{iss}	N-Channel V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz P-Channel V _{DS} = - 20 V, V _{GS} = 0 V, f = 1 MHz	N-Ch		640		pF	
Output Capacitance	C _{oss}		P-Ch		970			
			N-Ch		73			
			P-Ch		120			
Reverse Transfer Capacitance	C _{rss}	N-Ch		41				
		P-Ch		95				
Total Gate Charge	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 5 A	N-Ch		11.7	20	nC	
		V _{DS} = - 20 V, V _{GS} = - 10 V, I _D = - 5 A	P-Ch		25	38		
	N-Channel V _{DS} = 20 V, V _{GS} = 4.5 V I _D = 5 A	N-Ch		5.3	9			
		P-Ch		11.8	18			
Gate-Source Charge	Q _{gs}	N-Ch		1.9				
		P-Ch		3.0				
Gate-Drain Charge	Q _{gd}	N-Ch		1.7				
		P-Ch		5.2				
Gate Resistance	R _g	f = 1 MHz	N-Ch	0.5	2.2	4.5	Ω	
			P-Ch	1.0	5.5	11		



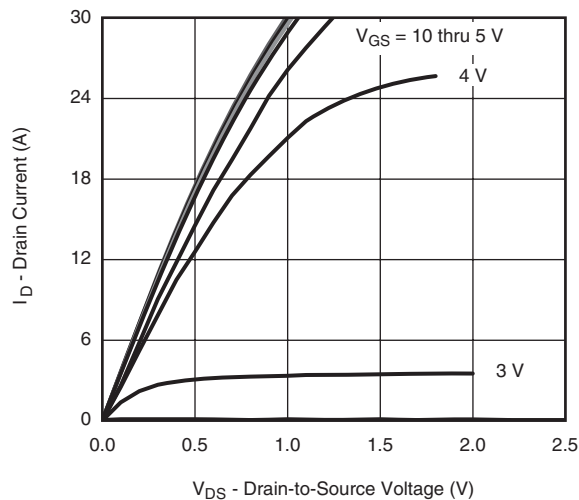
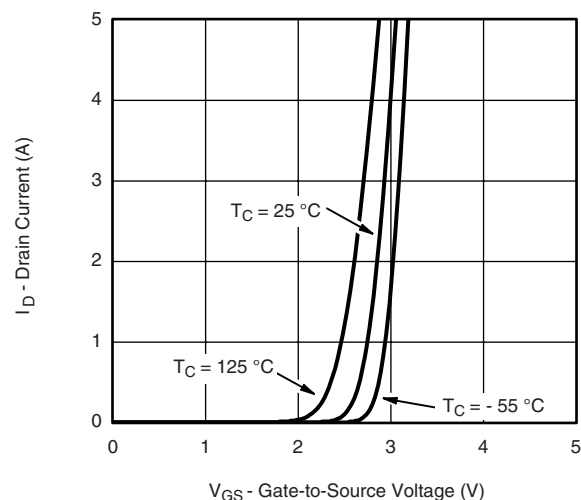
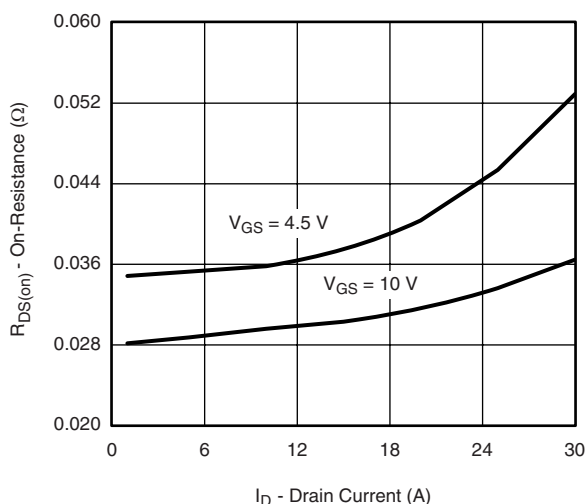
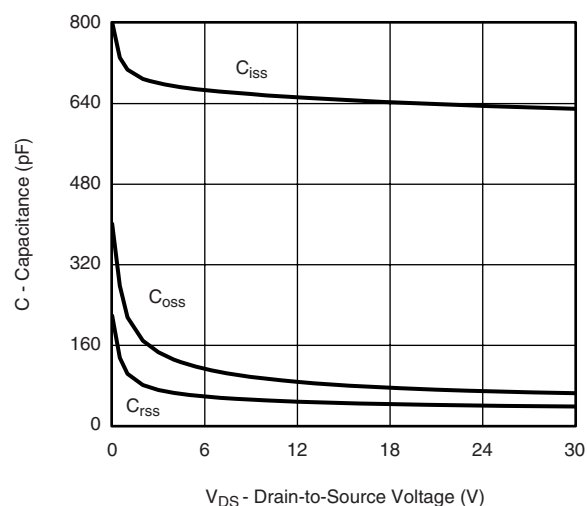
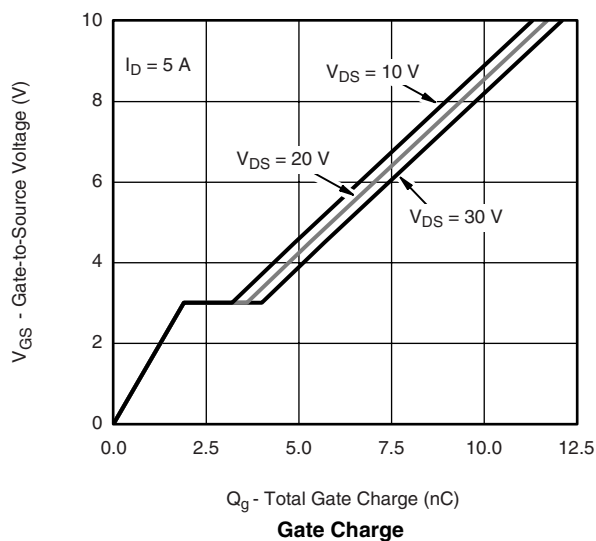
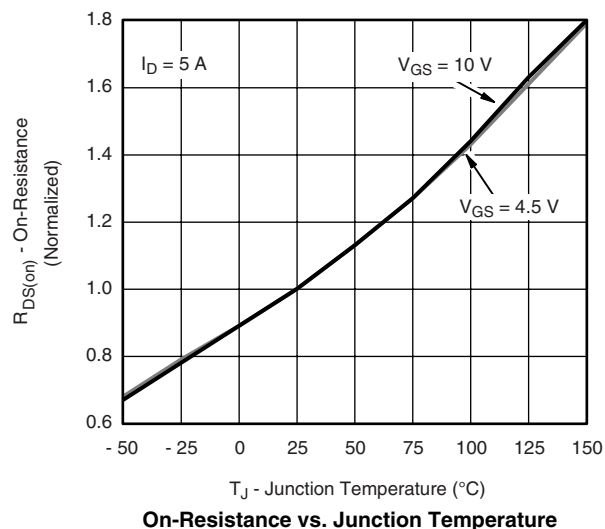
SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions		Min.	Typ. ^a	Max.	Unit
Dynamic ^a							
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 20\text{ V}$, $R_L = 4\text{ }\Omega$ $I_D \cong 5\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$	N-Ch		7	14	ns
			P-Ch		7	14	
Rise Time	t_r		N-Ch		10	20	
			P-Ch		12	24	
Turn-Off Delay Time	$t_{d(off)}$	N-Ch		15	30		
		P-Ch		30	60		
Fall Time	t_f	N-Ch		9	18		
		P-Ch		9	18		
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 20\text{ V}$, $R_L = 4\text{ }\Omega$ $I_D \cong 5\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$	N-Ch		16	30	
			P-Ch		44	80	
Rise Time	t_r		N-Ch		17	30	
			P-Ch		33	50	
Turn-Off Delay Time	$t_{d(off)}$	N-Ch		16	30		
		P-Ch		28	60		
Fall Time	t_f	N-Ch		10	20		
		P-Ch		13	25		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$	N-Ch			2.5	A
			P-Ch			- 2.5	
Pulse Diode Forward Current ^a	I_{SM}		N-Ch			20	
			P-Ch			- 20	
Body Diode Voltage	V_{SD}	$I_S = 1.6\text{ A}$	N-Ch		0.78	1.2	V
		$I_S = - 1.6\text{ A}$	P-Ch		- 0.76	- 1.2	
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$	N-Ch		19	30	ns
			P-Ch		26	50	
Body Diode Reverse Recovery Charge	Q_{rr}		N-Ch		14	25	nC
			P-Ch		18.5	35	
Reverse Recovery Fall Time	t_a	$I_F = - 2\text{ A}$, $di/dt = - 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$	N-Ch		13		ns
			P-Ch		12.5		
Reverse Recovery Rise Time	t_b		N-Ch		6		
			P-Ch		13.5		

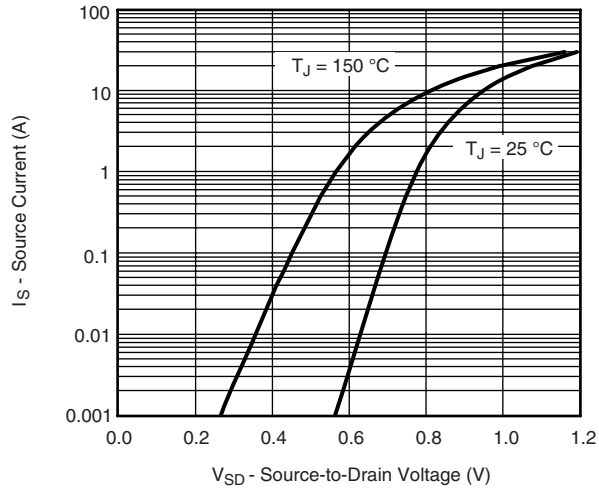
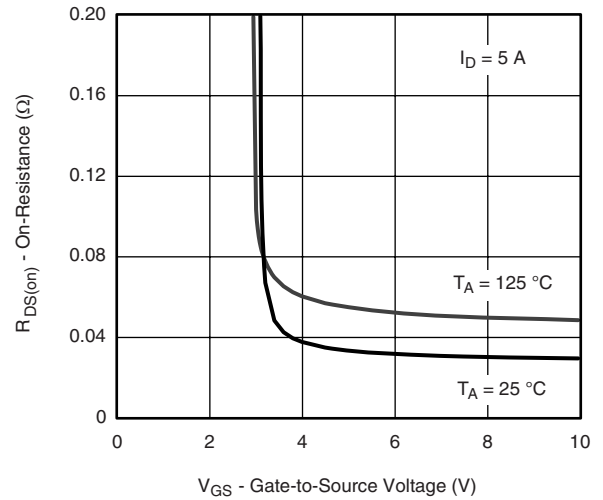
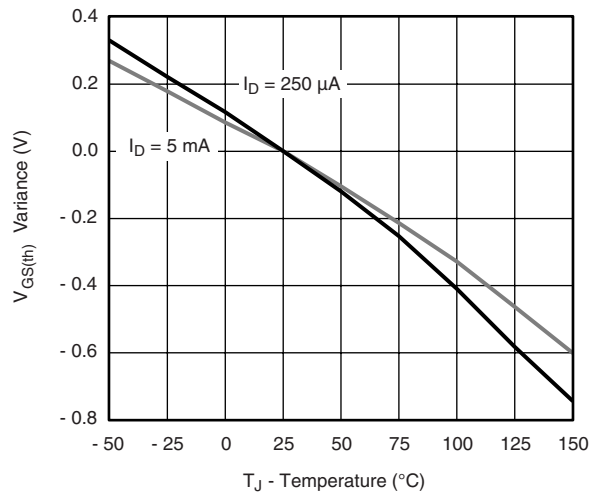
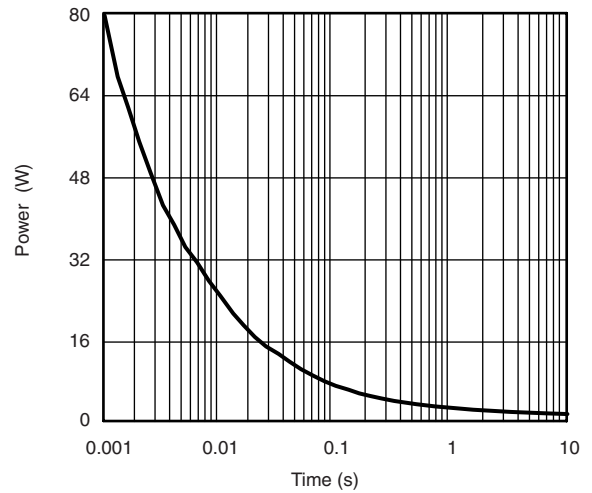
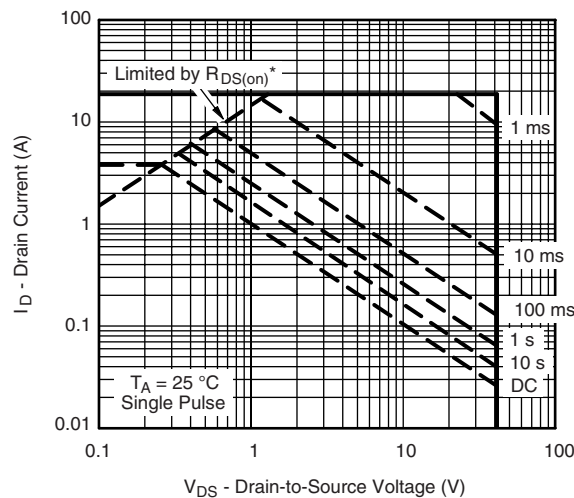
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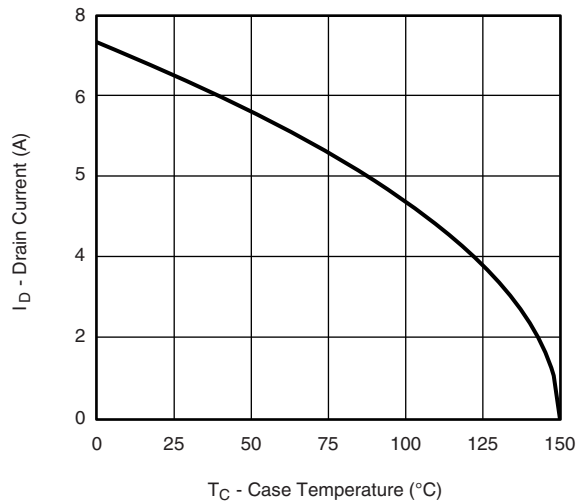
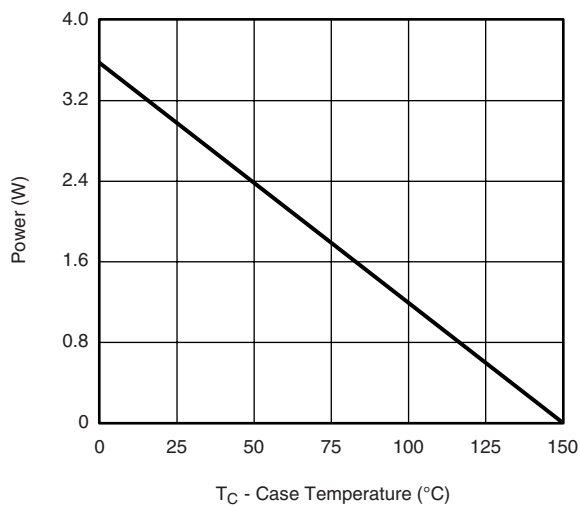
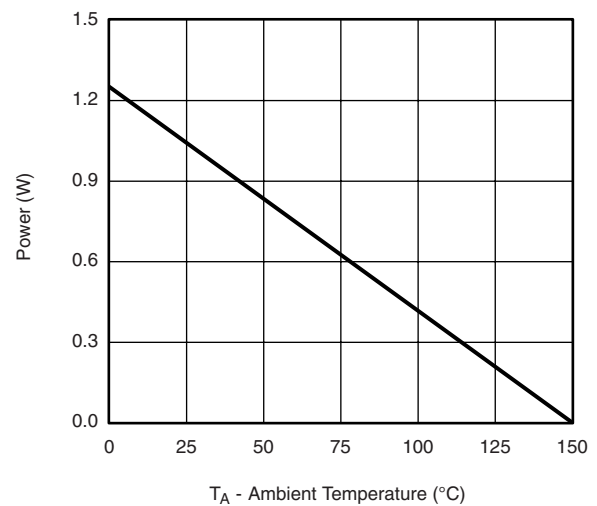
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

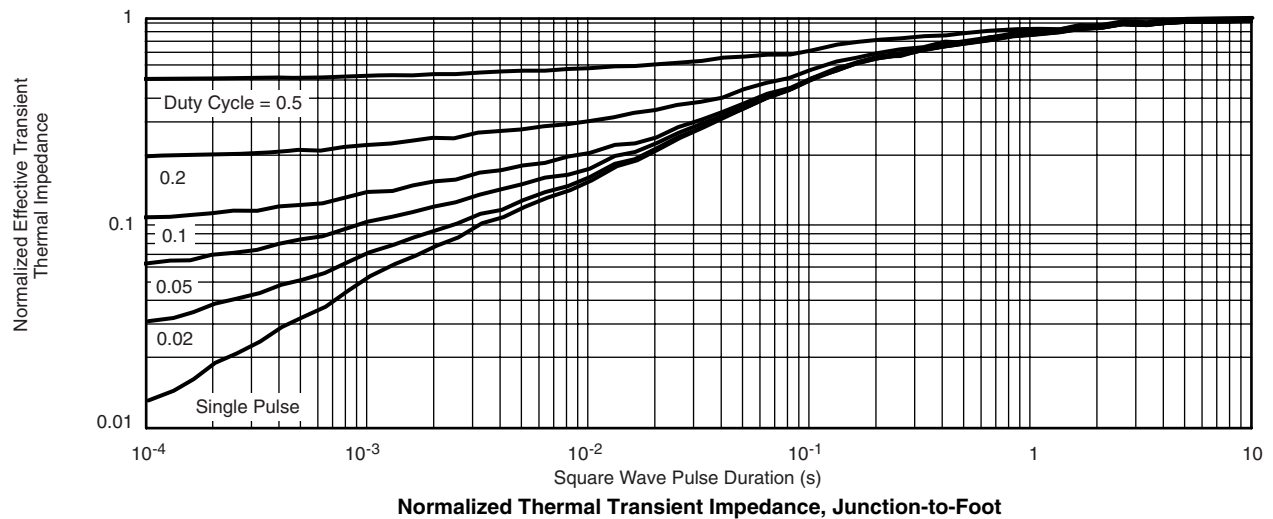
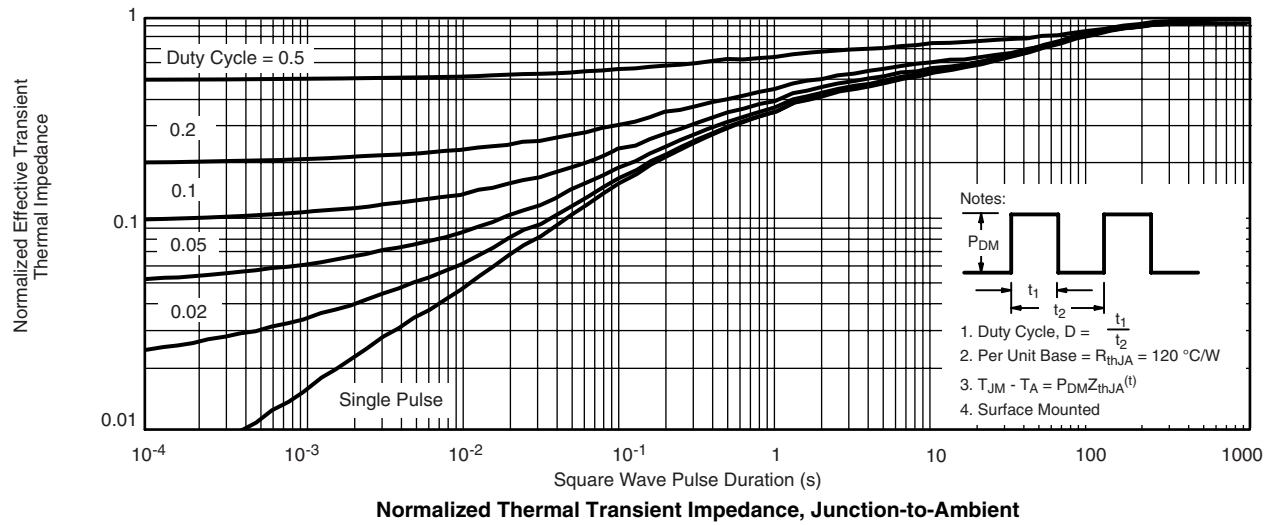
**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient*** $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**

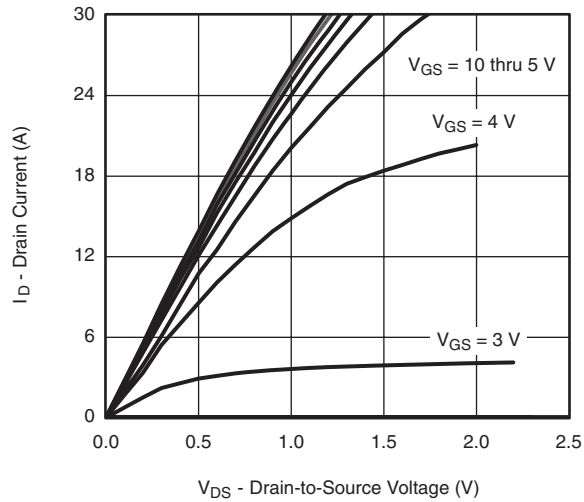
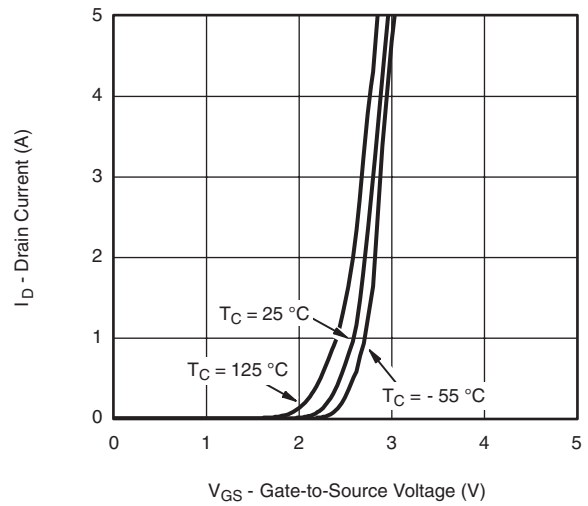
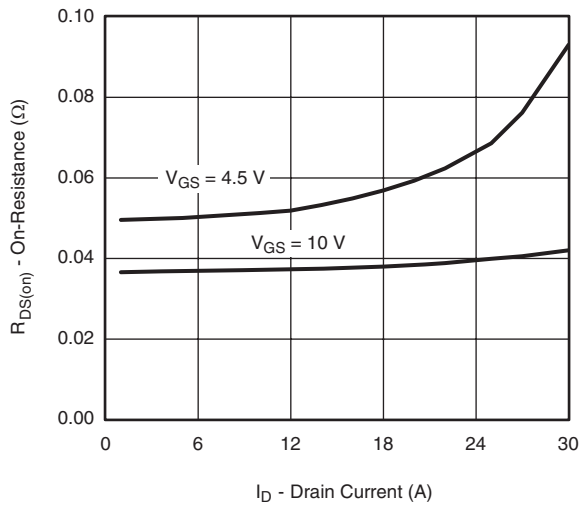
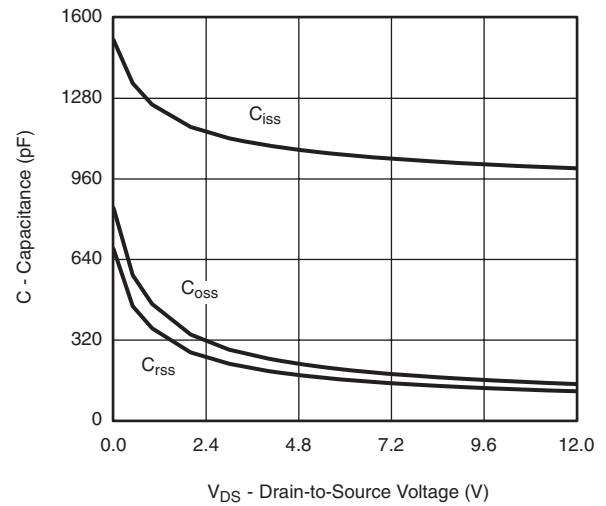
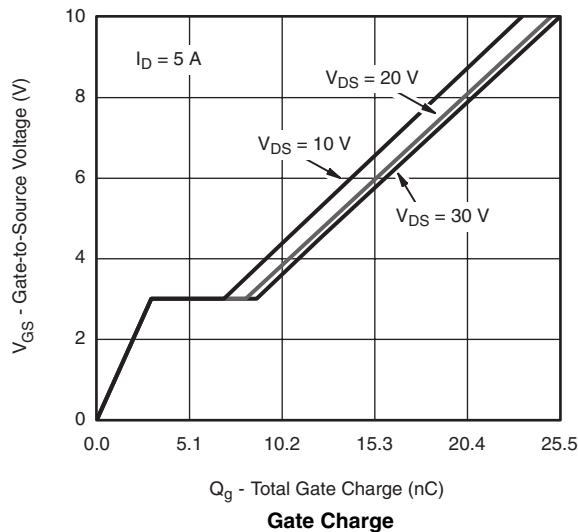
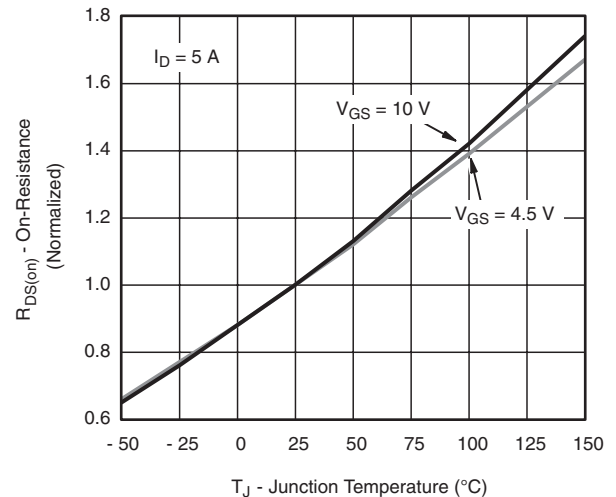
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Current Derating*****Power Derating, Junction-to-Foot****Power Derating, Junction-to-Ambient**

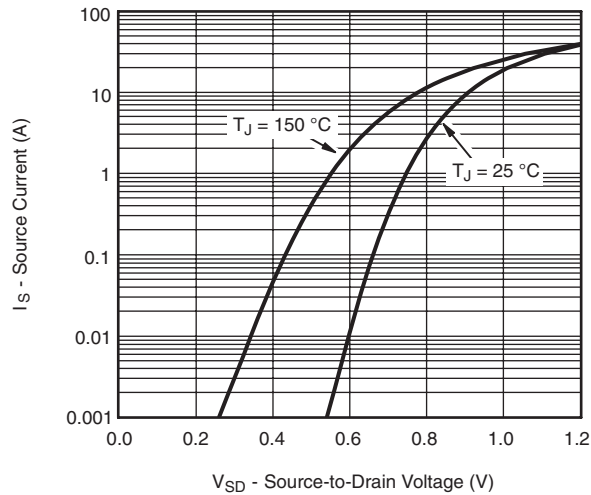
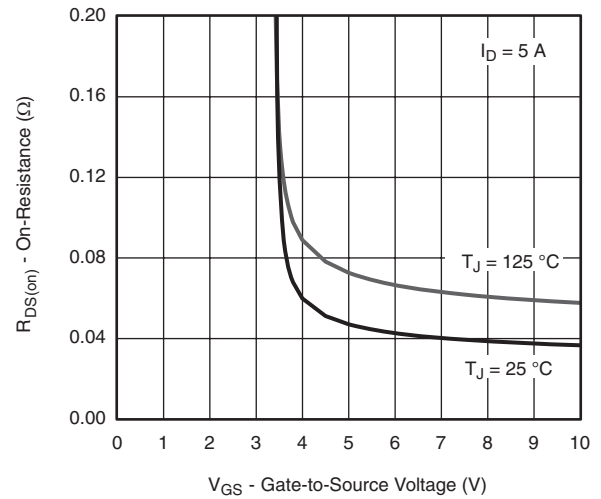
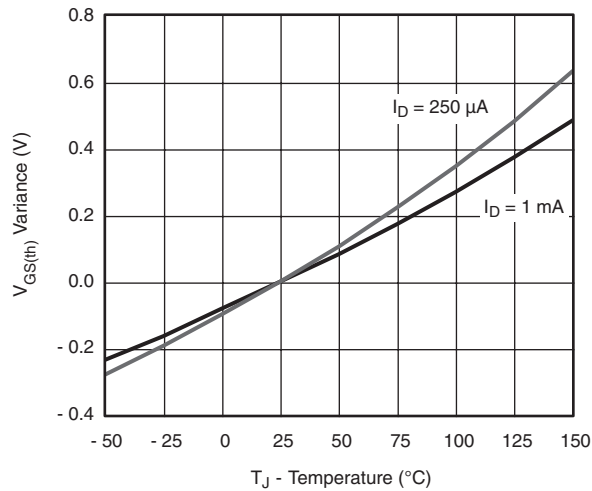
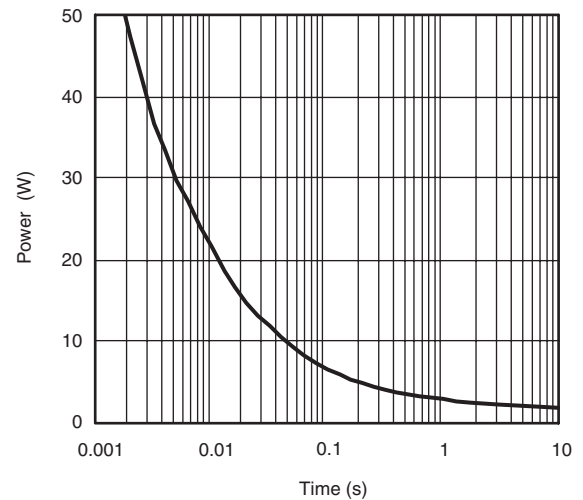
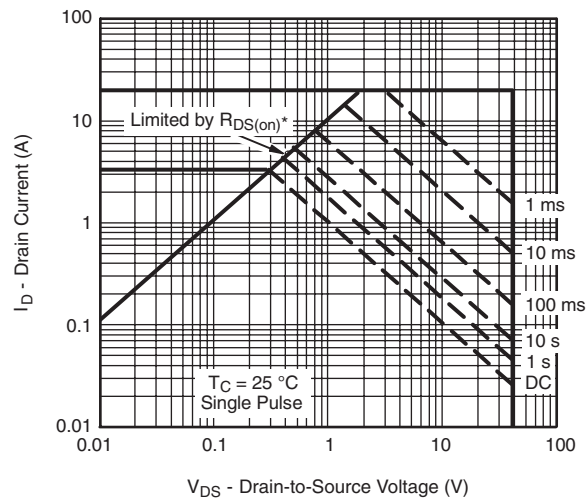
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

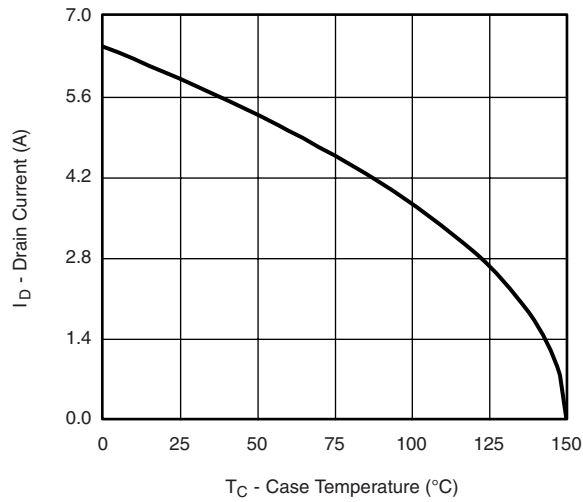
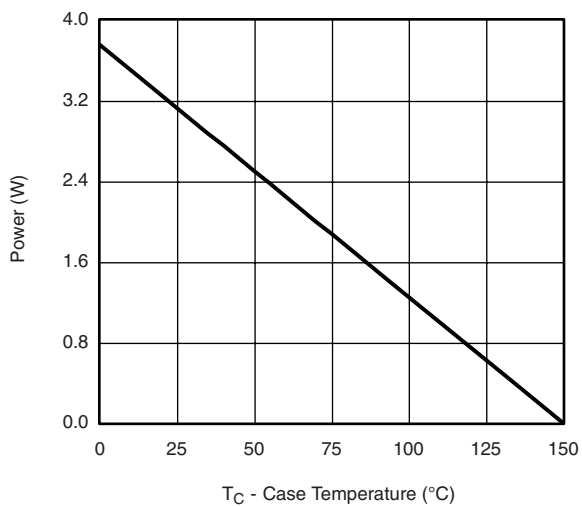
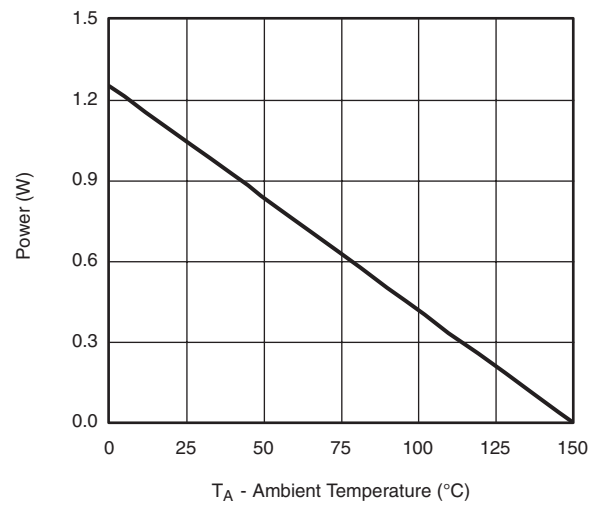


N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

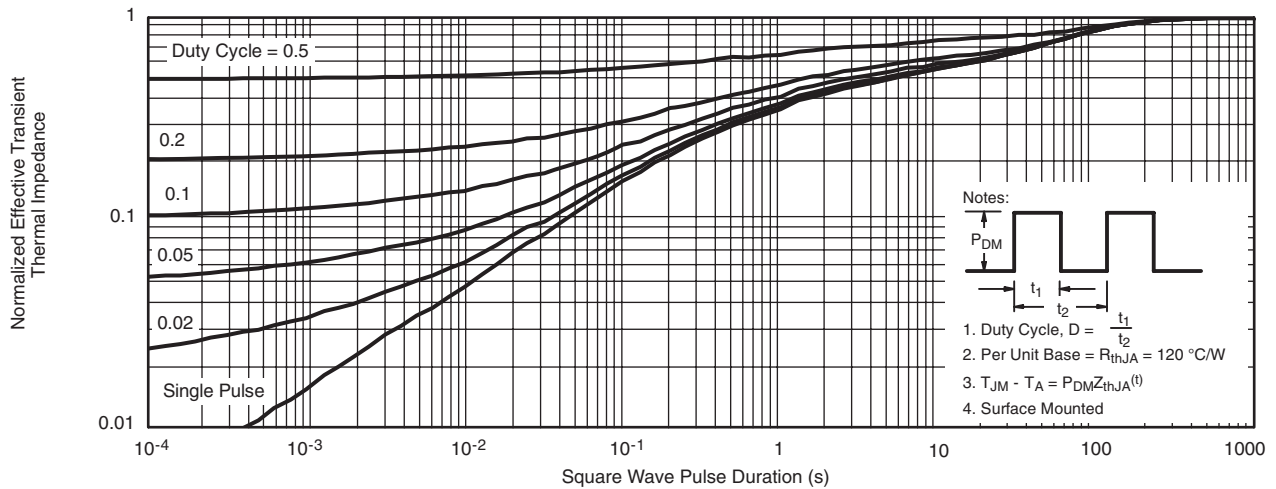
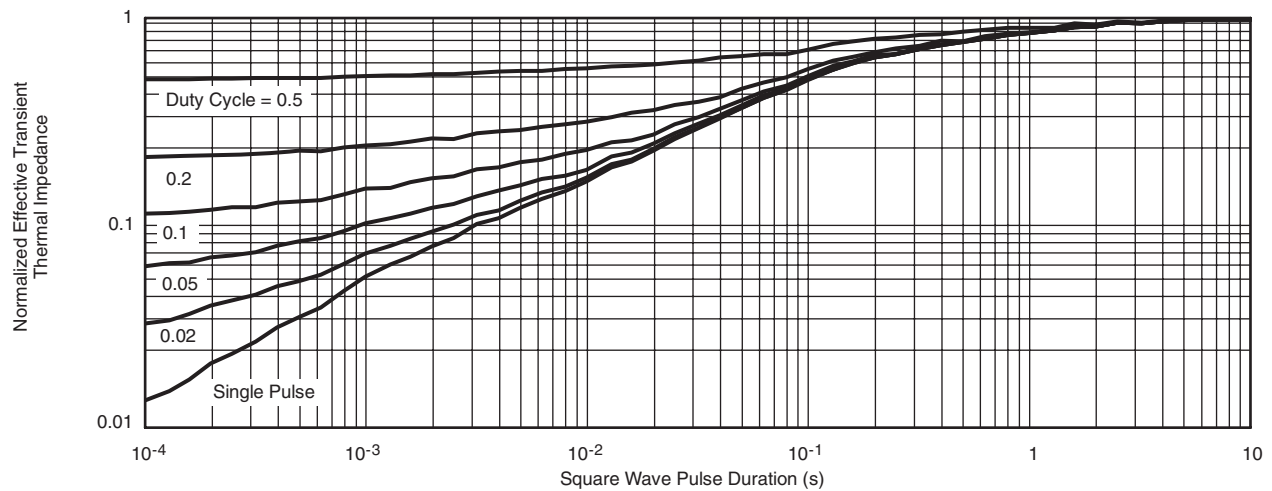


P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Current Derating*****Power Derating, Junction-to-Foot****Power Derating, Junction-to-Ambient**

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Foot**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?68971>.

SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026

ECN: C-06527-Rev. I, 11-Sep-06
DWG: 5498

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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